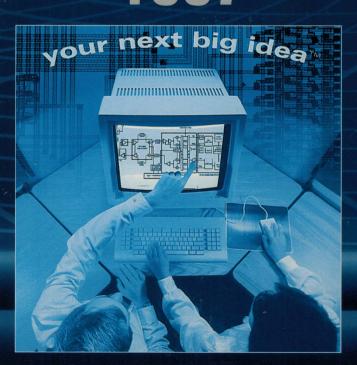
APPLICATIONS FOR

# APPLICATIONS FOR COMMUNICATION ICS 1997

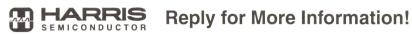




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Which category best describes y  100 Video/Imaging  1101 - Desktop Multimedia 1102 - Prof/Broadcast Video 1103 - Medical Imaging 1104 - Cable TV 1105 - Video Conferencing 1199 - Other Video/Imaging  1200 Wireless Communication 1201 - Base Stations 1202 - Wireless LAN/PCS/PB 1203 - Handset/Terminals 1204 - Satellite Communication 1205 - Wireless Local Loop 1299 - Other Wireless Comm. 1300 Government/Military 1301 - Space 1302 - Guidance/Control 1303 - Radar 1304 - Communications	1305 - Avionics 1399 - General Gov't/Military 1400 Telecom 1401 - PBX or CO Line Cards 1402 - Fiber-in-the-Loop 1403 - Wireless Local Loop 1404 - Fiber Optics 1405 - ADSL/HDSL 1406 - Other High Speed Datacomm 1499 - Other Telecom 1500 Computers/Peripherals 1501 - Laptops/Palmtops 1502 - Desktop PCs 1503 - Workstation/File Server 1504 - Disk/Tape Drives 1505 - Printers/Plotter/Scanner 1506 - Datacomm 1599 - General Computer/EDP	1600 Transportation/Consumer 1601 - Power Train 1602 - Vehicle Control 1603 - Safety & Convenience 1604 - Driver Information 1605 - Entertainment 1606 - Electric Vehicles 1607 - Consumer 1699 - Other Transportation 1700 Power Supply/Power Mgmt 1701 - UPS (Uninterruptible Power Supplies) 1702 - AC-DC Power Supplies 1703 - DC-DC Power Supplies 1704 - Transmission Lines 1705 - Utility Substations 1706 - Panel Boxes 1707 - General Protection 1799 - Other Power Supplies/Mgmt	1800 Motor Control  1801 - AC Motors  1802 - 3 Phase Motors  1803 - Brushless  1804 - DC Motors  1805 - Stepper Motors  1809 - Other Motor Control  1900 Industrial Controls & Instrumentation  1901 - Manufacturing System  1902 - High Speed Instrumentation  1903 - Handheld Instruments  1904 - Medical Electronics  1905 - HVAC  1906 - Automatic Test Equipment (ATE)  1999 - General Industrial & Instrumentation  2000 Other Electronics, Not Listed Above
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### HARRIS COMMUNICATION PRODUCTS

As one millennium comes to a close and a new one approaches, a revolution is upon us. The telecommunications industry is experiencing rapid social and regulatory change throughout the world. Fueled by advancing technology, the upsurge of change is gaining momentum. Consumers now have access to technology that less than a decade ago only the military could afford. From Internet access to personal communications systems, consumers are demanding higher data rates and more bandwidth at lower costs. To address these needs Harris Semiconductor is developing highly integrated chip set solutions targeted for the communications market.

This book is organized to help the reader quickly find solutions for their particular needs and applications. Section 1 contains a listing of our new products, followed by Section 2 with the table of contents and general information. Section 3 is dedicated to wireless communication products. In this section, you will find highly integrated solutions for applications such as wireless LAN and wireless point-to-point applications. Section 4 represents applications for wired communication systems. It includes product solutions for applications such as ISDN modems, ADSL, Cable telephony and PBX systems. Section 5, our standard products section, contains application notes describing communication products including Data Acquisition and Digital Signal Processing. Complete data sheets for Standard Products can be obtained from our Internet web site, http://www.harris.com/, AnswerFAX, the Harris fulfillment center, or your local sales office or authorized distributor, (see Section 8).

Section 6 contains a listing of Development Tools including SPICE models, evaluation boards, macromodels, etc. Complete information about these tools is available from any of the above referenced sources.

Section 7 contains information on how to use Harris' on-line services to obtain data sheets and application notes. And last but not least, Section 8 contains a listing of our world wide sales offices.

For complete, current and detailed technical specifications on any Harris devices, please contact the nearest Harris sales, representative or distributor office, listed in Section 8; or direct literature requests to:

Harris Semiconductor Data Services Department P.O. Box 883, MS 53-204 Melbourne, FL 32902 Phone: 1-800-442-7747 Fax: 407-724-7240

This data book is an invaluable reference for engineers and technicians in the communications field. Please contact your local sales office listed in Section 8 for further assistance.

For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG201; ordering information above).

All Harris Semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Harris Semiconductor products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/ or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Harris is believed to be accurate and reliable. However, no responsibility is assumed by Harris or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Harris or its subsidiaries.



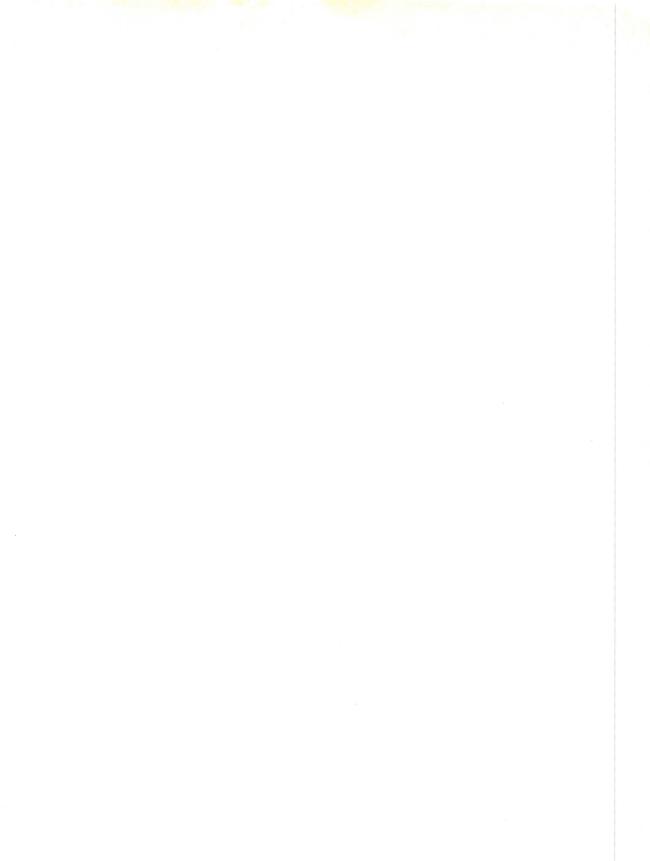
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HFA3421	1.7GHz - 2.3GHz Low Noise Amplifier	4288
HFA3661	2.0GHz to 2.7GHz DownConverter	4240
HFA3663	2.3GHz UpConverter with Gain Control	4241
HFA3726	400MHz Quadrature IF Modulator/Demodulator	4310
HFA3761	400MHz AGC and Quadrature IF Demodulator	4236
HFA3763	400MHz Quadrature Modulator and AGC	4237
HFA3824	Direct Sequence Spread Spectrum Baseband Processor	4308
HFA3926	2.0GHz - 2.7GHz 250mW Power Amplifier	4282
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HC55171 (Note)	5 REN Ringing SLIC for ISDN Modem/TA and WLL	4323
HC5503 (Note)	Low Cost 24 Volt SLIC for PABX/Key Systems	
HC5519	ITU CO SLIC with Polarity Reversal and Integrated Combo	4232
HC5520	ITU CO SLIC with Polarity Reversal	4148
HC5521	ITU PABX SLIC with Polarity Reversal and Ground Key Detect	4265
HC5513	TR909 DLC/FLC SLIC with Low Power Standby	3963
HC5515	ITU CO/PABX SLIC with Low Power Standby	4235
HC5523	LSSGR/TR57 CO/Loop Carrier SLIC with Low Power Standby	4144
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HC-5502B1	ITU Low Cost, PABX SLIC with 30mA Loop Feed	4127
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HC-5502B	EIA/ITU PABX SLIC with 30mA Loop Feed	2884
HC-5524	EIA/ITU 24 Volt PABX SLIC with 25mA Loop Feed	2798
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HI5731	12-Bit, 100 MSPS High Speed D/A Converter	4070
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HSP50214	Programmable Downconverter	4266
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HSP50306	Digital QPSK Demodulator	4162
HSP50307	Burst QPSK Modulator	4219

NOTE: Coming soon.

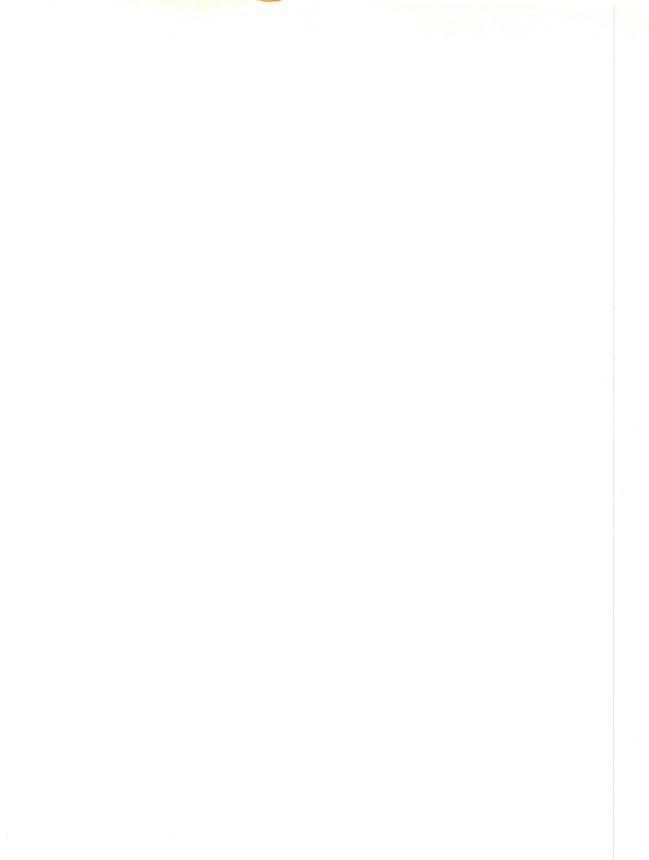
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# MAPPOTE

No. AN9614.1 January 1997

### Harris Wireless Products

### Using the PRISM™ Chip Set for Low Data Rate Applications

Authors: Carl Andren and John Fakatselis



### ™ Introduction

The PRISM™ chip set has been optimized to address high data rate applications with up to 4 MBPS data rates. The

PRISMTM can also be utilized for low data rate applications. To implement low data rate applications (below 250 KBPS) the designer needs to address design considerations in the following areas:

- A. Selection of external filtering supporting the PRISM™ components.
- B. Limitations on filter cut off frequencies of the HFA3724 internal Low Pass Filters.
- C. Selection of appropriate carrier and clock oscillators to achieve the desired performance, given the HSP3824 internal Acquisition and Tracking loop integration constraints.

The system designer should also evaluate the option where the radio maintains its high data rate configuration but transmits the data using infrequent high data rate burst packets.

Where the system requires that the radio operate at low rates (<250 KBPS), the designer must address the areas highlighted on the PRISM™ block diagram shown in Figure 1.

### Description

### A. External IF Filtering

The band pass filters shown between the HFA3624 and the HFA3724 labeled as BPF1a and BPF1b on Figure 1 are centered at IF and filter the spread wideband waveform before demodulation on the receive side and before the final upconversion on the transmit side.

One might think that the TX filter can be avoided but it is required to meet the sidelobe suppression specifications according to FCC requirements.

### PRISM™ PCMCIA Reference Radio Block Diagram

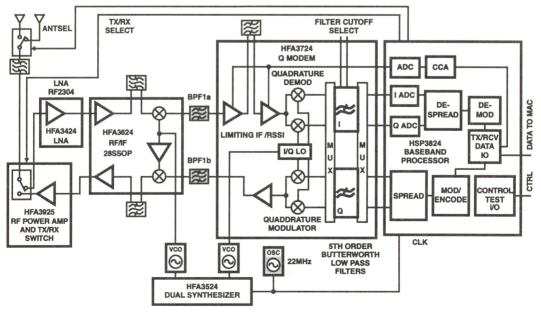


FIGURE 1. PRISM™ CHIP SET BLOCK DIAGRAM

For the high rate configuration of the PRISM™, a recommended implementation is to use SAW BPFs centered at 280MHz with a BW of about 17MHz. This is assuming an 11MHz chip rate (thus 22MHz spread null to null bandwidth). A recommended device that meets these requirements is the ToyoCom TQS-432.

If a low data rate configuration is implemented then substitute IF filters need to be identified that will filter to the channel bandwidth of the spread waveform at the lower chip rate. The designer can use any IF center frequency within the HFA3724 range. The designer must be sure, though, that the identified filter meets the transmission spectral mask requirements for FCC for the 2.4MHz ISM band. SAW filters for PCMCIA applications are not widely available at these specifications and a custom design may be required.

### B. Limitations of HFA3724 LPFs

The HFA3724 includes a set of baseband low pass filters as the final filtering stage of the complex spread waveform. These are placed before the In phase (I) and Quadrature (Q) A/D converters for baseband processing. These filters are shown on Figure 1, as LPFs (Rx) and LPFs(TX). There are four cut off frequencies that can be selected for these LPFs. The cut off can be selected to be 17.6MHz (for a chip rate of 22 MCPS), 8.8MHz (for a 11 MCPS rate), 4.4MHz (for a 5.5 MCPS rate) or 2.2MHz (for a 2.75 MCPS rate). In addition these cut off frequencies are tunable through an external resistor by ±20%. The user can select one of the four discrete cut off frequencies. The lowest cut off is set for a spread rate of 2.5MHz chip rate and any chip rates lower than this will require the design of external filtering between the HFA3724 outputs and the HSP3824 A/D inputs. The HFA3724 I and Q LPFs are fifth order Butterworth filters and equivalent external filters need to be designed at the lower cut off specifications.

### C. Selection of Carrier Frequency and Clock Oscillators

The HSP3824 performs the baseband demodulation function. The design includes digital signal acquisition and tracking loops for both the symbol timing clock and the carrier frequency.

The primary concern when the radio needs to be operated with a low instantaneous data rate is that it requires a wide bandwidth to accommodate oscillator frequency tolerances.

As an example at 2400MHz and ±25 PPM, the radio frequencies at each end of the link can be off by as much as 120kHz from each other. This offset must be well within the basic data bandwidth of the radio in order for it to be tolerated without degrading the performance of the link. If it is not, a frequency sweep would be needed to find the signals and this is not built into the radio design. Operating the radio with wide data bandwidth and low data rate is inefficient and would cause unacceptable loss in performance.

If the PRISM™ is used as a spread spectrum system with 11 chips per bit spreading ratio, this then gives it an IF bandwidth of nominally 22MHz null to null at 1 MSPS. We filter to 17MHz to allow closer packing of the channels. While this seems wide compared to the frequency offset, remember

that this is a direct spread system. The first stage of processing the signal despreads it and collapses it to the data bandwidth. In PRISM™ this is done in a time invariant matched filter correlator. This correlator has an FIR filter structure where the PN sequence is substituted for the tap weights. The filter is operated at baseband, so the I and Q quadrature components are separately correlated with the same sequence. The outputs of the I and Q correlators are the vector components of the correlation. These will show a distinct peak in magnitude (compressed pulse) when correlation occurs. Correlation performance falls off when the signal is not stationary (i.e. has offset). The correlator convolves a stationary signal, (the PN sequence) with the input signal. The vector correlation is being rotated throughout the correlation by the offset frequency. This means that the signal correlates at one angle at the start of a symbol and at a different angle at the end. If this angular difference is small, no great loss occurs. The net correlation goes as the vector sum of all the correlation angles between the start and the end of the symbol as shown below. Thus the magnitude falls off to zero if the offset causes a baseband phase rotation of one cycle per symbol. The magnitude is obviously maximum at no offset and falls off about 0.22dB at 45 degrees rotation. This corresponds to the 120kHz offset (~1/8th of 1 MBPS).

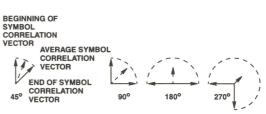


FIGURE 2. PRISM™ CORRELATION PERFORMANCE vs FREQUENCY OFFSET

Crystal oscillators of better than  $\pm 25$  PPM accuracy can be purchased, but their cost goes up significantly as the tolerances are tightened. Given this offset, we must be sure that the receiver can accept the offset. At a data rate of 250 KBPS, the same offset loss occurs with a frequency offset 1/4th as large. This means that to get the same performance, we need oscillators specified to  $\pm 6$  PPM. To go lower in data rate means tightening up the specification even further.

Similar consideration needs to be taken for the clocks that are used to run the baseband processor itself. The symbol timing clock tracking algorithm operates over 128 symbol integration intervals. To maintain acceptable BER performance the symbol timing phase drift must be less than 1/8th chip over the 128 symbol integration interval. Remember that we are tracking the peak of the compressed pulse which is 2 chips wide and must keep the straddling loss low by sampling close to the peak. For a 0.25 MBPS data rate, the chip rate is 2.75 MCPS. With this rate, the integration interval is 512ms which translates to an oscillator within ±89 PPM to keep the drift less than 1/8th chip (0.045ms). Since the spread rate to data rate ratio is not changed at the lower data rates, this tolerance is not effected by lower data rates.

### **High Rate Burst Transmissions With Low Average Rate**

Generally, the incentive to use lower data rates is to achieve a given range with the minimum amount of power. We can show that this is also achievable by using the radio in its high data rate design configuration. The PRISM™ is a packet radio communications device and, as such, can send the data in a short burst with open environment ranges up to 5 miles. This has significant potential for power savings and reduction in interference. In the high data rate configuration the design considerations mentioned above are no longer of concern.

The system approach is to accept the 1 MBPS data rate of the radio as long as the achievable range is acceptable, and use it in a short burst mode which is consistent with its' packet nature. With a low power watch crystal, the controller can keep adequate time to operate either a polled or a time allocated scheme. In these modes, the radio is powered off most of the time and only awakens when communications is expected. This station would be awakened periodically to listen for a beacon transmission. The beacon serves to reset the timing and to alert the radio to traffic. If traffic is waiting, the radio is instructed when to listen and for how long. In a polled scheme, the remote radio can respond to the poll with its traffic if it has any. With these techniques, the average power consumption of the radio can be reduced by more than an order of magnitude while meeting all data transfer objectives.

Even using the 802.11 network protocols, the low data rate can allow low average power operation. The Media Access Controller (MAC) or network processor can operate the radio in the sleep mode except for the times it needs to receive the beacon signals.

The short, fast transmission is good for several reasons. First, if the signal is corrupted for any reason, a retransmission will occur without noticeable delay. Secondly, interference to other spectrum users is of brief duration. Third, and most important, the burst can be sent into small time gaps in the medium, which makes it more effective against certain type of interference in the ISM band. For example, if an 802.11 FH network is operating in the vicinity, it could cause interference with this network. The FH network has, however, a brief guard time when it is hopping and none of its stations are on the air. This time can be used to transmit the burst communications packets. Additionally, the microwave oven has been identified as an interference source of concern within the 2.4GHz ISM band. The oven is a pulsed source with about a 50% duty cycle. The gaps allow messages of about 1000 bytes through at the 1 MBPS rate.

In addition, the system can be set at its sleep mode most of the time to achieve low power consumption. It only needs to operate at full power consumption during the transmission of a packet or during the expected window for received packets.

The communications range achievable depends on the nature of the environment. A line of sight (LOS) path allows the best range. With 1W and 6dB gain in the antennas, you can readily achieve a 5 mile LOS range. The propagation loss at S-band is less than 0.5dB per mile in heavy rain, so weather is not usually of great concern. Antennas with 6dB gain are for fixed installations with one on one links. Mobile and network installations use omnidirectional antennas with around 0dB gain. Indoors, the range is much reduced by extra losses due to walls and other obstructions. The power is also usually reduced to 100mW for interference and safety concerns. These reduce the available range, but most applications will achieve sufficient range (300 ft.).

Antenna diversity is also used in the PRISM™ design to combat multipath interference. Since the PRISM™ waveform is wideband by being spread at the chip rate, the 1 MBPS data rate is not a contributor to multipath problems and a lower data rate is of no benefit.

So, in general, unless it is required to use low instantaneous data rates to achieve some other purpose, the packet capabilities of PRISM™ will serve well for these applications in its normal high data rate design configuration.

# M APPROTE

No. AN9615 April 1996

### Harris Digital Signal Processing

### Using the HSP3824 Evaluation Board and Associated Software

Authors: Carl Andren, John Fakatselis (Harris Semiconductor) and Eric Turner (Squires Engineering)

## (T)

### Introduction

This application note describes the Harris PRISM™ Evaluation Board and its associated evaluation software referred to as

the SW. This covers a functional overview of the software interface with a description of the user screen layout philosophy. It includes a description of the configuration form and of the self-test utility.

The evaluation board SW supports (but does not require) the Harris HSP3824 evaluation boards.

For details on the operation of the HSP3824, refer to the datasheet entitled "HSP3824 Direct Sequence Spread Spectrum Baseband Processor."

The evaluation board kit includes the hardware PC board, a copy of the configuration SW, cabling required for external interfaces including the cable required for the computer interface, the HSP3824 Datasheet and this evaluation board application note. Each of the PC boards has one HSP3824 device.

The power supplies and clock sources are provided externally. The SW runs on any PC with WINDOWS™ 3.1 or 95. The PC interfaces with the evaluation board through its parallel port. There is no signal processing done at the PC. The PC interface is required as the user interface to configure the HSP3824 into its various modes of operation and to monitor the data from the internal registers of the HSP3824.

### External Interfaces

The following external hardware interfaces are required as shown on the block diagram of Figure 1.

### **PC Interface**

This interface is between the parallel PC port and J3B of the evaluation board. The cable for this interface is provided by Harris as part of the evaluation kit. The interface is for programming the registers on the HSP3824.

### **Power Supply Interface**

There is a single power supply connection for the entire evaluation board. The cabling that connects with the external supply is already provided on the board. Refer to the HSP3824 Datasheet for supply voltage specifications.

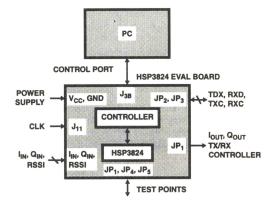


FIGURE 1. HSP3824 EVALUATION BOARD TOP LEVEL INTERFACE BLOCK DIAGRAM

### Clock Interface

The clock is provided through an external source at the SMA connector  $J_{11}$  of the evaluation board. The board has a  $50\Omega$  resistor on the clock input and is intended for operation with a programmable signal source such as the HP8165A. A typical clock is  $5V_{P.P}$  with 2.5V offset (i.e., CMOS levels) for 5V operation.

### **Note For Power and Clock Interfaces:**

The evaluation board contains an ACTEL configurable gate array that interfaces the computer to the HSP3824. This device is rated only to 10MHz clock with a 5V supply and may fail to perform if it is used over the full HSP3824 voltage and clock rate ranges (i.e., 22MHz at 3V). The ACTEL can normally be programmed at 22MHz, but it is recommended not to exceed its ratings. During programming, the evaluation board clock should not exceed 10MHz and the voltage should be set at 5V.

After programming, the user can increase the clock rate and vary the voltage as required for the evaluation tests of the HSP3824.

### **Analog Inputs Interfaces**

These interfaces are the analog inputs to the HSP3824 A/Ds. They are provided through SMA connectors or through  $JP_5$  on

### **Application Note 9615**

the evaluation board. The SMA connectors are labeled on the board according to their corresponding signal name. That is  $I_{\rm IN}$  for the in phase component of the complex baseband analog waveform,  $Q_{\rm IN}$  for the Quadrature component of the complex baseband waveform and RSSI for the analog RSSI input. The electrical characteristics of these interfaces are included in the HSP3824 Datasheet. These can be  $50\Omega$  terminated on the board with jumpers if desired. For interfacing with the HFA3724 Harris IF Quad modem, they should be set at high impedance.

### **Digital Data and Clock Interface**

This interface is intended to interface with the external digital data generator and receiver. This is typically for evaluation purposes with some form of Bit Error Rate Tester (BERT). The signals of this interface are:

TXD: TX Data; RXD: RX Data; TXC: TX Clock; RXC: RX Clock.

These signals are available on  $\rm JP_2$  and  $\rm JP_3$  of the evaluation board and Harris provides the cable as part of the evaluation kit.

In addition the output digital lout an Qout data, as well as the control and handshaking signals for the TX and RX operations are available through  ${\rm JP_1}$ .

For information on the timing and electrical characteristics of these interface signals refer to the HSP3824 Datasheet.

### **Test Point Interfaces**

A number of signals including signals of the HSP3824 test port are available for access as test points on the evaluation board. These signals are available through JP<sub>1</sub>, JP<sub>4</sub> and JP<sub>5</sub>. For signal pin assignments refer to the attached sche-

matic of this application note. For the description of each of the signals refer to the HSP3824 Datasheet.

### **Jumpers**

There are several jumpers on the evaluation board. These are for connection of the signal inputs to the JP<sub>5</sub> connector and/or to the SMA input connectors. All jumper options are indicated on the attached evaluation board schematic.

### **Test Bed Configuration**

Figure 2 illustrates a recommended configuration to be used for system evaluation of the HSP3824 performance. In order to make proper BER performance measurements the waveform needs to be upconverted to some IF frequency, as a minimum, where noise and interference sources can be used to evaluate performance. This configuration is set to evaluate performance based on continuous transmissions. The user needs to customize a test bed that is appropriate for packetized data performance evaluation. The translation to IF and back to baseband can be accomplished by either using the Harris HFA3724 I, Q modem evaluation board or off the shelf commercially available test equipment. The configuration example in Figure 2 utilizes the HP8780 signal generator, the Noise/Com 6108 noise source, the HP8981 vector analyzer, the HP8657B signal generator, and the Firebert 6000A Bit Error Rate Tester.

### SW Overview

The software supplied with the HSP3824 evaluation kit makes it easy to configure the board. Upon program startup, the user is presented with a "tabbed-notebook" containing eight "pages." Each page represents a logical grouping of various control and status registers in the HSP3824. The

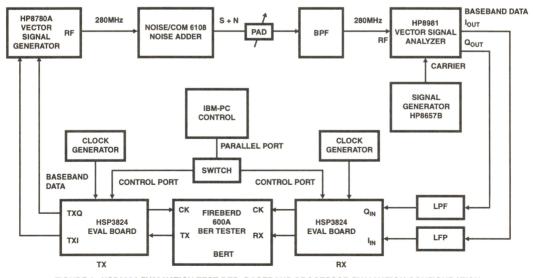


FIGURE 2. HSP3824 EVALUATION TEST BED, BASEBAND PROCESSOR EVALUATION CONFIGURATION

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desired page is made active by selecting the tab associated with that page. Once changes are made to the components on the screen, these values must be downloaded to take effect. The pages are:

### Preamble/Header

Components on this page include preamble generation, transmit modes and receive modes.

### **Modem Configuration**

Components on this page include configuration for transmitter and receiver. The master clock contained on this page is used to calculate and display in "real-time" the transmit and receive symbol rates. Scrambler configuration and antenna operation are also contained on this page.

### I/O Configuration

Components on this page include configuration of active signal levels (polarity) of HSP3824 I/O signals and setup of other miscellaneous I/O signal parameters.

### **Test Port Configuration**

This page contains the configuration component for selection of internal HSP3824 signals and/or data to become available to the evaluation board Test Port pins.

### **Threshold Settings**

Components on this page include a number of configurable threshold settings. It covers Received Signal Strength Indication and Clear Channel Assessment configuration registers, as well as received signal quality thresholds used during acquisition and data tracking.

### A/D Calibration

Components on this page include configuration data to activate the A/D level adjustment circuit of the HSP3824.

### **Modem Status**

Components on this page represent modem status (readonly) registers. These modem status components are updated approximately once per second.

### Signal Status

Components on this page represent both control and status registers. The status components have a green background to discriminate them from control components. Components on this page include preamble information, received signal quality indicators and signal field configuration.

### Other Status

In addition, there is a status area in the lower left corner of the main screen. The status display contains:

- Current Time
- Current Communication (Printer) Port
- . Currently Active Board
- Chip Detected (PN Acquisition)

On the bottom right of the screen are several shortcut buttons. The buttons are:

### Configure Button

This button calls up the configuration dialog box.

### Download Button

This button downloads (with verification) the current control register values.

### Exit

This button exits the Evaluation program.

### Software Controls

There are several basic types of components within the main tabbed notebook. Each of these components represents a bit field contained within one or more HSP3824 control/status registers. The component types are:

### · Radio Button Groups

These components allow the user to make a single selection from a set of choices (typically from 2 to 16 selections).

### Decimal Numeric Fields

These components allow the user to specify a decimal number.

### Hexadecimal/Binary Numeric Fields

These components allow the user to specify either a hexadecimal or a binary number. The Evaluation Board software keeps the related field synchronized with the data entry field as data is being entered.

### Check Boxes

These components allow the user to make a Yes/No choice.

Components which are not valid or meaningful for a specific configuration are "dimmed-out" and cannot be selected.

Status fields are polled and updated approximately once per second.

Status (read-only) fields which are numeric in nature (i.e. the Signal Status page) have a green background. A numeric status field will not update if it has focus. To resume updating, move the focus to a different component.

### Configuration

This form (accessed by selecting the "Board Settings" option under the main menu choice "Configure") contains configuration options pertaining to the evaluation board as opposed to the HSP3824 itself. Be aware that the components on this form take place immediately (unlike changes to the "tabbed-notebook" which must be downloaded to take effect). These configuration options are:

### Communication Port

This configuration option allows the user to specify which communication (printer) port to use when downloading/ uploading the evaluation board.

### Reset

This radio button directly controls the reset pin on the HSP3824.

### • RX PE

This radio button directly controls the RX\_PE pin on the HSP3824. The RX\_PE signal enables the Rx operations.

### • TX PE

This radio button directly controls the TX\_PE pin on the HSP3824. The TX\_PE signal enables the transmit operations of the HSP3824. At the time that TX\_PE is asserted the HSP3824 will begin packet transmission starting with preamble and header transmission.

### Part Number

This configuration option will allow the user to specify the part number of the chip. Currently there is only one part number, so the user shouldn't need to modify this field.

The following components are available on the HSP3824 Rev. C Evaluation Board only:

### Board Selection

This configuration option allows the user to specify which board identifier to use when downloading/uploading the evaluation board. This allows the two boards to be connected without a 2-port switch.

### Data Mode

The Rev. C Evaluation Board is capable of generating a data stream that can be either packetized or continuous. This option allows the user to select the type of data stream to use. Rev. C has been designed to simplify packet performance evaluation (i.e. PER instead of only BER performance).

### · Packet Length

This configuration option along with the "Data Mode" option allows the user to specify the length of the packets generated by the evaluation board.

### Self Test Utility

The Evaluation Board software contains a simple self-test utility to test communication link availability and resiliency. To run the self-test, select "Self Test" under "Tools" on the main menu. The self test dialog box will appear which contains various communication link statistics. To begin the test, select "constant" or "increasing" and press the Start button. If the evaluation board is powered on and being clocked properly, the "Download Attempts," the "Registers Written" and the "Reads Required to Verify" data areas should start to increment.

Download failures are recorded in the list box at the bottom of the dialog box and in the "Download Failure Count" data area. A download has failed when four unsuccessful attempts have been made to download a specific control register and read back the value.

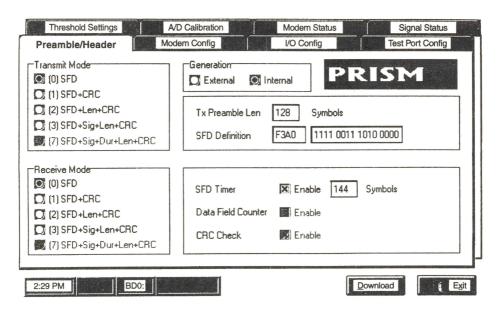
The section entitled "Reads Required to Verify" displays the number of reads required to verify that a register has been downloaded. Download failures do not contribute to the these statistics.

A "healthy" board/communication link should exhibit no download failures, a quickly increasing "Registers Written" and "Reads Required to Verify (1)" data area and an occasional "Reads Required to Verify (2)" data area increment.

### Detailed Description of the Contents of Each of the Tabbed Pages

The following paragraphs describe the content of each of the entries and status fields of the user SW pages. The corresponding HSP3824 Configuration Registers (CR) that are involved with each of the pages are also cross referenced. For a more detailed description of these registers, use the HSP3824 Datasheet.

### Preamble/Header Page



### Preamble Generation CR3<2:2>

This control bit is used to select the origination of the Preamble/Header information. The preamble and header can be either generated internally by the HSP3824 or from an external source.

### Transmit Mode CR0<4:3>

These control bits are used to select one of four Preamble Header modes for transmitting data.

CR0<4:3> Header Contents

00: SFD

01: SFD and CRC16

10: SFD, Length and CRC16

11: SFD, Signal, Service, Length and CRC16

### Receive Mode CR2<1:0>

These control bits are used to select one of four Preamble Header modes for receiving data.

CR2<1:0> Header Contents

00: SFD

01: SFD and CRC16

10: SFD, Length and CRC16

11: SFD, Signal, Service, Length and CRC16

### Transmit Preamble Length CR56<7:0>

This control register defines the Preamble length field value.

### Start Frame Delimiter Definition CR49<7:0> CR50<7:0>

These control registers contain the Start Frame Delimiter used for both the Transmit and Receive header.

### Start Frame Delimiter Timer Enable CR0<2:2>

This control bit is used to enable the Start Frame Delimiter timer. If the timer expires before the SFD has been detected, the HSP3824 returns to acquisition mode.

### Start Frame Delimiter Value CR41<7:0>

This control register contains the number of symbol periods for the demodulator to search for a SFD in a receive header before returning to acquisition mode.

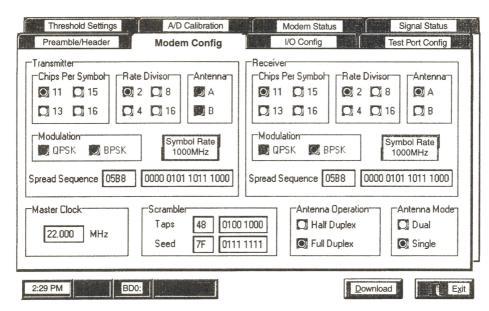
### Data Field Counter Enable CR0<1:1>

This control bit is used to enable/disable counting the number of data bits in the length field embedded in the header. The HSP3824 returns to acquisition mode at the end of the count. Only used in header modes 2 and 3.

### CRC Check Enable CR2<5:5>

This control bit is used to enable/disable the CRC16 check on the received Header.

### Modem Configuration Page



### TRANSMIT CONFIGURATION

### Chips per Symbol CR3<6:5>

These control bits are used to select the number of chips per symbol used in the I and Q transmit paths.

CR3<6:5> 00 01 10 11 Chips/Symbol 11 13 15 16

### Rate Divisor CR3<4:3>

These control bits are used to select the divide ratio required to achieve the required data rate.

CR3<4:3> 00 01 10 11 Divisor 2 4 8 16

### Antenna Select CR0<7:7>

This control bit is used to select the transmit antenna (half-duplex mode only).

### Modulation CR3<1:1>

This control bit is used to select the signal modulation type for the transmit packet.

### **Symbol Rate**

This indication-only field calculates the current transmit symbol rate. It is a function of the Master Clock, Modulation Type, Chips per Symbol and Rate Divisor.

### Spread Sequence CR13<7:0> CR14<7:0>

These control registers contain the spreading code for the I and Q transmit paths.

### RECEIVE CONFIGURATION

### Chips per Symbol CR2<7:6>

These control bits are used to select the number of chips per symbol used in the I and Q receive paths.

CR2<7:6> 00 01 10 11 Chips/Symbol 11 13 15 16

### Rate Divisor CR2<4:3>

These control bits are used to select the divide ratio required for the desired receive data rate.

CR2<4:3> 00 01 10 11 Divisor 2 4 8 16

### Antenna Select CR0<6:6>

This control bit is used to select the receive antenna (single antenna mode only).

### Modulation CR3<0:0>

This control bit is used to select the signal modulation type for the receive packet.

### Symbol Rate

This indication-only field calculates the current receive symbol rate. It is a function of the Master Clock, Modulation Type, Chips per Symbol and Rate Divisor.

### Spread Sequence CR20<7:0> CR21<7:0>

These control registers contain the despreading code for the I and Q receive paths.

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### **Master Clock**

This field allows the user to specify the clock being used to drive the HSP3824 chip. The clock is operator-entered and must be manually changed each time the signal generator frequency is changed. This value is used in formulas for displays that show frequency or time.

### Scrambler Taps CR16<6:0>

This control register contains the tap configuration for the transmit scrambler/receive descrambler.

### Scrambler Seed CR15<6:0>

This control register contains the seed value for the transmit scrambler/receive descrambler.

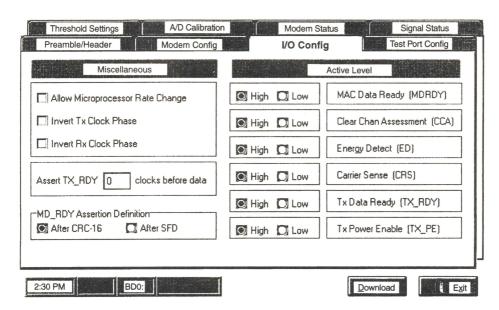
### Antenna Operation CR0<5:5>

This control bit is used to select between full duplex and half duplex operation.

### Antenna Mode CR2<2:2>

This control bit is used to select single or dual antenna mode

### I/O Configuration Page



### Allow Microprocessor Rate Change CR1<7:7>

This control bit is used to enable/disable constant data rates to the external processor that receives the demodulated data from the HSP3824. Rate changes from DBPSK to DQPSK within the same packet can be programmed to be transparent to the external processor.

### Invert Transmit Clock Phase CR9<0:0>

This control bit is used to select the phase of the transmit output clock.

### Assert TX RDY Clock Count CR1<6:2>

These control bits are used to define the number of clocks before the first data bit that TX\_RDY will be asserted.

### **Active Signal Levels**

These components allow the user to invert the sense of some signals.

### MAC Data Ready (MDRDY) CR9<6:6>

This control bit is used to select the active level of the MD RDY signal.

### Clear Channel Assessment (CCA) CR9<5:5>

This control bit is used to select the active level of the CCA signal.

### Energy Detect (ED) CR9<4:4>

This control bit is used to select the active level of the ED signal.

### Carrier Sense (CRS) CR9<3:3>

This control bit is used to select the active level of the CRS signal.

### Transmit Data Ready (TX\_RDY) CR9<2:2>

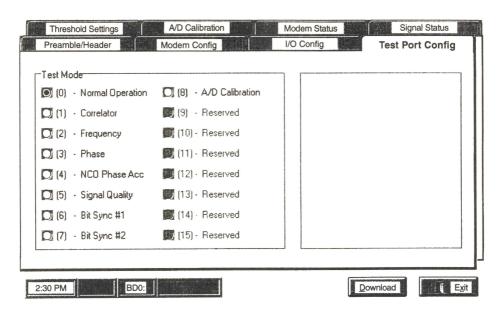
This control bit is used to select the active level of the TX\_RDY signal.

### Transmit Power Enable (TX\_PE) CR9<1:1>

This control bit is used to select the active level of the TX\_PE signal.

### **Application Note 9615**

### **Test Port Configuration Page**



### Test Mode CR4<7:0>

The HSP3824 provides the capability to access a number of internal signals and/or data through the test port pins TEST 0-7 and TEST\_CLK.

### (0) Normal Operation Mode

- <7:7> Carrier Sense (CRS)
- <6:6> Energy Detect (ED)
- <5:3> Reserved
- <2:2> Initial Detect
- <1:0> Reserved
- TEST\_CLK Internal TX Clock

### (1) Correlator Test Mode

<7:0> Correlator Magnitude

TEST\_CLK Internal TX Clock (TX chip rate)

### (2) Frequency Test Mode

<7:0> Frequency offset Register

TEST\_CLK Subsample Clock (Rx symbol rate)

### (3) Phase Test Mode

<7:0> Phase

TEST\_CLK Subsample Clock (Rx symbol rate)

### (4) NCO Test Mode

<7:0> Phase Accum Register (8 most significant bits)

TEST\_CLK Subsample Clock (Rx symbol rate)

### (5) SQ Test Mode

<7:0> SQ Phase Variance (8 most significant bits)

TEST\_CLK Load Signal Quality Signal

### (6) Bit Sync Test Mode 1

<7:0> Bit Sync Accum

TEST\_CLK Internal RX Clock

### (7) Bit Sync Test Mode 2

<7:0> SQ Bit Sync Reference Data (8 most significant bits) TEST\_CLK Load SQ Signal

### (8) A/D Cal Test Mode

<7:7> Carrier Sense (CRS)

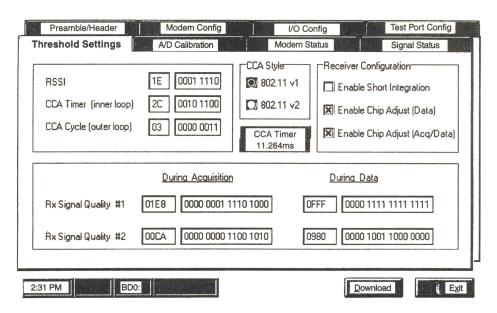
<6:6> Energy Detect (ED)

<5:5> Reserved

<4:0> A/D Calibrate

TEST\_CLK Internal RX Clock

### Threshold Settings Page



### Received Signal Strength Indication (RSSI) CR19<5:0>

These control bits are used to specify the RSSI threshold for measuring and generating the energy detect (ED) signal. When RSSI exceeds this threshold, ED is declared.

### Clear Channel Assessment Timer CR17<7:0>

This control register is used to configure the period of the time-out threshold of the CCA watchdog timer.

### Clear Channel Assessment Cycle CR18<7:0>

This control register is used to configure how many times the CCA timer is allowed to reach its maximum count before it declares that the channel is clear (independent of the actual energy measured in the channel).

### Enable 1/4 Chip Adjust During Acquisition/Data CR5<6:6>

This control bit is used to enable/disable 1/4 chip timing adjustments during acquisition or data.

### **Actual Clear Channel Assessment Time**

This indication-only field calculates the actual Clear Channel Assessment Time Out interval (the inner loop).

### Receive Bit Sync Amplitude (Acquisition/Data) CR22<7:0> CR23<7:0>

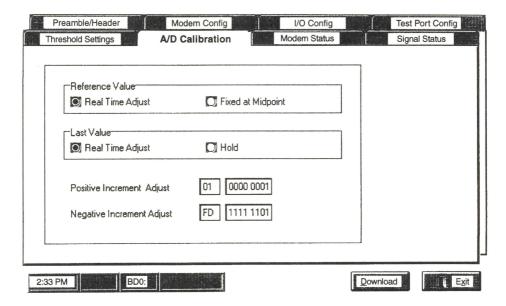
These control registers are used to specify the bit sync amplitude quality threshold used for acquisition and for data. See typical values in the HSP3824 Datasheet.

### Receive Phase Variance (Acquisition/Data) CR30<7:0> CR31<7:0>

These control registers are used to specify the phase variance quality threshold used for acquisition and for data. See typical values in the HSP3824 Datasheet.

### **Application Note 9615**

### A/D Calibration Page



### Reference Value CR1<1:1>

This control bit is used to select whether internal A/D calibration circuit is active or not and if not, sets the reference to mid-scale.

### Last Value CR1<0:0>

This control bit is used to select whether internal A/D calibration circuit is held at its most recent value.

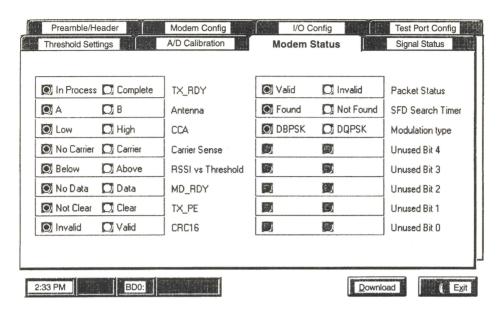
### Positive Increment Adjust CR11<7:0>

This control register contains the value used for positive increments of the level adjusting circuit of the A/D reference. These positive increment steps define how fast the A/D will be driven to saturation.

### Negative Increment Adjust CR12<7:0>

This control register contains the value used for negative increments of the level-adjusting circuit of the A/D reference. These negative increments define the back off step size from when the A/D reaches saturation.

### Modem Status Page



### Transmit Ready (TX\_RDY) CR7<7:7>

This status bit indicates the status of the TX\_RDY output pin. It is only used when the Preamble/Header is generated internally within the HSP3824.

### Antenna CR7<6:6>

This status bit indicates the antenna selected by the device (status of the ANTSEL pin).

### Clear Channel Assessment (CCA) CR7<5:5>

This status bit indicates the status of the Clear Channel Assessment output pin.

### Carrier Sense (CRS) CR7<4:4>

This status bit indicates the status of Carrier Sense (or PN lock).

### RSSI vs Threshold CR7<3:3>

This status bit indicates whether the RSSI signal is above or below threshold (or energy detect (ED)).

### MAC Data Ready (MD\_RDY) CR7<2:2>

This status bit indicates the status of the MD\_RDY output pin. It signals that a valid Preamble/Header has been received and that the next available bit on the RXD bus will be the first data packet bit.

### Transmit Power Enable (TX\_PE) CR7<1:1>

This status bit indicates whether the external device has acknowledged that the channel is clear for transmission (or status of the TX\_PE pin).

### Valid CRC16 CR7<0:0>

This status bit indicates whether a valid CRC16 has been calculated for the Header information. The CRC16 does not cover the preamble bits.

### Packet Status CR8<7:7>

This status bit indicates whether a valid packet has been received. This is meaningful only when the device operates under the full protocol mode.

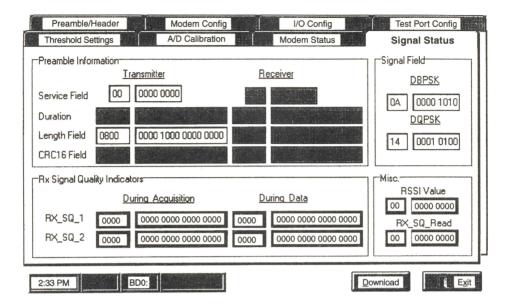
### Start Frame Delimiter Search Timer CR8<6:6>

This status bit indicates the status of the SFD search timer.

### Modulation Type CR8<5:5>

This status bit indicates the modulation type for the data packet. Preamble and Header data are always DBPSK, but the data can be either DBPSK or DQPSK.

### Signal Status Page



### TRANSMIT PREAMBLE INFORMATION

### Service Field CR51<7:0>

This control register contains the value of the service field to be transmitted in a Header.

### Length Field CR52<7:0> CR53<7:0>

These control registers contain the value of the length field to be transmitted. It indicates the number of bits transmitted in the data packet.

### CRC16 Field CR54<7:0> CR55<7:0>

These status registers indicate the calculated CRC16 for the transmitted header.

### RECEIVE PREAMBLE INFORMATION

### Service Field CR44<7:0>

This status register contains the value of the service field received in a Header.

### Length Field CR45<7:0> CR46<7:0>

These status registers contain the value of the length field of the received packet. It indicates the number of bits transmitted in the data packet.

### CRC16 Field CR47<7:0> CR48<7:0>

These status registers indicate the received CRC16 for the received header.

### SIGNAL FIELD

### BPSK CR42<7:0>

This control register contains the 8-bit value indicating that the data packet modulation is DBPSK.

### QPSK CR43<7:0>

This control register contains the 8-bit value indicating that the data packet modulation is DQPSK.

### **RECEIVE SIGNAL QUALITY INDICATORS**

### Bit Sync Amplitude Acquisition CR24<6:0> CR25<7:0>

These status registers contain the measured bit sync amplitude signal quality during acquisition.

### Bit Sync Amplitude Data CR28<6:0> CR29<7:0>

These status registers contain the measured bit sync amplitude signal quality during data tracking.

### Phase Variance Acquisition CR32<7:0> CR33<7:0>

These status registers contain the measured phase variance signal quality during acquisition.

### Phase Variance Data CR36<7:0> CR37<7:0>

These status registers contain the measured phase variance signal quality during data tracking.

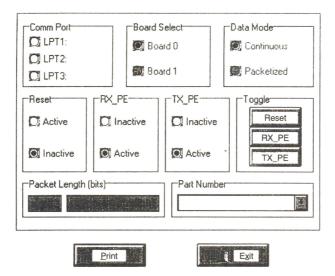
### RSSI Value CR10<5:0>

These status bits contain the value of the RSSI analog input signal from the on-chip ADC. This register is updated at the chip rate divided by 11.

### Receive Signal Quality for Best Antenna Dwell CR38<7:0>

This status register contains the bit sync amplitude signal quality measurement derived from the Bit Sync signal quality stored in the CR28-29 registers of the HSP3824. This value is the result of the signal quality measurement for the best antenna dwell in the antenna diversity mode.

## Configuration Dialog Box



The configuration dialog box is called up by choosing the "Board Settings" menu item under the "Configure" main menu choice. This form contains options pertaining to the evaluation board. Changes made on this form take place immediately (unlike changes to the "tabbed-notebook" which must be downloaded to take effect.

The common configuration options are:

#### **Communication Port**

This configuration option allows the user to specify which communication (printer) port to use when downloading/uploading the evaluation board.

#### Reset

This radio button directly controls the reset pin on the HSP3824 chip.

#### RX PE

This radio button directly controls the RX\_PE pin on the HSP3824 chip.

#### TX\_PE

This radio button directly controls the TX\_PE pin on the HSP3824 chip.

#### Part Number

This configuration option will allow the user to specify the part number of the chip. Currently, there is only one part number, so the user shouldn't need to modify this field.

The following options apply to the Rev. C Evaluation Board only:

#### Board Selection

This configuration option allows the user to specify which board identifier to use when downloading/uploading the evaluation board.

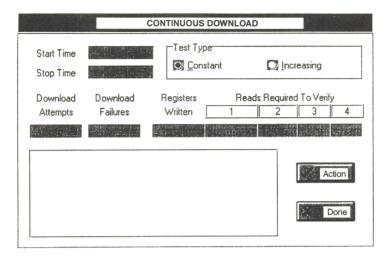
#### Data Mode

The Rev. C evaluation board is capable of generating a data stream that can be packetized or continuous. This option allows the user to select the type of data stream to use.

#### **Packet Length**

This configuration option along with the "Data Mode" option allows the user to specify the length of the packets generated by the evaluation board.

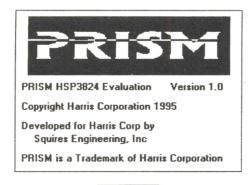
### Self Test Utility



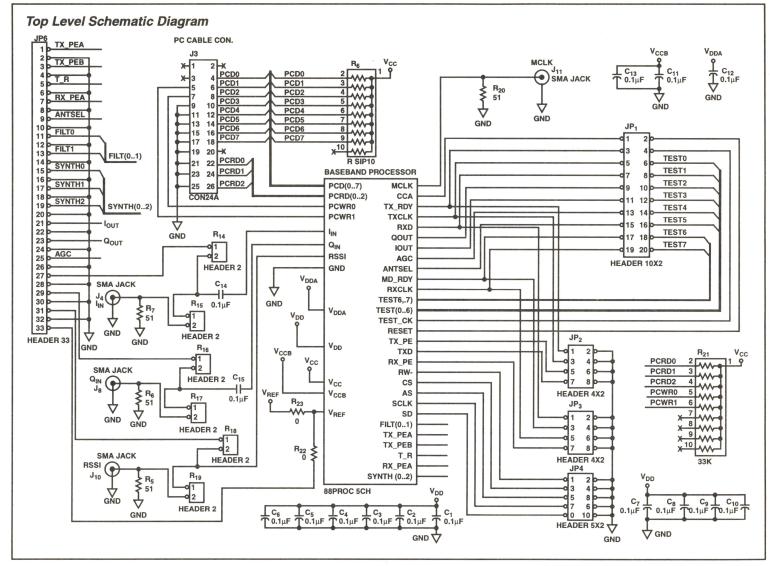
The self test utility provides the capability to perform continuous configuration register downloads. This tests communication link availability and resiliency. To run the self-test, select "Self Test" under "Tools: on the main menu. To begin the test, select "constant" or "increasing" and press the Start button. If the evaluation board is powered and being clocked properly, the "Download Attempts", "Registers Written" and "Reads Required to Verify" data areas should start to increment.

Download failures are recorded in the list box at the bottom of the dialog box and in the "Download Failure Count" data area. A download is considered to have failed when four unsuccessful attempts have been made to download a specific control register and read back the value.

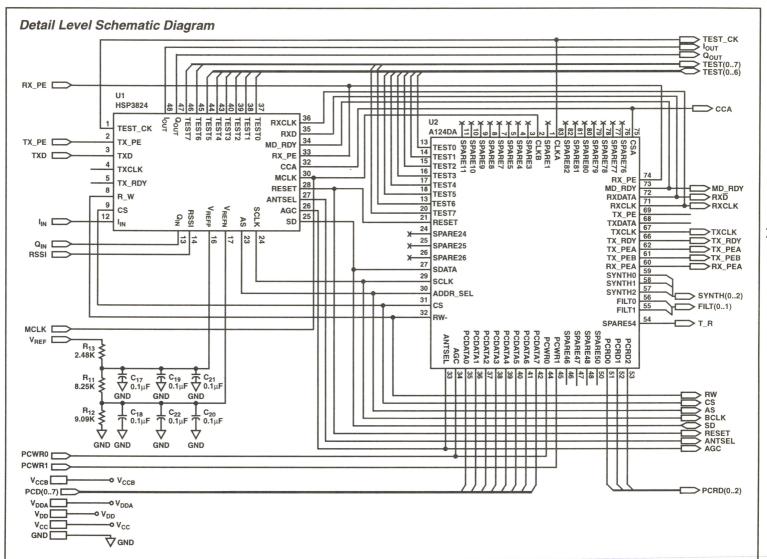
A healthy board/communication link should exhibit no download failures, a quickly increasing "Registers Written" and "Read Required to Verify(1)" data areas and an occasional "Reads Required to Verify(2)" data area increment.



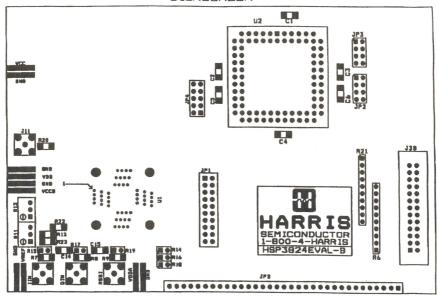




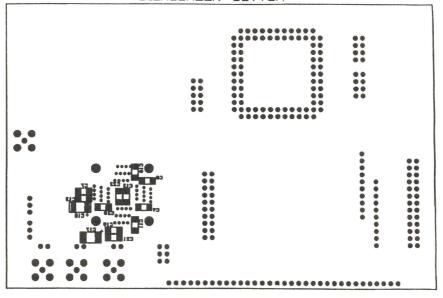
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## SILKSCREEN



## SILKSCREEN BOTTOM





No. AN9616 August 1996

## Harris Wireless Products

## **Programming the HSP3824**

Author: John Fakatselis



#### Introduction

This application note serves as a firmware designers manual for the PRISM™ HSP3824 baseband processor. The note

groups the programmable registers and their bit content by function. This note can serve as a quick reference for code development and system test and modification by function.

#### SW Overview

The HSP3824 offers flexibility for various system configurations through its programmable features. Among other the user has many options to control synchronization time, link protocol formats, data rates, performance thresholds, and visibility to internal modem parameters and status.

#### Preamble/Header

These configuration registers include preamble generation, transmit header modes and receive header modes. Preamble and header can be either generated internally from the HSP3824 or can be received from an external source i.e. a network processor.

#### **Modem Configuration**

These configuration registers include configuration for transmitter and receiver modem. The transmit and receive symbol rates, scrambler configuration, PN code configuration and antenna selection are also programmed through these registers.

#### I/O Configuration

These configuration registers include configuration of active signal levels (polarity) of HSP3824 I/O signals and set up of other miscellaneous I/O signal parameters. This is to provide flexibility and minimize glue logic to external circuits if there is a signal polarity issue.

#### **Test Port Configuration**

These configuration registers include configuration for selection of internal HSP3824 signals and/or data to become available at the Test Port pins. These signals can be useful during debugging, regulatory compliance testing as well as to design enhanced external algorithms to improve overall radio performance.

#### **Threshold Settings**

These configuration registers include a number of configurable threshold settings. They cover, Received Signal Strength Indication and Clear Channel Assessment threshold parameters, as well as, received signal quality thresholds used during acquisition and data tracking. By setting these acquisition and tracking thresholds, the user can define the desired modem performance i.e. set the probability of detection vs. the probability of false alarm ratio.

#### A/D Calibration

These configuration registers include configuration data to activate the A/D level adjustment circuit of the HSP3824. This circuit is designed to maximize utilization of the A/D dynamic range. This programmable circuit tries to keep the A/Ds close to saturation.

#### **Modem Status**

These configuration registers include information that represent both control and status registers (read-only). The status components indicate the real time state of the modem operation.

#### **Signal Status**

These configuration registers include information that represent modem parameter (read-only) registers. These modem status components are updated real time. They can be used to design external SW or HW algorithms to improve overall modem performance. In addition this set of registers provide information on the link protocol (header) that is presently in use.

# Description of Configuration Register Assignments by Function.

The following paragraphs describe the configuration register (CR) content of the programmable HSP3824 registers. The bits within the CR that define the particular function or data are also indicated. The CR description and references below are broken by the primary HSP3824 programmable functional groups which are:

- · Preamble/ header.
- · Modem configuration
- · I/O configuration
- · Test Port configuration
- · Threshold settings
- A/D calibration
- · Modem status
- · Signal status

This can serve as a quick reference to program or to modify registers by function. Refer also to the HSP3824 data sheet for description of the hardware algorithms at its appropriate sections. An example of a default set up is also attached to this note.

#### Preamble/Header

#### Preamble Generation CR3<2:2>

This control bit is used to select the origination of the Preamble/Header information. The preamble and header can be either generated internally by the HSP3824 or from an external source.

#### Transmit Mode CR0<4:3>

These control bits are used to select one of the four Preamble Header modes for transmitting data. The four modes contain different combinations of fields.

CR0<4:3> Header Contents

- 00 SFD, field
- 01 SFD and CRC16, fields
- 10 SFD, Length and CRC16, fields
- 11 SFD, Signal, Length and CRC16, fields

#### Receive Mode CR2<1:0>

These control bits are used to select one of four Preamble Header modes for receiving data.

CR2<1:0> Header Contents

- 00 SFD
- 01 SFD and CRC16
- 10 SFD, Length and CRC16
- 11 SFD, Signal, Length and CRC16

#### Transmit Preamble Length CR56<7:0>

This control register defines the Preamble length field value.

#### Start Frame Delimiter Definition CR49<7:0> CR50<7:0>

These control registers contain the Start Frame Delimiter used for both the Transmit and Receive header. This field is the address field for each individual receiver within the network.

#### Start Frame Delimiter Timer Enable CR0<2:2>

This control bit is used to enable the Start Frame Delimiter timer. If the timer expires before the SFD has been detected, the HSP3824 returns to acquisition mode. The search time is defined by the start frame delimiter value registers.

#### Start Frame Delimiter Value CR41<7:0>

This control register contains the number of symbol periods for the demodulator to search for a SFD in a receive header before returning to acquisition mode.

#### Data Field Counter Enable CR0<1:1>

This control bit is used to enable/disable counting the number of data bits in the length field embedded in the header. The HSP3824 returns to acquisition mode at the end of the count as defined by the "Length" field of the header. This can only be used in header modes 2 and 3.

#### CRC Check Enable CR2<5:5>

This control bit is used to enable/disable the CRC16 check on the received Header.

## **Modem Configuration**

#### TRANSMIT CONFIGURATION

#### Chips per Symbol CR3<6:5>

These control bits are used to select the number of chips per symbol used in the I and Q transmit paths.

CR3<6:5>	00	01	10	11
Chips/Symbol	11	13	15	16

#### Rate Divisor CR3<4:3>

These control bits are used to select the divide ratio required to achieve the required data rate (refer to the HSP3824 data sheet).

CR3<4:3>	00	01	10	11
Divisor	2	4	8	16

#### Antenna Select CR0<7:7>

This control bit is used to select the transmit antenna (half-duplex mode only).

#### Modulation CR3<1:1>

This control bit is used to select the signal modulation type for the transmit packet.

#### Spread Sequence CR13<7:0> CR14<7:0>

These control registers contain the spreading code for the I and Q transmit paths.

#### RECEIVE CONFIGURATION

#### Chips per Symbol CR2<7:6>

These control bits are used to select the number of chips per symbol used in the I and Q receive paths.

CR2<7:6> 00 01 10 11 Chips/Symbol 11 13 15 16

#### Rate Divisor CR2<4:3>

These control bits are used to select the divide ratio required for the desired receive data rate.

CR2<4:3> 00 01 10 11 Divisor 2 4 8 16

#### Antenna Select CR0<6:6>

This control bit is used to select the receive antenna (single antenna mode only).

#### Modulation CR3<0:0>

This control bit is used to select the signal modulation type for the receive packet.

#### Spread Sequence CR20<7:0> CR21<7:0>

These control registers contain the despreading code for the I and Q receive paths.

#### Scrambler Taps CR16<6:0>

This control register contains the tap configuration for the transmit scrambler / receive descrambler.

#### Scrambler Seed CR15<6:0>

This control register contains the seed value for the transmit scrambler / receive descrambler.

#### Antenna Operation CR0<5:5>

This control bit is used to select between full duplex and half duplex operation.

#### Antenna Mode CR2<2:2>

This control bit is used to select single or dual antenna mode.

## I/O Configuration

#### Allow Microprocessor Rate Change CR1<7:7>

This control bit is used to enable/disable constant data rates to the external processor that receives the demodulated data from the HSP3824. Rate changes from DBPSK to DQPSK within the same packet can be programmed to be transparent to the external processor.

#### Invert Transmit Clock Phase CR9<0:0>

This control bit is used to select the phase of the transmit output clock.

#### Assert TX\_RDY Clock Count CR1<6:2>

These control bits are used to define the number of clocks before the first data bit that TX\_RDY will be asserted.

#### **ACTIVE SIGNAL LEVELS**

These components allow the user to invert the sense of certain signals available as pins on the HSP3824.

#### MAC Data Ready (MD RDY) CR9<6:6>

This control bit is used to select the active level of the MD RDY signal.

#### Clear Channel Assessment (CCA) CR9<5:5>

This control bit is used to select the active level of the CCA signal.

#### Energy Detect (ED) CR9<4:4>

This control bit is used to select the active level of the ED signal.

#### Carrier Sense (CRS) CR9<3:3>

This control bit is used to select the active level of the CRS signal.

#### Transmit Data Ready (TX\_RDY) CR9<2:2>

This control bit is used to select the active level of the TX\_RDY signal.

#### Transmit Power Enable (TX\_PE) CR9<1:1>

This control bit is used to select the active level of the TX\_PE signal.

## Test Port Configuration

#### Test Mode CR4<7:0>

The HSP3824 provides the capability to access a number of internal signals and/or data through the test port pins TEST 0-7 and TEST\_CLK. The TEST\_CLK is selected given the data that is clocked out from TEST 0-7 port. TX\_CLK is intended to be used to clock the TEST 0-7 data from the HSP3824.

#### (0) Normal Operation Mode

<7:7> Carrier Sense (CRS)

<6:6> Energy Detect (ED)

<5:3> Reserved

<2:2> Initial Detect

<1:0> Reserved

TEST CLK Internal TX Clock (TX chip rate)

#### (1) Correlator Test Mode

<7:0> Correlator Magnitude (PN correlator)

TEST\_CLK Internal TX Clock (TX chip rate)

#### (2) Frequency Test Mode

<7:0> Frequency offset Register

TEST\_CLK Subsample Clock (Rx symbol rate)

#### (3) Phase Test Mode

<7:0> Phase (instantenous I,Q)

TEST\_CLK Subsample Clock (Rx symbol rate)

#### (4) NCO Test Mode

<7:0> Phase Accum Register (8 most significant bits)

TEST\_CLK Subsample Clock (Rx symbol rate)

#### (5) SQ Test Mode

<7:0> Signal Quality (SQ) Phase Variance (8 most significant bits)

TEST CLK Load Signal Quality Signal

#### (6) Bit Sync Test Mode 1

<7:0> Bit Sync Accum

TEST\_CLK Internal RX Clock

#### (7) Bit Sync Test Mode 2

<7:0> SQ Bit Sync Reference Data (8 most significant bits)
TEST CLK Load SQ Signal

#### (8) A/D Cal Test Mode

<7:7> Carrier Sense (CRS)

<6:6> Energy Detect (ED)

<5:5> Reserved

<4:0> A/D Calibrate

TEST CLK (Internal RX Clock)

## Threshold Settings

#### Received Signal Strength Indication (RSSI) CR19<5:0>

These control bits are used to specify the RSSI threshold for measuring and generating the energy detect (ED) signal. When RSSI exceeds this threshold. ED is declared.

#### Clear Channel Assessment Timer CR17<7:0>

This control register is used to configure the period of the time-out threshold of the CCA watchdog timer.

#### Clear Channel Assessment Cycle CR18<7:0>

This control register is used to configure how many times the CCA timer is allowed to reach its maximum count before it declares that the channel is clear (independent of the actual energy measured in the channel).

## Enable 1/4 Chip Adjust During Acquisition/Data CR5<6:6>

This control bit is used to enable/disable 1/4 chip timing adjustments during acquisition or data. The default is 1/2 chip adjustments.

# Receive Bit Synch Amplitude (Acquisition/Data) CR22<7:0> CR23<7:0>

These control registers are used to specify the bit synch amplitude quality threshold used for acquisition and for data. See typical values in the HSP3824 data sheet. The received

signal must be above this programmable value to be declared valid.

# Receive Phase Variance (Acquisition/Data) CR30<7:0> CR31<7:0>

These control registers are used to specify the phase variance quality threshold used for acquisition and for data. See typical values in the HSP3824 data sheet. The received signals phase variance has to be less than this programmable value to be declared as valid signal.

#### A/D Calibration

#### Reference Value CR1<1:1>

This control bit is used to select whether internal A/D calibration circuit is active or not and if not, sets the reference to mid-scale.

#### Last Value CR1<0:0>

This control bit is used to select whether internal A/D calibration circuit is held at its most recent value.

#### Positive Increment Adjust CR11<7:0>

This control register contains the value used for positive increments of the level adjusting circuit of the A/D reference. These positive increment steps define how fast the A/D will be driven to saturation.

#### Negative Increment Adjust CR12<7:0>

This control register contains the value used for negative increments of the level-adjusting circuit of the A/D reference. These negative increments define the back off step size from when the A/D reaches saturation.

#### Modem Status

#### Transmit Ready (TX\_RDY) CR7<7:7>

This status bit indicates the status of the TX\_RDY output pin. It is only used when the Preamble/Header is generated internally within the HSP3824.

#### Antenna CR7<6:6>

This status bit indicates the antenna selected by the device (status of the ANTSEL pin) during antenna diversity.

#### Clear Channel Assessment (CCA) CR7<5:5>

This status bit indicates the status of the Clear Channel Assessment output pin.

#### Carrier Sense (CRS) CR7<4:4>

This status bit indicates the status of Carrier Sense (or PN lock).

#### RSSI vs. Threshold CR7<3:3>

This status bit indicates whether the RSSI signal is above or below threshold (or energy detect (ED)).

#### MAC Data Ready (MD\_RDY) CR7<2:2>

This status bit indicates the status of the MD\_RDY output pin. It signals that a valid Preamble/Header has been received and that the next available bit on the RXD bus will be the first data packet bit.

#### Transmit Power Enable (TX\_PE) CR7<1:1>

This status bit indicates whether the external device has acknowledged that the channel is clear for transmission (or status of the TX PE pin).

#### Valid CRC16 CR7<0:0>

This status bit indicates whether a valid CRC16 has been calculated for the Header information. The CRC16 does not cover the preamble bits or the data packet.

#### Packet Status CR8<7:7>

This status bit indicates whether a valid packet has been received. This is meaningful only when the device operates under the full protocol (mode 3).

#### Start Frame Delimiter Search Timer CR8<6:6>

This status bit indicates the status of the SFD search timer.

#### Modulation Type CR8<5:5>

This status bit indicates the modulation type for the data packet. Preamble and Header data are always at 1MBPS.

#### Signal Status

## TRANSMIT PREAMBLE INFORMATION

Service Field CR51<7:0>

This control register contains the value of the service field to be transmitted in a Header.

#### Length Field CR52<7:0> CR53<7:0>

These control registers contain the value of the length field to be transmitted. It indicates the number of bits transmitted in the data packet.

#### CRC16 Field CR54<7:0> CR55<7:0>

These status registers indicate the calculated CRC16 for the transmitted header.

#### RECEIVE PREAMBLE INFORMATION

#### Service Field CR44<7:0>

This status register contains the value of the service field received in a Header.

#### Length Field CR45<7:0> CR46<7:0>

These status registers contain the value of the length field of the received packet. It indicates the number of bits transmitted in the data packet.

#### CRC16 Field CR47<7:0> CR48<7:0>

These status registers indicate the received CRC16 for the received header.

#### SIGNAL FIELD

#### BPSK CR42<7:0>

This control register contains the 8-bit value indicating that the data packet modulation is DBPSK.

#### QPSK CR43<7:0>

This control register contains the 8-bit value indicating that the data packet modulation is DQPSK.

#### RECEIVE SIGNAL QUALITY INDICATORS

#### Bit Synch Amplitude Acquisition CR24<6:0> CR25<7:0>

These status registers contain the measured bit synch amplitude signal quality during acquisition.

#### Bit Synch Amplitude Data CR28<6:0> CR29<7:0>

These status registers contain the measured bit synch amplitude signal quality during data tracking.

#### Phase Variance Acquisition CR32<7:0> CR33<7:0>

These status registers contain the measured phase variance signal quality during acquisition.

#### Phase Variance Data CR36<7:0> CR37<7:0>

These status registers contain the measured phase variance signal quality during data tracking.

#### RSSI Value CR10<5:0>

These status bits contain the value of the RSSI analog input signal from the on-chip ADC. This register is updated at the chip rate divided by 11.

## Receive Signal Quality for Best Antenna Dwell CR38<7:0>

This status register contains the bit synch amplitude signal quality measurement derived from the Bit Synch signal quality stored in the CR28-29 registers of the HSP3824. This value is the result of the signal quality measurement for the best antenna dwell in the antenna diversity mode.

#### **DEFAULT CONFIGURATION**

Table 1 contains a set of default configuration values that can be used for QPSK and BPJK modulation. These values can be initially used for systems test and then modified as appropriate, per each application. The default configuration table is followed by the detail description of all the available registers of the HSP3824.

TABLE 1. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION

REGISTER	NAME	TYPE	REG ADDR IN HEX	QPSK	BPSK
CR0	MODEM CONFIG. REG A	R/W	00	3C	64
CR1	MODEM CONFIG. REG B	R/W	04	00	00
CR2	MODEM CONFIG. REG C	R/W	08	07	24
CR3	MODEM CONFIG. REG D	R/W	0C	04	07
CR4	INTERNAL TEST REGISTER A	R/W	10	00	00
CR5	INTERNAL TEST REGISTER B	R/W	14	00	00
CR6	INTERNAL TEST REGISTER C	R	18	Х	Х
CR7	MODEM STATUS REGISTER A	R	1C	×	Х
CR8	MODEM STATUS REGISTER B	R	20	Х	. х
CR9	I/O DEFINITION REGISTER	R/W	24	00	00
CR10	RSSI VALUESTATUS REGISTER	R	28	Х	Х
CR11	ADC_CAL_POS REGISTER	R/W	2C	01	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD	FD
CR13	TX_SPREAD SEQUENCE(HIGH)	R/W	34	05	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8	В8
CR15	SCRAMBLE_SEED	R/W	3C	7F	7F
CR16	SCRAMBLE_TAP (RX AND TX)	R/W	40	48	48
CR17	CCA_TIMER_TH	R/W	44	2C	2C
CR18	CCA_CYCLE_TH	R/W	48	03	03
CR19	RSSI_TH	R/W	4C	1E	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05	05
CR21	RX_SREAD SEQUENCE (LOW)	R/W	54	B8	B8
CR22	RX_SQ1_ IN_ACQ (HIGH) THRESHOLD	R/W	58	01	01
CR23	RX-SQ1_ IN_ACQ (LOW) THRESHOLD	R/W	5C	E8	E8
CR24	RX-SQ1_ OUT_ACQ (HIGH) READ	R	60	Х	х
CR25	RX-SQ1_ OUT_ACQ (LOW) READ	R	64	Х	Х
CR26	RX-SQ1_ IN_DATA (HIGH) THRESHOLD	R/W	68	0F	0F
CR27	RX-SQ1-SQ1_ IN_DATA (LOW) THRESHOLD	R/W	6C	FF	FF
CR28	RX-SQ1_ OUT_DATA (HIGH)READ	R	70	Х	Х
CR29	RX-SQ1_ OUT_DATA (LOW) READ	R	74	Х	Х
CR30	RX-SQ2_ IN_ACQ (HIGH) THRESHOLD	R/W	78	00	00

TABLE 1. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION (Continued)

REGISTER	NAME	TYPE	REG ADDR IN HEX	QPSK	BPSK
CR31	RX-SQ2- IN-ACQ (LOW) THRESHOLD	R/W	7C	CA	CA
CR32	RX-SQ2_ OUT_ACQ (HIGH) READ	R	80	Х	×
CR33	RX-SQ2_ OUT_ACQ (LOW) READ	R	84	X	х
CR34	RX-SQ2_IN_DATA (HIGH)THRESHOLD	R/W	88	09	09
CR35	RX-SQ2_ IN_DATA (LOW) THRESHOLD	R/W	8C	80	80
CR36	RX-SQ2_OUT_DATA (HIGH) READ	R	90	Х	Х
CR37	RX-SQ2_OUT_DATA (LOW) READ	R	94	Х	Х
CR38	RX_SQ_READ; FULL PROTOCOL	R	98	Х	Х
CR39	RESERVED	W	9C	00	00
CR40	RESERVED	W	A0	00	00
CR41	UW_Time Out_LENGTH	R/W	A4	90	90
CR42	SIG_DBPSK Field	R/W	A8	0A	0A
CR43	SIG_DQPSK Field	R/W	AC	14	14
CR44	RX_SER_Field	R	В0	Х	х
CR45	RX_LEN Field (HIGH)	R	B4	Х	X
CR46	RX_LEN Field (LOW)	R	B8	Х	Х
CR47	RX_CRC16 (HIGH)	R	BC	Х	Х
CR48	RX_CRC16 (LOW)	R	C0	Х	х
CR49	UW -(HIGH)	R/W	C4	F3	F3
CR50	UW_(LOW)	R/W	C8	A0	A0
CR51	TX_SER_F	R/W	СС	00	00
CR52	TX_LEN (HIGH)	R/W	D0	FF	FF ,
CR53	TX_LEN(LOW)	R/W	D4	FF	FF
CR54	TX_CRC16 (HIGH)	R	D8	Х	х
CR55	TX_CRC16 (LOW)	R	DC	Х	х
CR56	TX_PREM_LEN	R/W	E0	80	80

## Control Registers, Address and Bit Location Specification

The following tables describe the function of each control register along with the associated bits in each control register.

#### CONFIGURATION REGISTER 0 ADDRESS (0h) MODEM CONFIGURATION REGISTER A

Bit 7	Log	This bit selects the transmit antenna, controlling the output ANT_SEL pin. It is only used in half duplex mode. (Bit 5 = 0) Logic 1 = Antenna A. Logic 0 = Antenna B.					
Bit 6	Log	In single antenna operation this bit is used as the output of the ANT_SEL pin. In dual antenna mode this bit is ignored.  Logic 1 = Antenna A.  Logic 0 = Antenna B.					
Bit 5	AN ina Log	This control bit is used to select between full duplex and half duplex operation. If set for full duplex operation, the ANT_SEL pin reflects the setting of CR0 bit 7 when TX_PE is active and reflects the receiver's choice when TX_PE is inactive. In full duplex operation, the ANT_SEL pin always reflects the receiver's choice antenna.  Logic 1 = full duplex.  Logic 0 = half duplex.					
Bit 4, 3	and	l header are [	DBPSK for all	modes of ope	the four input Preamble Header modes for transmitting data. The preamble eration. Mode 0 is followed by DBPSK data. For modes 1-3, the data can This is a "don't care" if the header is generated externally.		
		MODE BIT 4 BIT 3 MODE DESCRIPTION					
		0	0	0	Preamble with SFD Field.		
		1	0	1	Preamble with SFD, and CRC16.		
		2	1	0	Preamble with SFD, Length, and CRC16.		
		3	1	1	Full preamble and header.		
Bit 2	This control bit is used to enable the SFD (Start Frame Delimiter) timer. If the time is set and expires before the SFD has been detected, the HSP3824 will return to its acquisition mode.  Logic 1: Enables the SFD timer to start counting once the PN acquisition has been achieved.  Logic 0: Disables the SFD Timer.						
Bit 1	This control bit enables counting the number of data bits per the length field embedded in the header. Only used in header modes 2 and 3. Then according to the count it returns the processor into its acquisition mode at the end of the count. If length field is 0000h, modern will reset at end of SFD regardless of this bit setting.  Logic 1 = Enable Length Time Out.  Logic 0 = Disabled.						
Bit 0	Uni	used don't car	re.				
		NECUDATI	ON DECICE		SS (04h) MODEM CONFIGURATION REGISTER B		

#### CONFIGURATION REGISTER 1 ADDRESS (04h) MODEM CONFIGURATION REGISTER B

Bit 7	When active this bit maintains the RXCLK and TXLK rates constant for preamble and data transfers even if the data is modulated in DQPSK. This bit is used if the external processor can not accommodate rate changes. This is an active high signal. The rate used is the QPSK rate and the BPSK header bits are double clocked.
Bit 6, 5, 4, 3, 2	These control bits are used to define a binary count (N) from 0 - 31. This count is used to assert TX_RDY N - clocks (TXCLK) before the beginning of the first data bit. If this is set to zero, then the TX_RDY will be asserted immediately after the last bit of the Preamble Header.
Bit 1	When active the internal A/D calibration circuit sets the reference to mid-scale. When inactive then the calibration circuit adjusts the reference voltage in real time to optimize I, Q levels.  Logic 1 = Reference set at mid-scale (fixed).  Logic 0 = Real time reference adjustment.
Bit 0	When active the A/D calibration circuit is held at its last value.  Logic 1 = Reference held at the most recent value.  Logic 0 = Real time reference level adjustment.

Bit 7, 6	These control bits a filter correlators (se	are used to select the num ee table below).	nber of chips per s	ymbol used	in the I and Q paths of the	e receiver matche
		CHIPS PER SYMBO	L BIT 7	7	BIT 6	
		11	0		0	
		13	0		1	
		15	1		0	
		16	1		1	
Bit 5	and any packet error the carrier is lost or times out. Logic 1 = Disable ror Logic 0 = Enable ror These control bits determined by the	sed to disable the CRC16 or checks have to be deter the network processor receiver error checks. eceiver checks.  are used to select the div following equation:  LLK/(N x Chips per symbol.)	ected externally. T esets the device to device to	he HSP3824 the acquisi	4 will remain in the receivition mode, or if, in mode	re mode until eithe s 2 or 3, the lengt
		MASTER CLOCK/N		4	BIT 3	* 1
		N = 2	0		0	
		N = 4	0		1	
		N = 8	1		0	
		N = 16	1		1	
Bit 2	whether the moder bit 6 otherwise it re Logic 0 = Acquisiti Logic 1 = Acquisiti These control bits includes different of	s the receiver into single in scans antennas is controllects the receiver's choicon processing is for dual on processing is for single are used to indicate one combinations of Header field grequirements. The Header	rolled by this bit. If ce of antenna. antenna acquisitic e antenna acquisi of the four Preamb elds. Users can ch	in single and on. tion.  le Header moose the mo	tenna mode, the ANT_Si	Each of the mode
	Data length field (indicates the number of data bits that follow the Header information)     Full protocol Header					
	INPUT MOD		BIT 0		VE PREAMBLE - HEAD	ER FIELDS
	0	0			vith SFD Field	
	1	0			vith SFD, CRC16	
	3	1 1	0		vith SFD Length, CRC16vith Full Protocol Header	
			1 I			

Bit 7	Reserved (must set	to "0").						
Bit 6, 5	These control bits combined are used to select the number of chips per symbol used in the I and Q transmit paths (see table below).							
		CHIPS PER	BIT 6	BIT 5				
		11	0	0				
		13	0	1				
		15	1	0				
		16	1	1				
Bit 4, 3		re used to select the divide of N is determined by the fo		p clock timing. bl Rate = MCLK/(N x Chips	per symbol)			
		MASTER	BIT 4	BIT 3				
		N = 2	0	0				
		N = 4	0	1				
		N = 8	1	0				
		N = 16	1	1				
Bit 1	Logic 0: Accepts the	erating a TX_RDY to indica Preamble/Header informa 	tion from an externally g	enerated source. mitted data packet. When co	onfigured for mo			
	Logic 1 = DBPSK m Logic 0 = DQPSK m	odulation for data packet. nodulation for data packet.		-				
Bit 0	This control bit is use 1 and 2. See registe Logic 1 = DBPSK. Logic 0 = DQPSK.		Iulation type for the recei	ved data packet Used only w	ith header mod			
	CONFIGURA	TION REGISTER 4 ADDR	ESS (10h) INTERNAL T	EST REGISTER A				
Bit 7 - 0	tored to fault isolate will result to the follo Pin 46 (TEST7): Ca Pin 45 (TEST6): En	the device at manufacturing owing signals becoming ava- rrier Sense (CRS), a Logic ergy Detect (ED), a Logic 1 SI exceeds the threshold le	g testing. During normal ailable at the output test 1 indicates PN lock. indicates that there is e	nergy detected in the chann	commended. Th			
	CONFIGURATI	ON REGISTER 5 ADDRES	S (14h,18h) INTERNAL	TEST REGISTER B				
Bits 7 - 0	These bits need to be	pe programmed to 0h. They	are used for manufactu	ring test only.				
	CONFIGURA	TION REGISTER 7 ADDRE	SS (1Ch) MODEM STA	ATUS REGISTER A				
Bit 7	amble/Header data Logic 1: Indicates th data from the extern	internally. at the HSP3824 has compl aal source (i.e. MAC) to tran	eted transmitting Pream	d only when the HSP3824 g ble header information and i eamble Header information.	is ready to acce			

	CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A (Continued)
Bit 5	This status bit indicates the present state of clear channel assessment (CCA) which is output pin 32. The CCA is bein asserted as a result of a channel energy monitoring algorithm that is a function of RSSI, carrier sense, and time out counters that monitor the channel activity.
Bit 4	This status bit, when active indicates Carrier Sense, or PN lock. Logic 1: Carrier present. Logic 0: No Carrier Sense.
Bit 3	This status bit indicates whether the RSSI signal is above or below the programmed RSSI 6-bit threshold setting. This signal is referred as Energy Detect (ED).  Logic 1: RSSI is above the programmed threshold setting.  Logic 0: RSSI is below the programmed threshold setting.
Bit 2	This bit indicates the status of the output control pin MD_RDY (pin 34). It signals that a valid Preamble/Header has been received and that the next available bit on the TXD bus will be the first data packet bit.  Logic 1: Envelopes the data packet as it becomes available on pin 3 (TXD).  Logic 0: No data packet on TXD serial bus.
Bit 1	This status bit indicates whether the external device has acknowledged that the channel is clear for transmission. The is the same as the input signal TX_PE on pin 2.  Logic 1 = Acknowledgment that channel is clear to transmit.  Logic 0 = Channel is NOT clear to transmit.
Bit 0	This status bit indicates that a valid CRC16 has been calculated. The CRC16 is calculated on the Header informatio The CRC16 does not cover the preamble bits.  Logic 1 = Valid CRC16 check.  Logic 0 = Invalid CRC16 check.
	CONFIGURATION REGISTER 8 ADDRESS (20h) MODEM STATUS REGISTER B
Bit 7	This status bit is meaningful only when the device operates under the full protocol mode. Errors imply CRC errors of the header fields.  Logic 0 = Valid packet received.  Logic 1 = Errors in received packet.
Bit 6	This bit is used to indicate the status of the SFD search timer. The device monitors the incoming Header for the SFI If the timer, times out the HSP3824 returns to its signal acquisition mode looking to detect the next Preamble and Header.  Logic 1 = SFD not found, return to signal acquisition mode.  Logic 0 = No time out during SFD search.
Bit 5	This status bit is used to indicate the modulation type for the data packet. This signal is generated by the header d tection circuitry in the receive interface.  Logic 0 = DBPSK.  Logic 1 = DQPSK.
Bit 4	Unused, don't care.
Bit 3	Unused, don't care.
Bit 2	Unused, don't care.
Bit 1	Unused, don't care.
Bit 0	Unused, don't care.
	CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER
	This register is used to define the phase of clocks and other interface signals.
Bit 7	This bit needs to always be set to logic 0.

This control bit selects the active level of the MD\_RDY output pin 34.

Logic 1 = MD\_RDY is active 0. Logic 0 = MD\_RDY is active 1.

Bit 6

	CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER
Bit 5	This control bit selects the active level of the Clear Channel Assessment (CCA) output pin 32.  Logic 1 = CCA active 1.  Logic 0 = CCA active 0.
Bit 4	This control bit selects the active level of the Energy Detect (ED) output which is an output pin at the test port, pin 45.  Logic 1 = ED active 0.  Logic 0 = ED active 1.
Bit 3	This control bit selects the active level of the Carrier Sense (CRS) output pin which is an output pin at the test port, pin 46.  Logic 1 = CRS active 0.  Logic 0 = CRS active 1.
Bit 2	This control bit selects the active level of the transmit ready (TX_RDY) output pin 5.  Logic 1 = TX_RDY active 0.  Logic 0 = TX_RDY active 1.
Bit 1	This control bit selects the active level of the transmit enable (TX_PE) input pin 2.  Logic 1 = TX_PE active 0.  Logic 0 = TX_PE active 1.
Bit 0	This control bit selects the phase of the transmit output clock (TXCLK) pin 4.  Logic 1 = Inverted TXCLK.  Logic 0 = NON-Inverted TXCLK

#### **CONFIGURATION REGISTER 10 ADDRESS (28h) RSSI VALUE REGISTER**

Bits 0 - 7	This is a read only register re is updated at (chip rate/11). Example:				nip 6-bit ADC. This register
			BITS (0:7)	RANGE	
		RSSI_STAT	76543210		
			00000000	00h (Min)	
			00111111	3Fh (Max)	

#### CONFIGURATION REGISTER 11 ADDRESS (2ch) A/D CAL POS REGISTER

Bits 0 - 7	This 8-bit control register contains a binary value used for positive increment for the level adjusting circuit of the A/D
	reference. The larger the step the faster the level reaches saturation.

#### CONFIGURATION REGISTER 12 ADDRESS (30h) A/D CAL NEG REGISTER

	Bits 0 - 7	This 8-bit control register contains a binary value used for the negative increment for the level adjusting reference of
١		the A/D. The number is programmed as 256 - the value wanted since it is a negative number.

#### CONFIGURATION REGISTER 13 ADDRESS (34h) TX SPREAD SEQUENCE (HIGH)

	Bits 0 - 7	This 8-bit register is programmed with the upper byte of the transmit spreading code. This code is used for both the I
١		and Q signalling paths of the transmitter. This register combined with the lower byte TX_SPREAD(LOW) generates a
١		transmit spreading code programmable up to 16-bits. Code lengths permitted are 11, 13, 15, and 16. Right justified
ı		MSB first.

#### CONFIGURATION REGISTER 14 ADDRESS (38h) TX SPREAD SEQUENCE (LOW)

Bits 0 - 7 This 8-bit register is programmed with the lower byte of the transmit spreading code. This co

This 8-bit register is programmed with the lower byte of the transmit spreading code. This code is used for the I and Q signalling paths of the transmitter. This register combined with the higher byte TX\_SPREAD(HIGH) generates the transmit spreading code programmable up to 16-bits.

The example below illustrates the bit positioning for one of the 11-bit Barker PN codes. Example:

Fransmit Spreading Code 11-Bit Barker Word Hight Justified MSB First.

				MS	В								LS	B		
TX_SPREAD(HIGH)	15	14	13	12	11	10	9	8							-	
TX_SPREAD(LOW)									7	6	5	4	3	2	1	0
11-bit Barker code	Х	Χ	Χ	Χ	Х	1	0	1	1	0	1	1	1	0	0	0

#### **CONFIGURATION REGISTER 15 ADDRESS (3Ch) SCRAMBLER SEED**

Bits 0 - 7

This register contains the 7-bit (seed) value for the transmit scrambler which is used to preset the transmit scrambler to a known starting state. The MSB bit position (7) is unused and must be programmed to a Logic 0. The example below illustrates the bit positioning of seed.

#### CONFIGURATION REGISTER 16 ADDRESS (40h) SCRAMBLER TAP

Bits 0 - 7 This register is used to configure the transmit scrambler with a 7-bit polynomial tap configuration. The transmit scrambler is a 7-bit shift register, with 7 configurable taps. A logic 1 is the respective bit position enables that particular tap. The MSB bit 7 is not used and it is set to a Logic 0. The example below illustrates the register configuration for the polynomial  $F(x) = 1 + X^4 + X^7$ . Each clock is a shift left

		LSB
Bits (0:7)		76543210
		XZ <sup>-7</sup> Z <sup>-6</sup> Z <sup>-5</sup> Z <sup>-4</sup> Z <sup>-3</sup> Z <sup>-2</sup> Z <sup>-1</sup>
Scrambler Taps	$F(x) = 1 + X^{-4} + X^{-7}$	01001000

#### CONFIGURATION REGISTER 17 ADDRESS (44h)CCA TIMER THRESHOLD

Bits 0 - 7

This 8-bit register is used to configure the period of the time-out threshold of the CCA watchdog timer. If the channel is busy the timer counts until it reaches the programmed value and at that point it declares that the channel is clear independent of the actual energy measured within the channel. This register is programmable up to 8-bits.

Time (ms) =  $1000 \cdot \frac{N \cdot 5632}{\text{Chip Rate}}$ , where N is the programmable value of CR17.

For example, for a chip rate of 11 MCPS and a desired timeout of ~11ms, N = 2ch.

Bits 0 - 7

	LSB	
Bits (0:7)	76543210	
	0000010	02h (Min)
CCA_TIMER_TH	11111111	FFh (Max)

#### CONFIGURATION REGISTER 18 ADDRESS (48h) CCA CYCLE THRESHOLD

This 8-bit register is used to configure how many times the CCA timer is allowed to reach its maximum count before the channel is declared clear for transmission independent of the actual energy in the channel. This is an outer counter loop of the CCA timer. Each increment represents a time out of the CCA timer. Use a value of 03h for a time out of 2 CCA timer counts.

	MSB	LSB	
Bits (0:7)	7654	3210	
	0000	0010	2h; 1 CCA timer (Min)
CCA_TIMER_TH	1111	1111	FFh; 256 CCA timer (Max)

#### CONFIGURATION REGISTER 19 ADDRESS (4Ch) RSSI THRESHOLD, ENERGY DETECT

Bits 0 - 7	RSSI exceeds the thi	s the value for the RSSI th reshold ED is declared. El ammable. Bits 7 an 6 of th	D indicates the	e presence	of energy in the channel.	
			MSB	LSB		
		Bits (0:7)	76543	3210		

	MSB	LSB	
Bits (0:7)	7654	3210	
	0000	0000	00h (Min)
RSSI_STAT	0011	1111	3Fh (Max)

#### CONFIGURATION REGISTER 20 ADDRESS (50h) RX SPREAD SEQUENCE (HIGH)

Bits 0 - 7

This 8-bit register is programmed with the upper byte of the receive despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the lower byte RX\_SPRED(LOW) generates a receive despreading code programmable up to 16-bits. Right justified MSB first. See address 13 and 14 for example.

#### CONFIGURATION REGISTER 21 ADDRESS (54h) RX SPREAD SEQUENCE (LOW)

Bits 0 - 7

This 8-bit register is programmed with the lower byte of the receiver despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the upper byte RX\_SPRED(HIGH) generates a receive despreading code programmable up to 16-bits.

#### CONFIGURATION REGISTER 22 ADDRESS (58h) RX SIGNAL QUALITY 1 ACQ (HIGH) THRESHOLD

Bits 0 - 7

This control register contains the upper byte bits (8 - 14) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements made during acquisition at each antenna dwell. This threshold comparison is added with the SQ2 threshold in registers 30 and 31 for acquisition. A lower value on this threshold will increase the probability of detection and the probability of false alarm. Set the threshold according to instructions in the text.

#### CONFIGURATION REGISTER 23 ADDRESS (5Ch) RX SIGNAL QUALITY 1 ACQ THRESHOLD (LOW)

Bits 0 - 7 This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurement made during acquisition at each antenna dwell.

#### CONFIGURATION REGISTER 24 ADDRESS (60h) RX SIGNAL QUALITY 1 ACQ READ (HIGH)

Bits 0 - 7

This status register contains the upper byte bits (8 - 14) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the lower byte represents a 15-bit value, representing the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna.

#### CONFIGURATION REGISTER 25 ADDRESS (64h) RX SIGNAL QUALITY 1 ACQ READ (LOW)

Bits 0 - 7

This register contains the lower byte bits (0 - 7) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the higher byte represents a 15-bit value, of the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna.

#### CONFIGURATION REGISTER 26 ADDRESS (68h) RX SIGNAL QUALITY 1 DATA THRESHOLD (HIGH)

Bits 0 - 7

This control register contains the upper byte bits (8-14) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols. These thresholds set the drop lock probability. A higher value will increase the probability of dropping lock.

#### CONFIGURATION REGISTER ADDRESS 27 (6Ch) RX SIGNAL QUALITY 1 DATA THRESHOLD (LOW)

Bits 0 - 7

This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols.

CONF	IGURATION REGISTER 28 ADDRESS (70h) RX SIGNAL QUALITY 1 DATA (high) THRESHOLD READ (HIGH)
Bits 0 - 7	This status register contains the upper byte bits (8-14) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 15-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols.
co	NFIGURATION REGISTER 29 ADDRESS (74h) RX SIGNAL QUALITY 1 DATA THRESHOLD READ (LOW)
Bits 0 - 7	This register contains the lower byte bits (0-7) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 16-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols.
	CONFIGURATION REGISTER 30 ADDRESS (78h) RX SIGNAL QUALITY 2 ACQ THRESHOLD (HIGH)
Bits 0 - 7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold used for acquisition. This register combined with the lower byte represents a 16-bit threshold value for carrier phase variance measurement made during acquisition at each antenna dwell and is based on the choice of the best antenna. This threshold is used with the bit sync threshold in registers 22 and 23 to declare acquisition. A higher value in this threshold will increase the probability of acquisition and false alarm.
	CONFIGURATION REGISTER 31 ADDRESS (7Ch) RX SIGNAL QUALITY 2 ACQ THRESHOLD (LOW)
Bits 0 - 7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold used for acquisition.
	CONFIGURATION REGISTER 33 ADDRESS (84h) RX SIGNAL QUALITY 2 ACQ READ (LOW)
Bits 0 - 7	This status register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance used for acquisition. This register combined with the lower byte generates a 16-bit value, representing the measured signal quality of the carrier phase variance. This measurement is made during acquisition at each antenna dwell and is based on the selected best antenna
	CONFIGURATION REGISTER 34 ADDRESS (88h) RX SIGNAL QUALITY 2 DATA THRESHOLD (HIGH)
Bits 0-7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold. This register combined with the lower byte represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols.
	CONFIGURATION REGISTER 35 ADDRESS (8Ch) RX SIGNAL QUALITY 2 DATA THRESHOLD (LOW)
Bits 0-7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold. This register combined with the upper byte) represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols.
	CONFIGURATION REGISTER 36 ADDRESS (90h) RX SIGNAL QUALITY 2 DATA READ (HIGH)
Bits 0-7	This status register contains the upper byte bits (8-15) of the measured signal quality of the carrier phase variance. This register combined with the lower byte represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols.
	CONFIGURATION REGISTER 37 ADDRESS (94h) RX SIGNAL QUALITY 2 DATA READ (LOW)
Bits 0-7	This register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance. This register combined with the represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols.
	CONFIGURATION REGISTER ADDRESS 38 (98h) RX SIGNAL QUALITY 8-BIT READ
Bits 0 - 7	This 8-bit register contains the bit sync amplitude signal quality measurement derived from the 16-bit Bit Sync signal quality value stored in the CR28-29 registers. This value is the result of the signal quality measurement for the best antenna dwell. The signal quality measurement provides 256 levels of signal to noise measurement.
	CONFIGURATION REGISTER 39 ADDRESS RESERVED
	Reserved
	CONFIGURATION REGISTER 40 ADDRESS RESERVED
	Reserved

## Application Nata 0616

		Application N	ote 9616		
	CONFIGUR	RATION REGISTER 41 ADDF	RESS (A4h) SFD SEAI	RCH TIME	
Bits 0 - 7		mmed with an 8-bit value whic ader. Each bit increment repre	,		dulator to search for
	CONFIGU	IRATION REGISTER 42 ADD	RESS (A8h) DSBPSK	SIGNAL	
Bits 0 - 7	protocol operation at a	an 8-bit value indicating the da data rate of 1 MBPS, and is u etecting the modulation type or	ised in the transmitted	Signalling Field of the	
	CONFIGU	JRATION REGISTER 43 ADD	PRESS (ACh) DQPSK	SIGNAL	
Bits 0 - 7	protocol operation at a	the 8-bit value indicating the data rate of 2 MBPS and is unated the modulation type of	sed in the transmitted	Signalling Field of the	
	CONFIGURATION	I REGISTER 44 ADDRESS (E	30h) RX SERVICE FIE	LD (RESERVED)	
Bits 0 - 7		the detected received 8-bit val for future use and should be a		for the Header. This	field is reserved for
	CONFIGURAT	ION REGISTER 45 ADDRES	S (B4h) RX DATA LE	NGTH (HIGH)	
Bits 0 - 7		the detected higher byte (bits a lower byte indicates the num			in the Header. This
	CONFIGURAT	TION REGISTER 46 ADDRES	S (B8h) RX DATA LE	NGTH (LOW)	
Bits 0 - 7		the detected lower byte of the yte indicates the number of tra			ler. This byte com-
	CONFIGU	RATION REGISTER 47 ADDI	RESS (BCh) RX CRC1	16 (HIGH)	
Bíts 0 - 7	lower byte represents	the upper byte bits (8 -15) of th a 16-bit CRC16 value protecti ntrol bits at configuration regis	ng transmitted header.		
	CONFIGU	RATION REGISTER 48 ADD	RESS (C0h) RX CRC1	16 (LOW)	
Bits 0 - 7	upper byte represents	the lower byte bits (0-7) of the a 16-bit CRC16 value protecti ntrol bits at configuration regist	ng transmitted header.		
			MSB	LSB	
		RX_CRC16	15 14 13 12 11 10	9876543210	
		RX_CRC16(HIGH)	7 6 5 4 3 2	1 0	
		RX_CRC16(LOW)		76543210	

	MS	В											LS	В
RX_CRC16	15	14	13	12	11	10	9	8 7	7 6	5	4 :	3	2	10
RX_CRC16(HIGH)	7	6	5	4	3	2	1	0						
RX_CRC16(LOW)						-		7	6	5	4 3	3 :	2 .	1 0

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection, as defined in configuration register 2.

Mode 0 CRC16 not used

Mode 1 CRC16 protects SFD

Mode 2 CRC16 protects SFD, and Length Field

Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

#### CONFIGURATION REGISTER 49 ADDRESS (C4h) SFD (HIGH)

Bits 0 - 7 This 8-bit register contains the upper byte bits (8-15) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field.

D'1. 0. 7	T		DDRESS (C8h) SFD (LOW)		
Bits 0 - 7			of the SFD used for both the 16-bit value for the SFD field		Receive header. This
	CONFIGURA	ATION REGISTER 51 ADDR	ESS (CCh) TX SERVICE FI	ELD .	
Bits 0 - 7		ogrammed with the 8-bit valu and should be always a 00h	e of the Service Field to be to	ransmitted in a	Header. This field is
	CONFIGURATION	REGISTER 52 ADDRESS (I	00h) TX DATA LENGTH FIE	LD (HIGH)	
Bits 0 - 7	combined with the lowe		<ul> <li>of the transmit Length Field of bits to be transmitted in the n to reset after SFD.</li> </ul>		
	CONFIGURATION	REGISTER 53 ADDRESS (I	D4h) TX DATA LENGTH FIE	ELD (LOW)	
Bits 0 - 7	combined with the high	er byte indicates the number	of the transmit Length Field of the transmitted in the first to be transmitted in the first value would cause the first value would cause the first transmitter that the first transmitter is the first transmitter than the first transmitte	he data packet	, including the MAC
	CONFIGUR	ATION REGISTER 54 ADD	RESS (D8h) TX CRC16 (HIC	GH)	
Bits 0 - 7	combined with the lowe	er byte represents a 16-bit CF	6) of the transmitted CRC16 I RC16 value calculated by the uring the header mode control	HSP3824 to pr	rotect the transmitted
	CONFIGUR	ATION REGISTER 55 ADD	RESS (DCh) TX CRC16 (LC	OW)	
Bits 0 - 7	This 8-bit register contactombined with the high	ains the lower byte (bits 0-7) er byte represents a 16-bit Cl ected are selected by config	RESS (DCh) TX CRC16 (LC of the transmitted CRC16 Fi RC16 value calculated by the uring the header mode contro	eld for the Hea	rotect the transmitte
Bits 0 - 7	This 8-bit register conta	ains the lower byte (bits 0-7) er byte represents a 16-bit Cl ected are selected by config	of the transmitted CRC16 Fig RC16 value calculated by the	eld for the Hea	rotect the transmitte
Bits 0 - 7	This 8-bit register contactombined with the high	ains the lower byte (bits 0-7) er byte represents a 16-bit Cl ected are selected by config	of the transmitted CRC16 Fi RC16 value calculated by the uring the header mode control	eld for the Hea HSP3824 to p ol bits at registe	rotect the transmitte
Bits 0 - 7	This 8-bit register contactombined with the high	ains the lower byte (bits 0-7) er byte represents a 16-bit Cl ected are selected by config	of the transmitted CRC16 Final C16 value calculated by the uring the header mode control MSB	eld for the Hea HSP3824 to p ol bits at registe	rotect the transmitte
Bits 0 - 7	This 8-bit register contactombined with the high	ains the lower byte (bits 0-7) er byte represents a 16-bit Cl ected are selected by configu	of the transmitted CRC16 Fig. RC16 value calculated by the uring the header mode control MSB  15 14 13 12 11 10 9 8 7 6 7 6 5 4 3 2 1 0	eld for the Hea HSP3824 to p ol bits at registe	rotect the transmitte
Bits 0 - 7	This 8-bit register contacombined with the high-header. The fields proteconfiguration register 2	ains the lower byte (bits 0-7) er byte represents a 16-bit Cl ected are selected by configured by co	of the transmitted CRC16 Fig. RC16 value calculated by the uring the header mode control  MSB  15 14 13 12 11 10 9 8 7 6  7 6 5 4 3 2 1 0  Field protects the following field defined in register address (control)	eld for the Hea HSP3824 to piol bits at registe LSB 6 5 4 3 2 1 0 5 4 3 2 1 0 elds depending 02.	rotect the transmitter er address 02.
Bits 0 - 7	This 8-bit register contacombined with the high-header. The fields proteconfiguration register 2	ains the lower byte (bits 0-7) er byte represents a 16-bit Cl ected are selected by configured by co	of the transmitted CRC16 Fire RC16 value calculated by the uring the header mode control  MSB  15 14 13 12 11 10 9 8 7 6  7 6 5 4 3 2 1 0  7 6  Field protects the following field defined in register address (2)  Do, and Length Field	eld for the Hea HSP3824 to piol bits at registe LSB 6 5 4 3 2 1 0 5 4 3 2 1 0 elds depending 02.	rotect the transmitter er address 02.

# M APPNOTE

No. AN9617.1 January 1997

## Harris Wireless Products

# Hardware/Software Interface Description for PRISM™ Radio Design with an Example Using the AM79C930 Media Access Controller

Authors: John Fakatselis and Mike Paljug



#### Introduction

This document includes a description of the HW/SW interface for the IEEE802.11 target radio architecture

based on the Harris PRISM™ chip set and the AMD Media Access Controller (MAC) AM79C930 processor. The information includes all the necessary interface requirements that can be used to control the PRISM radio with any other controller or processor that does not necessarily target IEEE802.11. The design example, though, addresses special design issues interfacing with the AM79C930.

## Hardware Configuration

The block diagram in Figure 1 is intended to show a top level view of the basic hardware devices comprising the radio design. The detailed list of all signal interfaces required between MAC and the Physical Layer (PHY) or the PRISM radio are listed in Table 1 of this document.

## List of Signals

Table 1 summarizes the signals that are required to control the PHY radio operations. The first column lists the PHY signal name, the second column indicates whether the signal is an output or an input to the MAC, the next column contains a brief description of each listed signal and the last two columns indicate the HW component part number and the pin connection for each of the listed signals at both the PHY and the MAC ends.

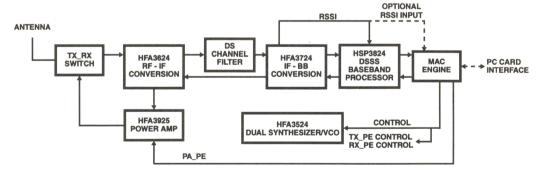


FIGURE 1. PRISM™ CHIPSET SYSTEM BLOCK DIAGRAM

## **Summary List of MAC-PHY Interface Signals**

## TABLE 1. MAC-PHY INTERFACE SIGNALS

PHY SIGNAL NAME	I/O FROM/ TO MAC	DESCRIPTION	PHY PART/PIN NUMBER	MAC PIN NUMBER AM79C930
SYNTH_DATA	0	Serial Data Bus (Synthesizer)	HFA3524 (12)	MAC (102)
SYNTH_CLK	0	Serial Control Clock (Synthesizer)	HFA3524 (11)	MAC (101)
SYNTH_LE	0	Load Enable (Synthesizer)	HFA3524 (13)	MAC (3)
RX_PE	0	Receive Power Enable (RF/IF Converter)	HFA3624 (28)	MAC (126)
TX_PE	0	Transmit Power Enable (RF/IF Converter)	HFA3624 (15)	MAC (142)
RX_PE	0	Receive Power Enable (Qmodem)	HFA3724 (21, 43, 54, 74)	MAC (126)
TX_PE	0	Transmit Power Enable (Qmodem)	HFA3724 (22, 41)	MAC (142)
SEL0	0	Low Pass Filter Control (Qmodem)	HFA3724 (17)	MAC (132)
SEL1	0	Low Pass Filter Control (Qmodem)	HFA3724 (16)	MAC (141)
TX_PE_BB	0	Transmit Power Enable (Transmit Port)	HSP3824 (2)	MAC (131)
TXD	0	Transmit Data (Transmit Port)	HSP3824 (3)	MAC (121)
TXCLK	1	Transmit Clock (Transmit Port)	HSP3824 (4)	MAC (115)
TX_RDY	1	Transmit Data Ready (Transmit Port)	HSP3824 (5)	MAC (91)
RX_PE_BB	0	Receiver Power Enable (Receive Port)	HSP3824 (33)	MAC (122)
MD_RDY	1	MAC Data Ready (Receive Port)	HSP3824 (34)	MAC (95)
RXD	1	Receive Data (Receive Port)	HSP3824 (35)	MAC (123)
RXCLK	1	Receive Clock (Receive Port)	HSP3824 (36)	MAC (124)
CS	0	Chip Select (Control Port)	HSP3824 (9)	MAC (107)
AS	0	Address Strobe (Control Port)	HSP3824 (23)	MAC (105)
R/W	0	Read/write Strobe (Control Port)	HSP3824 (8)	MAC (103)
SCLK	0	Serial Control Clock (Control Port)	HSP3824 (24)	MAC (101)
SDATA	I/O	Bi-directional Serial Data Bus (Control Port)	HSP3824 (25)	MAC (102)
CCA	ı	Clear Channel Assessment	HSP3824 (32)	MAC (96)
RESET	0	Master Reset	HSP3824 (28)	MAC (118)
PA_PE	0	Transmit Amplifier Power Enable (RFPA)	HFA3925 (11,18, 23)	MAC (131)
OSC_START	0	VCO Enable Circuit	VCO Startup Circuit	MAC (92)
RADIO_PE	0	Radio Power Enable	RADIO	MAC (2)

## **Interface Signal Description**

Table 2 Consists of a functional description for each of the PHY signals that are part of the HW/SW interface.

#### TABLE 2. MAC-PHY INTERFACE SIGNALS

SIGNAL NAME	SIGNAL DESCRIPTION				
SYNTH_DATA	Binary serial data input used to configure the PHY RF frequency synthesizer (HFA3524). Data is entered MSB first. A single data transfer is 22-bits wide. This is a high impedance CMOS input to the PHY.				
SYNTH_CLK	This is the clock for the SYNTH_DATA. The data is clocked in the appropriate synthesizer register on the rising edge of SYNTH_CLK. This is a high impedance CMOS input to the PHY.				
SYNTH_LE	Load enable for the PHY RF frequency synthesizer (HFA3524). When signal goes active (High), data stored in the shift register is loaded in one of the 4 synthesizer operational registers as defined by the control bits which are the two LSBs of the SYNTH_DATA.				
SEL0, SEL1	Digital control input to the PHY. Selects four programmed cut off frequencies for both receive and transmit channels of the analog baseband LPF. Tuning speed from one cutoff to another is less than 1ms. For IEEE802.11 the 8.8MHz cutoff frequency is used.  SEL1 SEL0 Cutoff Frequency SEL1 SEL0 Cutoff Frequency LO LO 2.2MHz HI LO 8.8MHz LO HI 4.4MHz				
TX_PE	Transmit Channel Power Enable Control Input. TTL compatible input. Enable logic level is High. This signal controls several IF/RF components of the PHY transmit chain. It is driving a total of 3 PHY inputs of the PHY components HFA3634 and HFA3724.				
RX_PE	Receive Channel Power Control Input. TTL compatible input. Enable logic level is High.This signal controls several IF/RF components of the PHY. It is driving a total of 5 PHY inputs of the PHY components HFA3624 and HFA3724.				
TX_PE_BB	TX_PE_BB is an input from the Media Access Controller (MAC). The rising edge of TX_PE_BB will start the internal transmit state machine of the PHY digital modem and the falling edge will inhibit the state machine. TX_PE_BB en velopes the transmit data.				
TXD	TXD is an input, used to transfer serial Data or Preamble/Header information bits from the MAC to the PHY digital modem (HSP3824). The data is received serially with the LSB first. The data is clocked in the HSP3824 at the falling edge of TXCLK.				
TXCLK	TXCLK is a clock output used to receive the data on the TXD from the MAC to the PHY digital modem (HSP3824), synchronously. Transmit data on the TXD bus is clocked into the PHY on the falling edge.				
TX_RDY	When the HSP3824 is configured to generate the Preamble and Header information internally, TX_RDY is an output to the external network processor indicating that Preamble and Header information has been generated and that the HSP3824 is ready to receive the data packet from the network processor over the TXD serial bus. TX_RDY returns to the inactive state when TX_PE goes inactive indicating the end of the data transmission. TX_RDY is an active high signal. This signal is meaningful only when the HSP3824 generates its own Preamble.				
CCA	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA algorithm is user programmable and makes its decision as a function of RSSI, Energy detect (ED), Carrier Sense (CRS) and the CCA watch dog timer. The CCA algorithm and its programmable features are described in the data sheet of the HSP3824 PHY component.  Logic 0 = Channel is clear to transmit.  Logic 1 = Channel is NOT clear to transmit (busy).  NOTE: This polarity is programmable and can be inverted.				
RXD	RXD is an output to the MAC transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD-RDY.				
RXCLK	RXCLK is the output bit clock to the MAC. This clock is used to transfer Header information and data through the RXD serial bus to the MAC. This clock reflects the bit rate in use. RXCLK will be held to a logic "0" state during the acquisition process of the PHY. RXCLK becomes active when the PHY enters in the data demodulation mode, im mediately following signal acquisition. This occurs once bit sync is declared and a valid signal quality estimate is made, when comparing the programmed signal quality thresholds.				
MD_RDY	MD_RDY is an output signal to the MAC, indicating a data packet is ready to be transferred to the MAC. MD_RDY is an active high signal and it envelopes the data transfer to the MAC over the RXD serial bus. MD_RDY returns to its inactive state when there is no more receiver data, when the programmable data length counter reaches its value or when the link has been interrupted. MD_RDY remains inactive during preamble synchronization. MD_RDY can be programmed to become active after the SFD detection in the protocol or after the CRC check field in the Header.				

TABLE 2. MAC-PHY INTERFACE SIGNALS (Continued)

SIGNAL NAME	SIGNAL DESCRIPTION
RX_PE_BB	When active, digital modem receiver of the PHY is configured to be operational, otherwise the digital modem receiver (HSP3824) is in standby mode. This is an active high input signal.
SD	SD is a serial bi-directional data bus which is used to transfer address and data to/from the internal registers of the PHY digital modem. The bit ordering of an 8-bit word is MSB first. The first 8-bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read from that register.
SCLK	SCLK is the clock for the SD serial bus of the PHY digital modem. The data on SD is clocked at the rising edge. SCLK is an input clock to the PHY digital modem (HSP3824). The maximum rate of this clock is 10MHz.
AS	AS is an address strobe used to envelope the Address or the data on SD of the PHY digital modem. This is an input signal to the PHY digital modem (HSP3824)  Logic 1 = envelopes the address bits.  Logic 0 = envelopes the data bits.
ŔW	R/W is an input to the PHY digital modem (HSP3824) used to change the direction of the SD bus when reading or writing data on the SD bus. R/W must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
CS	CS is a chip select for the PHY digital modem to activate the serial control port. This is an input signal to the PHY. The CS doesn't impact any of the other interface ports and signals, i.e., the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, AS and R/W become "don't care" signals.
RESET	Master reset for the PHY digital modem (HSP3824). When active, TX and RX functions are disabled. If RESET is kept low the HSP3824 goes into the power standby mode. RESET does not alter any of the configuration register values nor does it preset any of the registers into default values. The device requires programming upon power-up. RESET can be either active or inactive during programming of the device.
PA_PE	Enable for the PHY RF power amplifier (HFA3925) to start transmission. This is a digital interface. A Logic "1" enables the transmission.
OSC_START	Enable for the VCO Startup Circuit. A low going pulse of $200 \pm 10 \mu s$ is required to activate the VCO after programming the synthesizer.
RADIO_PE	Enable for power regulators and clocks driving the PHY. A logic "1" enables operation, a logic "0" puts the complete PHY in a power down mode.

#### HW/SW Interfaces

There are four primary HW/SW interfaces that are used for configuration and during normal operation of the device. The interfaces are power on initialization, transmit mode operation, receive mode operation and power shut down mode. These interfaces are summarized as follows

- The Initialization & Control Interface, which is used to configure, write and/or read the status of the physical layer digital modem and the RF synthesizer. This interface is required to configure the programmable portions of the PHY during power up and coming out of certain power down modes. This interface is also used during operations for real time reconfiguration of PHY parameters and / or for reading PHY status.
- The TX Interface, which is used to control the transmit data transfers between the MAC and the physical layer. It is also used to control all PHY devices for the transmit chain of the radio.
- The RX Interface, which is used to control the receive data transfers between the MAC and the physical layer. It is also used to control all PHY devices for the receive chain of the radio.
- The Power Down Interface, which is used to set the physical layer into one of three power savings modes.

#### **INITIALIZATION & CONTROL INTERFACE**

This HW/SW interface is used to configure and monitor the programmable registers of the PHY. There are two PHY devices that contain programmable registers:

- · The digital modem
- The RF frequency synthesizer. This interface is required to configure the PHY radio upon power up initialization and to monitor status during normal operation. This interface is also used to select or switch the frequency channel as required for the transmit and receive operations.

#### **Digital Modem Interface**

The signals necessary to accomplish the functions of this interface are:

CS: Chip select

AS: Address strobe

R/W: Read / Write strobe

SD: Serial Data.

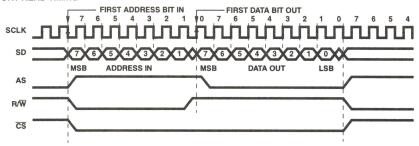
SCLK: Serial Data Clock.

This HW/SW interface is required to configure the digital modem registers and performs all read and write operations to and from the digital modem. The serial control interface is used to serially write and read data to/from the digital

modem. This serial interface can operate up to a 10MHz rate or the maximum sampling clock rate of the PHY (whichever is lower). The sampling or master clock of the physical layer is designated as MCLK and must be running during programming. This interface is used to program and to read all internal registers. The first 8-bits always represent the address followed immediately by the 8 data bits for that register. The serial transfers are accomplished through the serial data signal (SD). SD is a bi-directional serial data bus. An Address Strobe (AS), Chip Select (CS), and ReadWrite (R/W) are also required as handshake signals for this interface. The clock used in conjunction with the address and

data on SD is SCLK. This clock is provided to the PHY. The timing relationships of these signals are illustrated in Figure 2. AS is active high during the clocking of the address bits. R/W is high when data is to be read, and low when it is to be written. CS must be active (low) during the entire data transfer cycle. CS selects the device. The serial control interface operates asynchronously from the TX and RX interfaces and can accomplish data transfers independent of the activity at the other digital or analog interfaces. CS does not effect the TX or RX operation of the device; impacting only the operation of the Control interface.

#### **CONTROL PORT READ TIMING**



#### CONTROL PORT WRITE TIMING

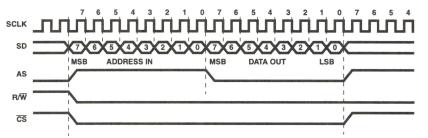


FIGURE 2. DIGITAL MODEM CONTROL INTERFACE

#### **PHY Modem Configuration**

The PHY modem has 57 internal registers that can be configured through the control interface. These registers are listed in Table 3 below. The table lists the configuration register number, a brief name describing the register, and the HEX address to access each of the registers. The type indi-

cates whether the corresponding register is Read only (R) or Read/Write (R/W). Some registers are two bytes wide as indicated on the table (high & low bytes). Table 3 indicates the proper modem register configuration to implement the IEEE802.11 requirements as of the JULY 95 proposed draft.

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR0	MODEM CONFIG. REG #1	R/W	00	1E
CR1	MODEM CONFIG. REG #2	R/W	04	82
CR2	MODEM CONFIG. REG #3 ytd	R/W	08	23
CR3	MODEM CONFIG. REG #4	R/W	0C	03
CR4	INTERNAL TEST REGISTER #1	R/W	10	00
CR5	INTERNAL TEST REGISTER #2	R/W	14	00

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR6	INTERNAL TEST REGISTER #3	R	18	-
CR7	MODEM STATUS REGISTER #1	R	1C	•
CR8	MODEM STATUS REGISTER #2	R	20	-
CR9	I/O DEFINITION REGISTER	R/W	24	00
CR10	RSSI VALUE REGISTER	R	28	
CR11	ADC_CAL_POS REGISTER	R/W	2C	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD
CR13	TX_SPREAD SEQUENCE (HIGH)	R/W	34	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8
CR15	SCRAMBLE_SEED	R/W	3C	7F
CR16	SCRAMBLE_TAP (RX & TX)	R/W	40	48
CR17	CCA_TIMER_TH	R/W	44	2C
CR18	CCA_CYCLE_TH	R/W	48	03
CR19	RSSI_TH	R/W	4C	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05
CR21	RX_SPREAD SEQUENCE (LOW)	R/W	54	B8
CR22	RX_SQ1_ACQ (HIGH) THRESHOLD	R/W	58	01
CR23	RX_SQ1_ACQ (LOW) THRESHOLD	R/W	5C	E8
CR24	RX_SQ1_ACQ (HIGH) READ	· R	60	•
CR25	RX_SQ1_ACQ (LOW) READ	R	64	-
CR26	RX_SQ1_DATA (HIGH) THRESHOLD	R/W	68	00
CR27	RX_SQ1_DATA (LOW) THRESHOLD	R/W 6C	00	-
CR28	RX_SQ1_DATA (HIGH) READ	R	70	-
CR29	RX_SQ1_DATA (LOW) READ	R	74	-
CR30	RX_SQ2_ACQ (HIGH) THRESHOLD	R/W	78	00
CR31	RX_SQ2_ACQ (LOW) THRESHOLD	R/W	7C	CA
CR32	RX_SQ2_ACQ (HIGH) READ	R	80	-
CR33	RX_SQ2_ACQ (LOW) READ	R	84	-
CR34	RX_SQ2_DATA (HIGH) THRESHOLD	R/W	88	FF
CR35	RX_SQ2_DATA (LOW) THRESHOLD	R/W	8C	FF
CR36	RX_SQ2_DATA (HIGH) READ	R	90	-
CR37	RX_SQ2_DATA (LOW) READ	R	94	-
CR38	RX_SQ_READ FULL PROTOCOL	R	98	-
CR39	RESERVED	w	9C	00
CR40	RESERVED	w	A0	00
CR41	UW_TIME_OUT_LENGTH	R/W	A4	90
CR42	SIG_DBPSK FIELD	R/W	A8	0A
CR43	SIG_DQPSK FIELD	R/W	AC	14

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR44	RX_SER_FIELD	R	ВО	-
CR45	RX_LEN FIELD (HIGH)	R	B4	-
CR46	RX_LEN FIELD (LOW)	R	B8	-
CR47	RX_CRC16 (HIGH)	R	ВС	-
CR48	RX_CRC16 (LOW)	R	C0	-
CR49	UW (HIGH)	R/W	C4	F3
CR50	UW (LOW)	R/W	C8	A0
CR51	TX_SER_F	R/W	CC	00
CR52	TX_LEN (HIGH)	R	D0	-
CR53	TX_LEN (LOW)	R	D4	-
CR54	TX_CRC16 (HIGH)	R	D8	-
CR55	TX_CRC16 (LOW)	R	DC	-
CR56	TX_PREM_LEN	R/W	E0	80

#### Synthesizer Interface

The following signals are required to accomplish the functions of this interface:

Synth\_Data: Serial Synthesizer Data Synth\_Clk: Synthesizer Data Clock Synth\_LE: Synthesizer Load Enable These signals are utilized to configure the RF frequency synthesizer. The synthesizer tunes the radio to the appropriate receive and transmit channels. Figure 3 illustrates the required timing to write the appropriate frequency to the PHY synthesizer.

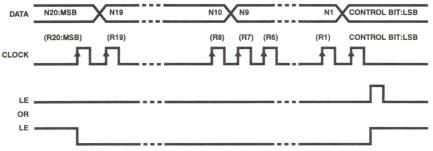


FIGURE 3. SYNTHESIZER SERIAL DATA INTERFACE

The following Data patterns are required to initialize the PHY synthesizer for IEEE802.11 operation. It should be noted that the register order is important with IF R first followed by IF N, RF R, and RF N. Also note that when powering up or coming out of Power Down Mode #2 (see page 10). The 4 registers should be written to twice. This is because the device RF and IF sections should be enabled before configuring the R and N pairs; and this effectively occurs if the values below are written twice in the IF R, IF N, RF R, RF N order. Also note that the OSC\_START signal must follow any synthesizer programming cycle.

SYNTH\_DATA 16,1801h
SYNTH\_DATA 6,60h
SYNTH\_DATA 16,4118h
SYNTH\_DATA 6,04h
SYNTH\_DATA 16,1801h
SYNTH\_DATA 6,68h

;IF R Counter register initialization.

;IF N Counter register initialization.

;RF R Counter register initialization.

The Harris\_Freq\_Table holds the 22-bit values for the synthesizer RF N Counter control register. Each entry is comprised of three bytes. Eight bits of the first byte is serially shifted out to the synthesizer (MSBit first), followed by 8-bits of the second byte (MSBit first), followed finally by the 6 MSBits of the third byte (MSBit first). The two LSBits of the third byte in each entry are ignored. The synthesizer configuration for each of the 12 IEEE802.11 channels is shown below.

Н

larris_Freq_Table	label byte	
db	02h, 011h, 04Ch	;Channel 1
db	02h, 011h, 09Ch	;Channel 2
db	02h, 011h, 0ECh	;Channel 3
db	02h, 018h, 03Ch	;Channel 4
db	02h, 018h, 08Ch	;Channel 5
db	02h, 018h, 0DCh	;Channel 6
db	02h, 019h, 02Ch	;Channel 7
db	02h, 019h, 07Ch	;Channel 8
db	02h, 019h, 0CCh	;Channel 9
db	02h, 020h, 01Ch	;Channel 10
db	02h, 020h, 06Ch	;Channel 11
db	02h, 021h, 0CCh	;Channel 12

#### TX INTERFACE

The signals required for the control of the transmit functions of the radio are:

TX PE BB: Transmit power enable for digital modem

TXD: Transmit digital data

TXCLK: Transmit data clock

TX\_RDY: Transmit data ready

TX\_PE: Transmit power enable for RF and IF sections

PA\_PE: Power amplifier transmit enable

SEL 0,1: Selection of appropriate baseband LPF

CCA: Clear channel assessment indicator from PHY

To initiate the transmit operation the MAC generates TX\_PE. The Preamble and Header are then generated by the PHY. Finally, when cued, the MAC delivers the data packet to the PHY for transmission. The transmit data digital interface transfers the data that needs to be transmitted serially to the PHY. The data is modulated and transmitted as soon as it is received from the MAC. The serial digital data is input to the PHY through TXD using the falling edge of TXCLK to clock it in the PHY. TXCLK is an output from the PHY. A timing diagram of the transmit signal sequence is shown on Figure 4.

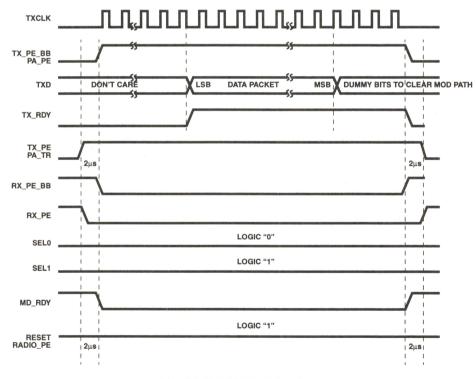


FIGURE 4. TRANSMIT TIMING DIAGRAM

The preamble and PHY header transmission is always at a 1 MBPS (BPSK) data rate. The MAC header and data that follows can be either at 1 MBPS (BPSK) or at 2 MBPS (QPSK). To avoid rate switching within any single transmission between the MAC-PHY interface, the TXCLK will always be at the higher rate of 2 MBPS. This implies that each of the BPSK symbols needs to be coming into the PHY twice. The MAC needs to send the same BPSK symbol twice at a rate of 2 MBPS and this action will make it equivalent to the required BPSK symbol rate of 1 MBPS. If QPSK data bits follow the PHY header, they will be sent from the MAC to the PHY only once at the 2 MBPS rate.

The MAC initiates the transmit sequence by asserting TX\_PE. Then TX\_PE\_BB envelopes the transmit data packet on TXD. The PHY responds by generating TXCLK to input the serial data on TXD. TXCLK will run until TX\_PE\_BB goes back to its inactive state indicating the end of the data packet. In addition Figure 4 illustrates the state of the PHY receive signals while transmitting as well as, the power enable, reset, and filter select proper signal states.

The PHY supports two possible data transfer scenarios, one where the preamble and header fields are generated within the PHY and one where the MAC generates the preamble and header fields. The scenario described herein assumes that the PHY generates the preamble and PHY header.

During this mode the PHY will immediately start transmitting the preamble and header as internally generated. Data available on TXD upon assertion of TX\_PE\_BB would be ignored. When the internally generated preamble and header are finished the PHY asserts TX\_RDY. This signals the MAC to begin sending the data packet. TX\_RDY assertion timing is programmable via Configuration Register (CR) 1. The timing diagram of this TX scenario, where the preamble and header are generated internal to the PHY, is illustrated on Figure 4.

One other signal that can be used to assist MAC transmit decisions as part of the TX interface is the Clear Channel Assessment (CCA) signal which is an output from the PHY. The CCA provides the indication that the channel is clear of energy and the transmission will not be subject to collisions. CCA can be monitored by the MAC to assist in deciding when to initiate transmissions. The CCA indication can be bypassed or ignored by the MAC without impacting any of the physical layer operations. The state of the CCA does not effect the transmit operation of the PHY. TX\_PE and TX\_PE\_BB will always initiate the transmit state independent of the state of CCA. The CCA timing is not shown in the timing diagram of Figure 4 since it is an optional signal and does not influence the PHY transmit operations.

Signals TX\_RDY, TX\_PE\_BB and TXCLK can be set individually, by programming CR9, as either active high or active low signals.

To avoid increasing throughput delays it is critical that the timing of TX\_PE and RX\_PE are as close to complementary of each other as possible.

When first attempting to transmit upon power-up, PA\_PE must stay low for at least 10ms after RADIO\_PE goes high.

#### **RX INTERFACE**

The signals that control the receive functions of the radio are:

RX\_PE\_BB: Receive power enable for digital PHY modem

MD\_RDY: MAC data ready, enveloping the MAC data

packet from the PHY

RXD: Receive serial baseband data to the MAC

RXCLK: Receive data clock to the MAC

RX\_PE: Receive power enable for the RF and IF section of the PHY radio

SEL 0,1: Receive LPF frequency select

Timing diagram, Figure 5 illustrates the relationships between the various signals required to control the PHY during the receive operations.

The receive data interface of the PHY digital modem (RXD) serially outputs the demodulated data to the MAC. The data is output as soon as it is demodulated by the PHY. RX\_PE and RX\_PE\_BB must be at their active state throughout the receive operation. When RX\_PE, RX\_PE\_BB are inactive the PHY receive functions, including acquisition,. will be in a stand by mode. The timing relationships between RX\_PE and RX\_PE\_BB, as well as, the state of the transmit signals, power enable signals, reset and filter select signal states are illustrated on Figure 5 for the receive operation during the reception of a single packet.

RXCLK is an output from the PHY and is the clock for the serial demodulated data on RXD. MD\_RDY is an output from the PHY and it envelopes the valid data on RXD. MD\_RDY is programmable and is asserted either after the Start Frame Delimiter field has been detected or immediately after the CRC field of the header has been checked. MD\_RDY is programmed through CR3, bit-7 to select when it will be asserted. The PHY may also be programmed to ignore error detection during the CRC check of the header fields. If programmed to ignore errors the device continues to output the demodulated data in its entirety regardless of the CRC check result. This option is programmed through CR2, bit-5.

The preamble and PHY header are always received at a 1 MBPS (BPSK) data rate. The MAC header and data that follows can be either at 1 MBPS (BPSK) or at 2 MBPS (QPSK). To avoid rate switching within any single packet reception between the MAC-PHY interface, the RXCLK will always be at the higher rate of 2 MBPS. This implies that each of the BPSK symbols is coming out of the PHY twice. The PHY sends to the MAC the same BPSK symbol twice at a rate of 2 MBPS and this action will make it equivalent to the required BPSK symbol rate of 1 MBPS. If QPSK data bits follow the PHY header, they will be sent to the MAC from the PHY only once at the 2 MBPS rate.

If rate switching is not an issue for the controller (MAC) then the HSP3824 can be configured to rate switch within the packet. The HSP3824 can automatically switch from BPSK to the QPSK rate at the appropriate time.

Note that RXCLK and RXD become active after acquisition, well before MD\_RDY is asserted. MD\_RDY returns to its inactive state under the following conditions:

- The number of data symbols, as defined by the length field in the protocol, has been received and output through RXD in its entirety (normal condition).
- · PN tracking is lost during demodulation.
- RX\_PE\_BB is deactivated by the MAC.

MD\_RDY can be configured through CR9, bit-6 to be active low, or active high.

To avoid increasing throughput delays it is critical that the timing of TX\_PE and RX\_PE are as close to complementary of each other as possible.

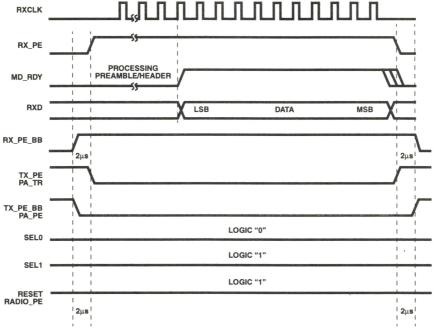


FIGURE 5. RECEIVE TIMING DIAGRAM

#### **POWER DOWN MODES**

The power consumption modes of the PHY are controlled by the following control signals:

- Receiver Power Enable (RX\_PE & RX\_PE\_BB), which disable the radio receiver when inactive.
- Transmitter Power Enable (TX\_PE & TX\_PE\_BB & PA\_PE), which disable the radio transmitter when inactive.
- Reset (RESET), which puts the digital receiver in a sleep mode when it is asserted at least 2 MCLK's after RX\_PE is set at its inactive state.
- RADIO\_PE, which disables power regulators and all digital clocks to the PHY.
- In addition the radio RF synthesizer is programmable and can be set at a maximum power savings mode.

Utilizing the availability of the signals above there are three power savings modes defined:

• Power Down mode #1: During this mode the current consumption of the radio is estimated at 38mA. The radio can not receive or transmit when configured for this mode. When in this mode, it takes 25µs. to return the radio in its operational mode. when set in this mode, the PHY maintains its configuration data. There is no need to reprogram any of the radio register values. To activate Power Down mode #1 the following signals need to be set at the states shown below:

RX\_PE: LOW
RX\_PE\_BB: LOW
TX\_PE: LOW
TX\_PE\_BB: LOW
PA\_PE: LOW
RESET: LOW
RADIO\_PE: HIGH

· Power Down mode #2: During this mode the current consumption of the radio is estimated at 23mA. The radio cannot receive or transmit when configured for this mode. When in this mode, it takes 2ms. to return the radio in its operational mode. During this mode the synthesizer is programmed into its power savings mode. When set at this mode, the PHY maintains its configuration data. There is no need to reprogram any of the radio register values. However, the Synthesizer needs to be reprogrammed according to Synthesizer Interface Section on page 7.

To activate Power Down mode #2 the following signals need to be set as shown below:

RX PE: LOW RX PE BB: LOW TX\_PE: LOW TX\_PE\_BB: LOW PA\_PE: LOW RESET: LOW RADIO PE: HIGH

In addition the Synthesizer needs to be programmed via the synthesizer configuration interface as shown below:

SYNTH\_DATA 16,1801h SYNTH\_DATA 6,0h

;IF R Counter register initialization.

SYNTH DATA 16.0C118h

:IF N Counter register

SYNTH DATA 6,04h

initialization.

SYNTH DATA 16,1801h SYNTH DATA 6,68h

SYNTH\_DATA 16,8211h SYNTH DATA 6.4Ch

:RF N Counter register

initialization. :RF N Counter register

initialization.

· Power Down mode #3: During this mode the current consumption of the radio is estimated at 1ma. The radio can not receive or transmit when configured for this mode. When set in this mode, it takes 15ms, to return the radio to its operational mode. When set in this mode, the PHY does not maintain its register configuration. All radio register values need to be reprogrammed to resume operation. This holds for both the PHY digital modem (HSP3824) and the PHY frequency synthesizer (HFA3925). To activate Power Down mode #3 the following signals need to be set as shown below:

RX\_PE: Don't Care RX PE BB: LOW TX PE: Don't Care TX\_PE\_BB: LOW PA PE: LOW RESET: LOW RADIO PE: LOW

When first attempting to transmit upon power-up, PA\_PE must stay low for at least 10ms after RADIO\_PE goes high.

## Appendix A

## **Control Register Values for Single Antenna Acquisition**

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR0	MODEM CONFIG. REG #1	R/W	00	3C	64
CR1	MODEM CONFIG. REG#2	R/W	04	00	00
CR2	MODEM CONFIG. REG#3	R/W	08	07	24
CR3	MODEM CONFIG. REG#4	R/W	0C	04	87
CR4	INTERNAL TEST REGISTER#1	R/W	10	00	00
CR5	INTERNAL TEST REGISTER #2	R/W	14	00	00
CR6	INTERNAL TEST REGISTER#3	R/W	18	00	00
CR7	MODEM STATUS REGISTER #1	R	1C	Х	х
CR8	MODEM STATUS REGISTER #2	R	20	Х	х
CR9	I/O DEFINITION REGISTER	R/W	24	00	00
CR10	RSSI VALUESTATUS REGISTER #2	R	28	×	×
CR11	ADC_CAL_POS REGISTER	R/W	2C	01	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD	FD

Appendix A

Control Register Values for Single Antenna Acquisition (Continued)

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR13	TX_SPREAD SEQUENCE (HIGH)	R/W	34	05	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8	B8
CR15	SCRAMBLE_SEED	R/W	3C	7F	7F
CR16	SCRAMBLE_TAP (RX & TX)	R/W	40	48	48
CR17	CCA_TIMER_TH	R/W	44	2C	2C
CR18	CCA_CYCLE_TH	R/W	48	03	03
CR19	RSSI_TH	R/W	4C	1E	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05	05
CR21	RX_SREAD SEQUENCE (LOW)	R/W	54	B8	B8
CR22	RX_SQ1_ IN_ACQ(HIGH) THRESHOLD	R/W	58	01	01
CR23	RX-SQ1_ IN_ACQ(LOW) THRESHOLD	R/W	5C	E8	E8
CR24	RX-SQ1_ OUT_ACQ(HIGH) READ	R	60	Х	×
CR25	RX-SQ1_ OUT_ACQ (LOW) READ	R	64	Х	х
CR26	RX-SQ1_ IN_DATA (HIGH) THRESHOLD	R/W	68	0F	0F
CR27	RX-SQ1-SQ1_ IN_DATA (LOW) THRESHOLD	R/W	6C	FF	FF
CR28	RX-SQ1_ OUT_DATA (HIGH) READ	R	70	х	х
CR29	RX-SQ1_ OUT_DATA (LOW) READ	R	74	х	х
CR30	RX-SQ2_ IN_ACQ (HIGH) THRESHOLD	R/W	78	00	00
CR31	RX-SQ2- IN-ACQ (LOW) THRESHOLD	R/W	7C	CA	CA
CR32	RX-SQ2_ OUT_ACQ (HIGH) READ	R	80	х	х
CR33	RX-SQ2_ OUT_ACQ (LOW) READ	R	84	х	х
CR34	RX-SQ2_IN_DATA (HIGH) THRESHOLD	R/W	88	09	09
CR35	RX-SQ2_ IN_DATA (LOW) THRESHOLD	R/W	8C	80	80
CR36	RX-SQ2_ OUT_DATA (HIGH) READ	R	90	х	Х
CR37	RX-SQ2_ OUT_DATA (LOW) READ	R	94	Х	Х
CR38	RX_SQ_READ; FULL PROTOCOL80211	R	98	Х	Х
CR39	RESERVED	W	9C	Х	Х
CR40	RESERVED	w	A0	х	Х
CR41	UW_TIME_OUT_LENGTH	R/W	A4	90	90

## Appendix A

## Control Register Values for Single Antenna Acquisition (Continued)

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR42	SIG_DBPSK Field	R/W	A8	0A	0A
CR43	SIG_DQPSK Field	R/W	AC	14	14
CR44	RX_SER_Field	R	В0	Х	х
CR45	RX_LEN Field (HIGH)	R	B4	Х	Х
CR46	RX_LEN Field (LOW)	R	B8	×	Х
CR47	RX_CRC16 (HIGH)	R	BC	х	х
CR48	RX_CRC16 (LOW)	R	C0	Х	х
CR49	UW -(HIGH)	R/W	C4	F3	F3
CR50	UW _(LOW)	R/W	C8	A0	A0
CR51	TX_SER_F	R/W	cc	00	00
CR52	TX_LEN (HIGH)	R	D0	х	Х
CR53	TX_LEN(LOW)	R	D4	Х	Х
CR54	TX_CRC16 (HIGH)	R	D8	х	х
CR55	TX_CRC16 (LOW)	R	DC	х	Х
CR56	TX_PREM_LEN	R/W	E0	80	80

# MAPPIOTE APPIOTE

No. AN9618.2 August 1996

## Harris Linear

# Using the PRISM™ HFA3624 Evaluation Board

Author: Bob Rood



#### Introduction

The HFA3624 Up/Down converter is one of the five chips in the Harris 2.4GHz PRISM™ chip set providing a solution

for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3624 is a monolithic bipolar device for up/down conversion applications in the 2.4GHz to 2.5GHz band. The device consists of a low noise amplifier and down conversion mixer in the receive section and an up conversion mixer with power preamp in the transmit section. An energy saving power enable control feature assures isolation between the receive and transmit circuits for half duplex systems.

## **Board Description**

The evaluation board provides maximum flexibility and ease of use by bringing out all device ports in a  $50\Omega$  impedance as shown in Figure 2. The HFA3624 inputs and outputs have been designed to provide a 50\Omega matched impedance with a minimum VSWR of 2:1, in the ISM band, with the exception of the IF ports. High Impedance IF ports give the customer another degree of design freedom when using non-50 $\Omega$  IF filtering or when higher transmit gain is desired. The evaluation board is built with an application circuit that transforms these high impedance ports to  $50\Omega$  but also provides optional circuit topology for other impedance values. This board provides a means of evaluating the HFA3624 as a stand alone device. Performance may vary in the final application due to non-ideal source and load impedance. In particular the ISM and IF bandpass filters may enhance or degrade basic performance depending on implementation.

#### Receive Mixer Differential IF Port

The differential open collector output port of the HFA3624 can provide maximum gain into a high impedance while using a minimum of power. Additionally matching to high impedance IF filters is simplified. A differential to single ended conversion circuit on the evaluation board has both wide bandwidth and high gain. The 70MHz -3dB IF bandwidth far exceeds the 18MHz DSSS signal requirement thus reducing the need for precision component values or trimming capacitors. The HFA3624 data sheet covers several other IF output circuit that can be used including; single ended output and differential to single ended conversion using a transformer. The differential to single ended

circuit provided offers high performance, low component cost and space savings, as well as a low profile for PCMCIA applications.

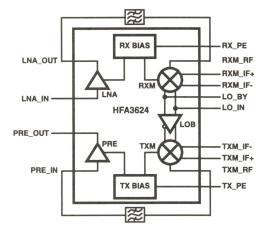


FIGURE 1.

## Transmit Mixer IF Input Port

The high impedance of the Transmit IF input gives the flexibility and ease to match high impedance IF filters as well a means of boosting transmit gain. An IF impedance of  $250\Omega$  instead of  $50\Omega$  will boost Transmit gain by 7dB. A  $50\Omega$  termination resistor is provided on board to give a good broadband match but optional component pads are provided for narrow band networks to transform the impedance from a  $50\Omega$  source to a higher value at the IF input.

#### Power Enable Control

The HFA3624 has two power enable control pins, the Receive Enable and the Transmit Enable. Although both Transmit and Receive channels will operate at the same time, Full Duplex mode, this operation is not recommended as considerable crosstalk and interference will be experienced. The RX\_PE and TX\_PE pins are connected to on board jumpers. The black plastic square jumpers enable the channel by connecting the enable pin to  $V_{\rm CC}$ . Leaving the enable pin open will disable the channel. Jumper JP1, near the power supply wires at the top of the board, controls

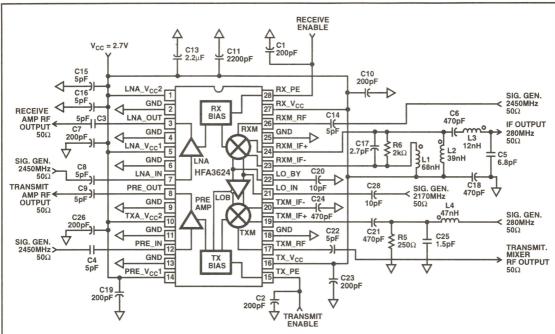


FIGURE 2. OPTIMIZED LAB EVALUATION CIRCUIT

Receive Enable while JP2, near the bottom, controls Transmit Enable. The enable pins each have a 200pF capacitor connected to ground to reduce sensitivity to noise or oscillation. These capacitors may slow the Power Enable/ Disable response time and should be removed before the evaluation of this parameter.

# Chip Component Selection

The HFA3624 Evaluation Board has been optimized for performance at an RF frequency of 2.4GHz to 2.5GHz and an IF frequency of 280MHz. The HFA3624 is capable of operating at other frequencies but care needs to be taken to select good quality RF components with self resonant frequencies (SRF) outside the boundaries of the application. A parts list is provided with the evaluation board to ensure that customers can duplicate the device performance in their application.

Operating a chip component close to its self resonant frequency will strongly effect its value. Knowing a component's effective impedance at the operating frequency is critical to the circuits proper operation; and this is how the SRF may be used to advantage. The AC bypass capacitors and power supply decoupling capacitors present their lowest impedance at the self resonant frequency. The RF and LO bypass capacitors were selected to be 5pF (0402) and 10pF to correspond with the SRF of 2.4GHz and 1.8GHz respectively. Likewise, the 470pF (0402) IF bypass capacitors have a SRF of 280MHz.

The inductors of the differential to single ended circuit form both a series and a parallel resonant circuit to provide high mixer gain. High Q inductors are recommended to provide a high and stable load impedance.

# Fixture Microstrip Return Loss

The Microstrip of the Evaluation Board has been designed to minimize fixture related limitations to device performance and measurement. A special low loss dielectric material GETEK has been used along with End Launch SMA connectors to minimize distortions. Figures 3 and 4 show the Return Loss and TDR plots of an evaluation board microstrip trace terminated into  $50\Omega$ 

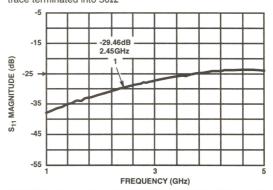


FIGURE 3. EVALUATION BOARD MICROSTRIP RETURN LOSS

# Test Set-Up Diagrams

The accuracy and correlation of test measurements often depend on the details of the test set-up. Therefore, several set-up diagrams (Figures 5 and 7) are included to aid in the verification of HFA3624 performance as well as evaluation of performance in the application.

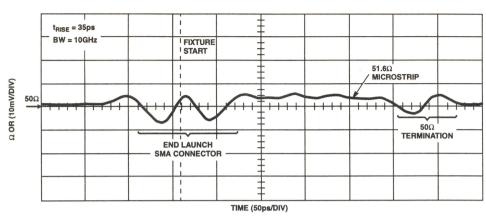


FIGURE 4. EVALUATION BOARD MICROSTRIP TIME DOMAIN REFLECTOMETRY

# Receive Mixer Third Order Intercept

Third order intercept (TOI) measures the non-linear performance of the mixer by measuring the 3rd order distortion products that may appear in band causing interference. Issues in the TOI measurement (Figure 5) are:

- Isolators are required on Signal Generators to prevent generator distortion products.
- The Bandpass Filter (BPF) on the LO signal is optional for the TOI test but is required for the Noise Figure Test. Including the BPF in the TOI test makes switching between the two test set-ups easier.
- 50Ω termination caps are required on unused ports of the active channel. For the TOI test, place 50Ω terminations on LNA\_IN and LNA\_OUT.
- The three signal generators must be phase locked together to prevent frequency drift. This is accomplished with the external 10MHz reference jacks on the rear panel of the Marconi 2041 Signal Generators. The external reference settings are accessed under the UTIL menu.
- · The Signal Generator frequencies for the TOI test are;
  - Freg1 = 2.4499GHz at -30dBm
  - Freq2 = 2.4501GHz at -30dBm
  - LO = 2.17GHz at -3dBm
- The HP8593E 22GHz Spectrum Analyzer should be set for a Span of 700kHz, center frequency is 280MHz, with Video Averaging at 100. The IF output port has a narrow band match to  $50\Omega$  and therefore any LO or RF leakage needs to be terminated at the Spectrum Analyzer input. It is recommended that the attenuation of the HP8593E be kept at a minimum of 10dB to provide a wideband  $50\Omega$  termination.
- The HP8593E has an automatic TOI function under the MEAS/USER key. If the distortion terms are close to the noise floor, the automatic TOI function may not capture the distortion peaks. In this case, a manual measurement can be made. Measure the lowest power of the two fundamen-

tals (P1), then measure the highest power of the two 3rd order terms (P3). TOI may be calculate as: ((3P1)-P3)/2.

 Correct for loss in the IF output cable by entering its value in the REF LVL OFFSET under the 2nd menu page of the AMPLITUDE key.

# Receive Mixer Noise Figure

Noise Figure (NF) is the ratio of total noise power at the output to the noise power at the output due to source noise at the input. Noise Figure can be expressed as;

$$NF = P_{NO} / (P_{NI} G_A)$$

This test can be difficult to get the correct result. The test set up is shown in Figure 7. Helpful hints are as follows:

- Care should be taken to minimize the environmental noise by taking measurements in an RF enclosure Screen Room.
- The Bandpass Filter on the noise source is required to produce the Single Sideband Measurement.
- The HP8593E has a Noise Figure (NF) option that will provide as good results as a dedicated noise figure meter.
   The Noise Figure measurement on the HP8593E will also handle the special circumstance of mixer noise figure.
- Good 50Ω match is required on both input and output and for both IF and RF frequencies to kill any reflections that will distort the measurement. A 3dB input pad and a 6dB output pad are the minimum values found to give consistently good results. These pads should be located directly on the evaluation board SMA connectors.
- 50Ω termination caps are required on unused ports of the active channel. For the Receive Mixer NF test, place 50Ω terminations on LNA\_IN and LNA\_OUT.
- Enter the input and output loss corrections into the HP8593E in the Noise Figure mode. Input Loss and Output Loss registers are located under the Main Menu, under the Config Menu's 2nd page, and then under the External Losses key.

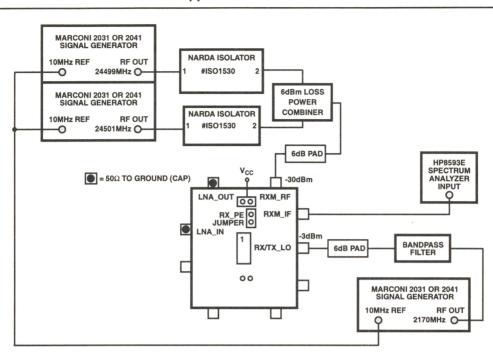


FIGURE 5. HFA3624 RX MIXER THIRD ORDER INTERCEPT

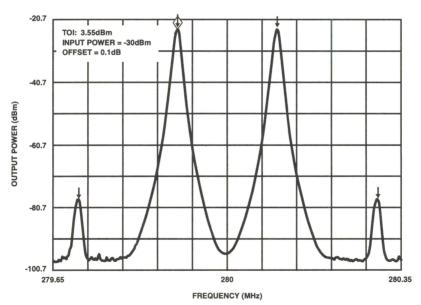


FIGURE 6. TYPICAL THIRD-ORDER INTERCEPT PLOT

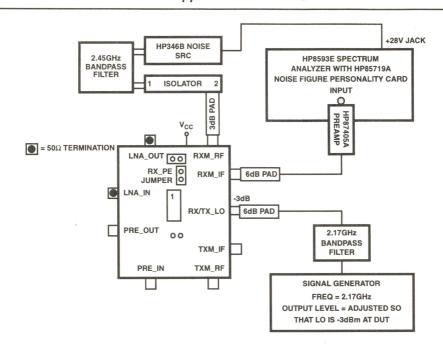


FIGURE 7. HFA3624 RX MIXER NOISE FIGURE SET-UP

# Receive Mixer 1dB Compression Point

Compression Point is the output power in dBm that causes the device gain to drop by 1dB from the gain at low power levels. The 1dB Conversion Compression Point of a Mixer adds the element of frequency conversion. For this test (Figure 8), it is recommended to use the HP8753D Network Analyzer in the Frequency Offset mode. This requires that the rigid coax jumper connected to Channel R be disconnected and the MEAS menu set to Channel R for absolute power measurement. The power accuracy of the HP8753D can be substantially improved with the use of an external Power Meter connected in feedback to the Network Analyzer by means of an HPIB cable and power splitter. The Continuous Mode Power Meter Calibration is available on the HP8753D under the Cal key and allows the power meter to correct each point of input power on every sweep. Although this slows the sweep time, the improved results are well worth the wait. A detail test procedure for 1dB Compression is available upon request.

# Low Noise Amplifier Noise Figure

This test (Figure 9) has a much simpler set up, but care needs to be taken to ensure a noise free environment by taking measurements in an RF Enclosed Screen Room. Eliminate possible reflections by attaching the Noise Source and Preamp directly on the fixture SMA connectors without cables. Terminate unused active ports with  $50\Omega$  caps. The

LNA Noise Figure test may also use the HP346A Noise Source (low noise power) due to the LNA high gain and the lack of need for attenuation pads in the input and output paths to improve match.

# Low Noise Amplifier 1dB Compression

The Low Noise Amplifier Compression Point (Figure 10) uses a similar set of equipment as the Receive Mixer but the set-up is significantly different. No frequency conversion takes place, so Frequency Offset Mode of the HP8753D is left off. The calibration procedure still uses the Continuous Power Meter Cal of each sweep but the MEAS menu is set on S21 providing a relative gain measurement.

# Transmit Channel 1dB Compression

The test setups for the Transmit Mixer and Preamp 1dB Compression point (Figures 11 and 12) are similar in concept to the Receive Mixer and LNA Compression and are provided for reference.

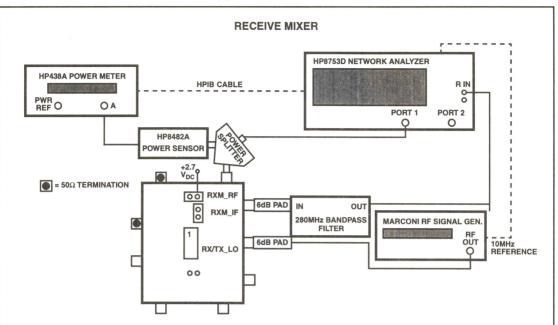


FIGURE 8. HFA3624 RECEIVE MIXER 1dB COMPRESSION TEST SET-UP

#### **LNA AMPLIFIER**

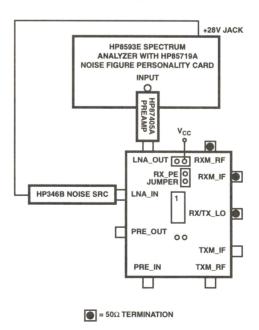


FIGURE 9. HFA3624 LOW NOISE AMPLIFIER FIGURE SET-UP

# HPB753D NETWORK ANALYZER HPB753D NETWORK ANALYZER PORT 1 PORT 2 LNA\_OUT OO RX PEO JUMPER 0 LNA\_IN 1 POWER 95 482A POWER 95 482A

FIGURE 10. HFA3624 LOW NOISE AMP 1dB COMPRESSION TEST SET-UP

#### TRANSMIT MIXER

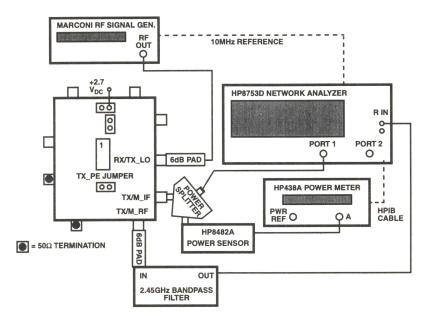


FIGURE 11. HFA3624 TRANSMIT MIXER 1dB COMPRESSION TEST SET-UP

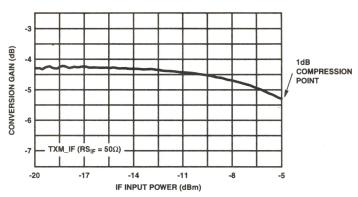


FIGURE 12. TYPICAL TRANSMIT MIXER 1dB COMPRESSION PLOT

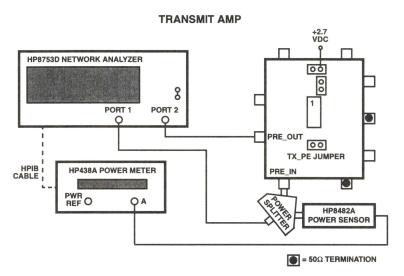


FIGURE 13. HFA3624 TRANSMIT AMP 1dB COMPRESSION TEST SET-UP

# HFA3624 Evaluation Board (REV -5) Parts List

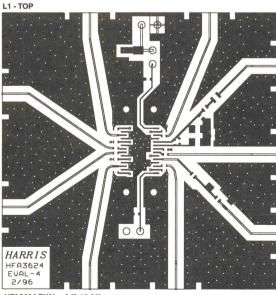
DESCRIPTION	SIZE	VALUE (TOL)	PART#	SOURCE	QTY	DESIGNATION
Banana Plug			39F1531	Newark	2	
PC Switch			SNT100BKT	Deanco	2	JP1, JP2
Posts			TSW11008GS	Deanco	1 (strip)	
Wire			24 Gauge		2 at 18"	
SMA End Launch Conn.			142-701-851	Newark	9	
Chip Resistor	0402	2.0kΩ (1%)	P2.00KLCT-ND	Digikey	1	R6
Chip Resistor	0402	250Ω (1%)	P249LCT-ND	Digikey	1	R5

# HFA3624 Evaluation Board (REV -5) Parts List (Continued)

DESCRIPTION	SIZE	VALUE (TOL)	PART#	SOURCE	QTY	DESIGNATION	
Chip Inductor	0805	68nH (2%)	0805CS-680XGBC	Coilcraft	1	L1	
Chip Inductor	0805	39nH (10%)	TKS2376CT-ND	Digikey	1	L2	
Chip Inductor	0603	12nH (10%)	TKS2346CT-ND	Digikey	1	L3	
Chip Inductor	0805	47nH (10%)	TKS2377CT-ND	Digikey	1	L4	
Chip Capacitor	0402	2.7pF (0.1pF)	GRM36C0G2R7B 050AB	Murata	1	C17	
Chip Capacitor	0402	6.8pF (0.25pF)	MCH155A6R8CK	Garrett	1	C5	
Chip Capacitor	0402	1.5pF (0.25pF)	MCH155A1R5CK	Garrett	1	C25	
Chip Capacitor	0402	5.0pF (0.25pF)	PCC050CQCT-ND	Digikey	6	C8, C9, C14, C15, C16, C22	
Chip Capacitor	0402	10.0pF (0.25pF)	PCC100CQCT-ND	Digikey	2	C20, C28	
Chip Capacitor	0402	200pF (5%)	PCC201CQCT-ND	Digikey	7	C1, C2, C7, C10, C19, C23, C26	
Chip Capacitor	0402	470pF (10%)	PCC471BQCT-ND	Digikey	4	C6, C18, C21, C24	
Chip Capacitor	0805	2200pF (10%)	PCC222BNCT-ND	Digikey	1	C11	
Chip Capacitor	1206	2.2μF (20%)	PCS3225CT-ND	Digikey	1	C13	

#### LAYOUT NOTES:

- 1. Use GETEK PC board material
  - a) Two Internal Ground Planes 10 mils from top and bottom surface.
  - b) Total PC Board Thickness 0.062" to fit End Launch Connector.
- 2. All Microstrip traces 21 mils wide.
- 3. Top Ground Clearance to microstrip trace is 40 mils.



HFA3624.EVAL - 4 (2-16-96)

FIGURE 14.

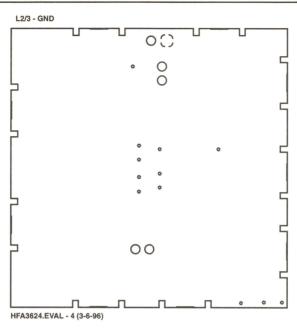


FIGURE 15.

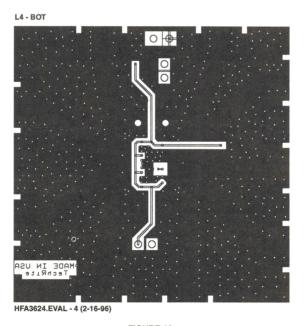


FIGURE 16.

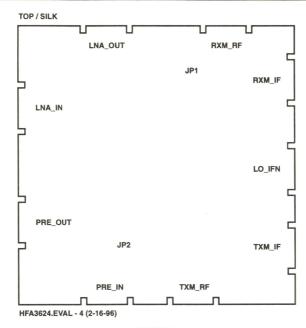
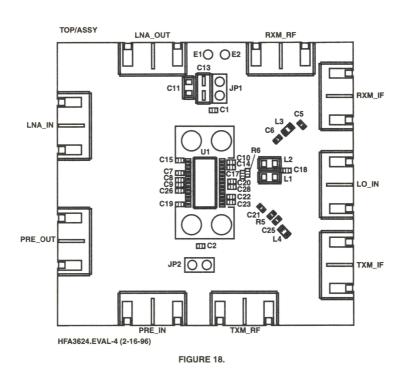
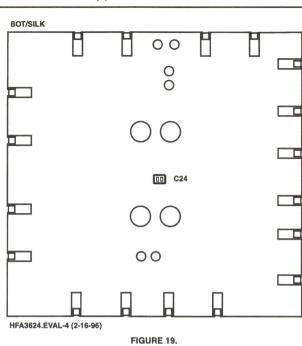


FIGURE 17.



3-64



3-65

# APPROTE

No. AN9622 July 1996

Harris Linear

# Using the PRISM™ HFA3724 Evaluation Board

Author: Raphael L. Matarazzo



#### Introduction

The HFA3724 is a highly integrated IF strip and baseband converter for half duplex wireless data applications. It fea-

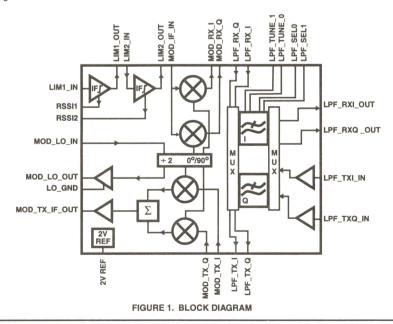
tures all the necessary blocks for baseband demodulation and modulation of "I" and "Q" quadrature multiplexing signals. It targets applications using all phase shift types of modulation (PSK) due to its limiting receiving front end. Four fully independent blocks adds flexibility for numerous applications covering a wide range of IF frequencies. Figure 1 depicts the simplified block diagram of the HFA3724.

The HFA3724 has a two stage integrated limiting IF amplifier with frequency response to 400MHz. These amplifiers exhibit a -84dBm, -3dB cascaded limiting sensitivity with a built in Receive Signal Strength Indicator (RSSI) covering 60dB of dynamic range with excellent linearity. An up conversion and down conversion pair of quadrature doubly balanced mixers are available for "I" and "Q" baseband IF processing. These converters are driven by an internal quadrature LO generator which exhibits a broadband

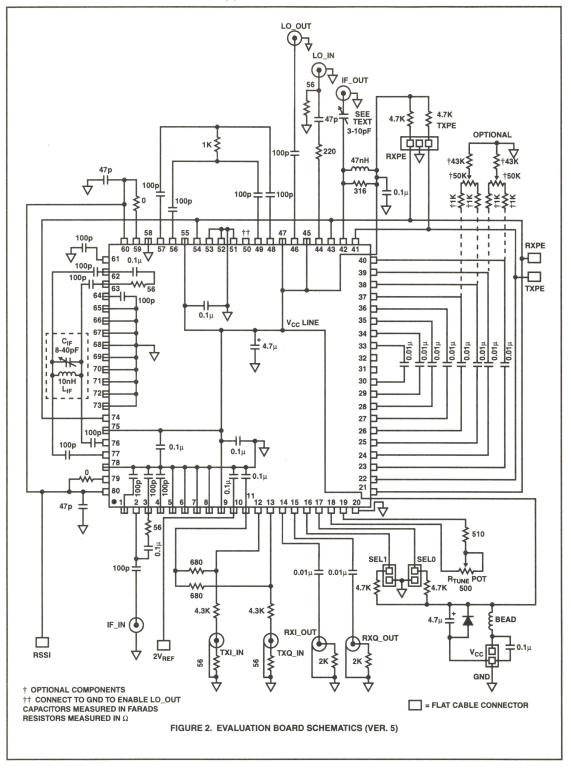
response with excellent quadrature properties. For broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency for modulation/demodulation. A buffered, divide by 2, LO single ended  $50\Omega$  selectable output is provided for convenience of PLL designs. The receive down converter mixers "I" and "Q" outputs have a frequency response up to 30MHz for Baseband signals and the transmit mixers outputs are summed and amplified to a single ended open collector output with frequency response up to 400MHz.

Multiplexed or half duplex baseband 5th order Butterworth low pass filters are also included in the design. The "I" and "Q" filters address applications requiring low pass and antialiasing filtering for external baseband threshold comparison or analog to digital conversion in the receive channel. During transmission, the filters are used for pulse shaping and control of spectral mask.

Four filter bandwidths are programmable, (2.2MHz, 4.4MHz, 8.8MHz and 17.6MHz) via a two bit digital or hardwired control interface. These cut off frequencies are selected and can be fine tuned for optimization of spectrum output responses.



3



# **Board Description**

An electrical schematic of the evaluation board is shown on Figure 2. The typical test diagram shown on page 13 of the HFA3724 Data Sheet has been implemented with few modifications to aid to the evaluation of the device in typical applications.

Pull up resistors to V<sub>CC</sub> of 4.7K have been added to the control pins together with shorting jumpers to ground to facilitate setting up the device into transmit and receive modes as well as the programmable Low Pass Filters.

The IF input to the Limiters is resistively terminated in  $50\Omega$ . This simplifies the matching at the expense of limiter Noise Figure. The NF is approximately 9dB in this configuration as opposed to 6dB in a  $250\Omega$  environment, such as shown in the Typical Application Diagram in the data sheet.

The interstage limiter filter is adjusted to a center frequency of 280MHz by means of an adjustable capacitor.

The receive I/Q outputs are terminated on board with  $2k\Omega$  resistors.

The transmit Digital (TTL) I/Q inputs are terminated on board with  $50\Omega$  A 4.3K and  $680\Omega$  attenuator is built in the evaluation board in case the transmit inputs need to interface with a TTL drive signal with no  $50\Omega$  load capabilities. The  $50\Omega$  chip resistors need to be removed in this case.

The transmit IF output is conveniently matched to  $50\Omega$  at 280MHz with a network with an adjustable capacitor.

Provision has been made to add potentiometers to reduce carrier suppression. These components are not installed.

A potentiometer and a resistor totalling  $1k\Omega$  have been added to the Low Pass Filter fine tuning pins for convenience of the evaluation. The boards have been adjusted for a -35dBc main lobe to side lobe difference by using the selectable 8.8MHz filter tuned low ( $R_{TLINE}$  value is approximately  $900\Omega$ ).

Version 5 layout addresses an option to connect pin 50 (LO\_GND) to ground. This pin has been left disconnected from ground in the present layout. A solder bridge must be placed from pin 50 to pin 51 when the LO\_OUT signal is required.

A flat cable connector is provided when interfacing with the Harris HSP3824 Baseband processor. The RSSI output can be monitored at its respective pin.

Figure 19 and Figure 20 show the access and adjustment points for the evaluation board.

# Evaluation Notes (Version 5)

Proper antistatic procedures must be used when handling the HFA3724 evaluation board.

When testing the receive demodulator sensitivity please remove the transmit baseband digital signals to avoid crosstalk.

Please terminate the LO\_OUT output port into  $50\Omega$  when enabling the LO\_OUT output. Leaving this port mismatched reduces the carrier suppression of the transmit signal.

When evaluating power consumption in stand by mode, please remember that most of the jumpers are pull up resistors which can add up to the total I<sub>CC</sub> when jumpers are placed to ground.

Do not add significant external capacitive loading to the I/Q receive ports. Measure these ports with low capacitance scope probe adapters or high impedance low capacitance vector voltmeter probes. High impedance low capacitance active probes for network analyzers can also be used.

Proper TTL driving capability and rise and fall time balance is important for code leakage evaluation of spread spectrum signals. Make sure that the TTL data inputs are below  $V_{CC}$ .

When interfacing with a HSP3824 evaluation board, make sure that the available HSP3824 board version can provide transmit signals with  $50\Omega$  capability, otherwise remove the two termination resistors from this evaluation board (HFA3724EVAL).

The pot R<sub>TUNE</sub> can assume very low values when evaluating the tuning range. It is advisable to contain this value within a  $\pm 30\%$  of the center value. Too low values can cause power up problems to the LPF biasing scheme. The resistance value can be read with an ohmmeter when the device is turned off.

## **Evaluation Description**

#### **DEMODULATOR TESTS**

#### **Demodulator Sensitivity Tests**

Please refer to Figure 5A and Figure 5B for a simplified block diagram and typical test set up. The evaluation board is set to Receive by placing a shorting jumper to the RX pins. The LPF filter setting (SEL0, SEL1) is to be set according to the desired baseband frequency of operation as explained below

A signal generator is connected to the IF\_IN SMA input and set to a CW frequency of 280MHz. This generator is used to provide a simulated IF input signal to the device. In case the generator is not capable of accurate low RF output levels, a step attenuator can be used at its input in order to accurately provide very small RF levels to the HFA3724 IF input. Note that the IF input frequency is set to the center of the intermediate bandpass filter frequency set in the evaluation board by  $L_{\rm IF}$  and  $C_{\rm IF}$  as in the board schematics, Figure 2.

A second signal generator is connected to the LO\_IN port to provide the local oscillator frequency. This input frequency must be always twice the reference LO frequency and will be referred as 2XLO for most of this document. As the "I" and "Q" baseband outputs frequency is dependent on the difference in frequency of the ref LO and the IF input, the user can choose any desired 2XLO frequency such that absolute difference in frequency between the ref LO and the IF input is within the baseband of the LPF filter.

Because the 2XLO input port is broad band (10MHz to in excess of 820MHz), all LPF filter settings can be evaluated. As in the example of Figure 5B, the LO input frequency has been chosen to be of 286MHz (2XLO of 572MHz) as high-

side injection (LO higher than the IF frequency) and the "I" and "Q" outputs frequency is of 6MHz. A LPF setting of 8.8MHz (SEL1 = High - no jumper and SEL0 = Low - shorting jumper) can then be used.

#### Limiter Output Test: Optional

One of the features of the high gain IF limiter chain is its stability and spur free spectrum. The limiter chain output can be tested by probing one of the outputs of the second limiter (pin 56 or 57) by using a high frequency very low capacitance AC coupled resistive probe like a HP54006A. The evaluation board itself does not provide a simpler hook up for this test as degradation of signal could occur.

The probe resistive impedance is of  $1k\Omega$  and can be connected to a spectrum analyzer for evaluation of spectrum purity and sensitivity. Figure 3A and Figure 3B show typical spectrum responses of the limiter amplifier chain with input signals of -90dBm, -70dBm and -50dBm at 280MHz respectively. Notice the "bump" created by a bandpass action of the intermediate band pass filter ( $L_{\rm IF}, C_{\rm IF}$ ) and resulting noise bandwidth amplification. As limiting starts to occur as in Figure 3B, the noise floor level is decreased accordingly (Limiter action on noise).

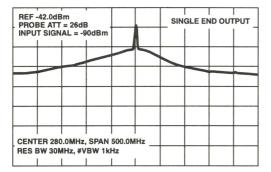


FIGURE 3A. LIMITER OUTPUT SPECTRUM IF = -90dBm

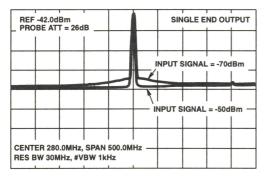


FIGURE 3B. LIMITER OUPUT SPECTRUM IF = -70dBm, -50dBm

With an "I" and "Q" output frequency of 6MHz and a LPF setting of 8.8MHz, the user can start with a IF signal of -30dBm at 280MHz and observe both "I" and "Q" outputs with a oscilloscope or spectrum analyzer with a high impedance probe. The output signals must be in quadrature. (90 degrees apart) and with a level of approximately 500mV<sub>P-P</sub>. When decreasing the IF input signal, to -50, and -70dBm, these "I" and "Q" signals must keep the same amplitude due to the limiting action of the IF limiting amplifiers. Further reduction of the IF input will show some decrease in the "I" and "Q" amplitudes up to the -3dB point where the 3dB sensitivity occurs. It is important to note that at very low level IF input signals these outputs will show a little smearing as observed in a oscilloscope. The use of a spectrum analyzer will improve the -3dB sensitivity measurement. It is also important to note that because the intermediate IF filters are set as wide band, (approximately 47MHz) some output noise energy starts to propagate to the "I" and "Q" outputs during this sensitivity evaluation.

#### **Demodulator Quadrature Tests**

As in the sensitivity test, the "I" and "Q" outputs as observed in a oscilloscope, or a vector voltmeter, will be in quadrature (where their phase relationship is of 90 degrees) with any reasonable IF input levels beyond sensitivity.

NOTE: For High-Side injection (ref LO higher than the IF frequency) the "I" channel leads the "Q" channel by 90 degrees. For Low-Side injection (548MHz 2XLO or 274MHz ref LO as in our example), the "I" channel lags the "Q" channel by 90 degrees.

A vector voltmeter can be used to evaluate the phase difference or phase balance as well as the amplitude balance of the 'I" and "Q" channels for various IF input levels.

When performing these tests and moving the LO frequency for different "I" and "Q" output frequencies, the user will observe what seems to be a distortion in the output signals when these frequencies are well below the 3dB roll off characteristics of the HFA3724 LPF filters. This apparent distortion is a result of the LPF response to a limited output which resembles a square wave (hyperbolic tangent function). In our example of a 6MHz output and a LPF filter setting of 8.8MHz, the outputs look sinusoidal.

#### Low Pass Filter Tests

These tests shall be performed by using a vector voltmeter or a spectrum analyzer. Both instruments lock in the fundamental frequency of the "I" and "Q" outputs where accurate 3dB roll off characteristics must be tested.

All LPF settings can be tested by varying the 2XLO frequency generator accordingly. The user need to use caution for very low frequency "!" and "Q" signals because of the use of coupling capacitors in the evaluation board from the down converter mixers to the LPF input and from the LPF output to the on board  $2k\Omega$  resistor load. These components create a high pass filter action with a 3dB point of approximately 15kHz for  $0.01\mu F$  decoupling capacitors.

An indirect method of the 3dB LPF filter evaluation is by setting a reference signal to the vector voltmeter at 1MHz for example (562MHz 2XLO as in our example). This level corresponds to a 0dB when this reference signal is saved in the voltmeter. Increasing the 2XLO frequency in fine steps will start moving the reference down until the vector voltmeter reads -3dB. This frequency setting (2XLO) is divided by 2 and subtracted from the IF frequency of 280MHz (for example) to find the 3dB point of the LPF filter. Note: Some vector voltmeters cannot scan or keep probe amplitude calibration for different frequencies and errors can occur.

As all LPF filter settings (2.2, 4.4, 8.8 and 17.6MHz) are slightly different from each other, it is suggested to calibrate a new reference 1MHz signal for each of the desired settings.

Another method of low pass characteristics evaluation is by using a network analyzer. Although a little more complicated, this method is useful to evaluate the overall group delay characteristics of the Demodulator at all LPF settings and will be explained later in this section.

#### **RSSI Tests**

The RSSI characteristics of the HFA3724 can be evaluated by monitoring the voltage level at the RSSI output pin available in the evaluation board. This pin is located and labelled in a flat cable connector used to interface with the Harris HSP3824 Base Band Processor.

The CW IF input level is varied from -90dBm to 0dBm for example, in steps, and the corresponding voltages in the RSSI output can be monitored and recorded. A typical RSSI output curve is depicted in Figure 4.

The RSSI output pin is sensitive to long wire loops as it can generate signal feedback to the IF input. This situation can lead to possible oscillation or increase in spurs from the IF amplifier outputs. Use caution when using long lead voltmeter probes at this pin. When performing the limiter output spectrum check earlier in this section, the user can make an assessment of the sensitivity of the RSSI line by placing and removing lead voltmeter wires at the RSSI test point.

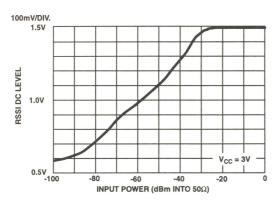


FIGURE 4. TYPICAL RSSI RESPONSE

The HFA3724 RSSI outputs are a sum of the two current outputs of each of the limiters. These current sources have been summed together through two on chip  $6k\Omega$  resistor in parallel. Zero ohm resistors have been added to feed the current outputs to the respective resistor pins (pins 60 and 80).

The user can modify the voltage range when required, by having the two current outputs summed through a different resistor value.

#### **Demodulator Group Delay Characteristics**

Group delay and filter passband characteristics can be evaluated by a network analyzer by using a set up as in Figure 6.

The network analyzer generator sweep baseband signal is upconverted to an IF signal by a doubly balanced mixer. The IF signal is a double side band suppressed carrier signal contrary to a CW signal as in the previous sensitivity tests paragraphs. This DSB signal can be conveniently used for the "I" and "Q" evaluation individually when a proper phase shift technique is used. The doubly balanced mixer must have a reasonably RF input frequency response down to a few hundreds of kilohertz and good passband characteristics across a 40MHz bandwidth which is very common for broad band diode mixers. The network analyzer generator output is split between its reference input "R" and the RF port of the mixer. A 280MHz signal generator is used for the LO input of the mixer and also as a reference LO for the HFA3724. The 2XLO signal for the LO\_IN input of the device is generated by an off the shelf frequency doubler (a second generator locked to the 280MHz generator is not suggested unless they have very good phase lock characteristics). The output of the frequency doubler is routed through a line stretcher for phase shift control.

Mathematical manipulation of a double side band input signal and the response of a quadrature demodulator suggests a phase relationship between the LO and the input signal such that one and only one of the outputs "I" and "Q" signals is present. The line stretcher is used to cancel the channel not being evaluated.

The outputs "I" and "Q" result from the following trigonometric equations:

 $I = 1/2\cos(w_m t - \Theta) + 1/2\cos(w_m t + \Theta)$  and

 $Q = 1/2\sin(w_m t - \Theta) - 1/2\sin(w_m t + \Theta)$ 

Where  $w_m$  is the network analyzer frequency in radians and  $\Theta$  is the phase shift between the IF input and the LO signal. In the case of a full "l" signal, the phase  $\Theta$  needs to be zero. For a full "Q" signal, the phase  $\Theta$  needs to be of -180 degrees.

The "T" channel of the network analyzer is used to monitor the "I" or the "Q" channel output. The analyzer T/R ratio for magnitude and phase responses from 500kHz to beyond the 3dB points can be displayed. Some network analyzers can also compute the group delay automatically. A typical Group delay and frequency response characteristic is depicted in Figure 7A and Figure 7B.

Group delay and 3dB response balance between "I" and "Q" output signals can also be evaluated when desired.

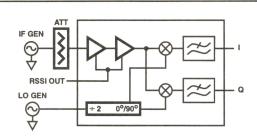


FIGURE 5A. SIMPLIFIED DEMODULATOR BLOCK DIAGRAM

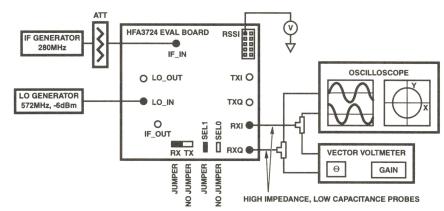


FIGURE 5B. TYPICAL TEST SETUP

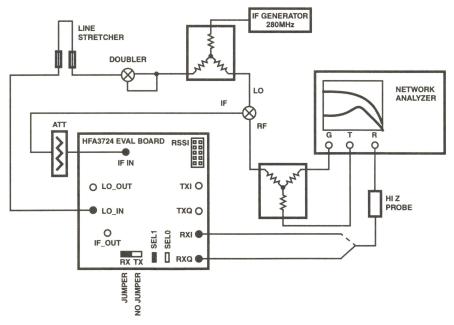


FIGURE 6. EVALUATING DEMODULATOR LPF CHARACTERISTICS AND GROUP DELAY

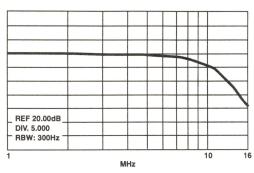


FIGURE 7A. TYPICAL LPF AMPLITUDE RESPONSE AT 8MHz

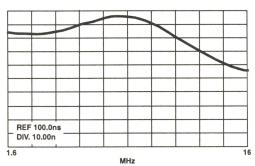


FIGURE 7B. TYPICAL DEMODULATOR GROUP DELAY AT 8MHz

#### **MODULATOR TESTS**

#### **Single Side Band Characteristics**

Please refer to Figure 9A and Figure 9B for a simplified block diagram and a typical test set up. The evaluation board is set to Transmit by placing a shorting jumper to the TX pins. The LPF filter setting (SEL0, SEL1) is to be set according to the desired baseband frequency of operation.

One of the figures of merit of a Vector or Quadrature Modulator is its the SSB characteristics. Phase and amplitude balance characteristics of this type of modulator are combined and are reflected directly into how good a sideband is suppressed. By using two accurate 90 degrees apart (cosine and sine) input signals into the "I" and "Q" baseband inputs, a quadrature modulator will output a single side band signal. Simple trigonometric mathematical manipulation of these signals (Baseband and Carrier or LO) yield a suppressed side band from the classical dual side band signal generated by multiplication, in a single mixer, of a Carrier (LO) and a modulating signal. The same concept can be used to prove that if the baseband signals are in phase, a dual side band, suppressed carrier output signal is generated by a quadrature modulator.

Another important consideration is carrier suppression, which is often referred as LO leakage. This parameter does not depend on amplitude and phase characteristics of a quadrature modulator but is a result of how well balanced are the upconverter mixers. This check is also carried out during the SSB tests.

The HFA3724 Modulator "I" and "Q" baseband inputs are TTL compatible i.e., they are equivalent to comparator inputs which output square waves before any filtering takes place. In other words, the baseband signals for testing the device have to be TTL compatible. 90 degrees apart TTL signals with a very accurate phase relationship must be generated in order to evaluate the device for single side band characteristics. As square waves are composed of the fundamental and odd harmonics, all previous math concepts are still valid for square wave signals.

#### Choice of LPF

The transmit low pass filters are used to preshape the comparator output square waves as desired by the user, therefore bandlimiting the output signal due to the frequency translation during upconversion. The LO signal, now referred as a "Carrier" is also generated by the 2XLO input. The choice of the LPF is made based upon which baseband frequency is to be upconverted such that a desired pre shaping takes place. Figure 8A and Figure 8B show a typical SSB output for two 90 degrees apart 5MHz square wave signals. Only the fundamental of the square wave signal is depicted in Figure 8A as the LPF filters take care of attenuating their harmonics.

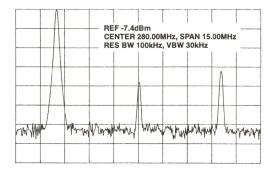


FIGURE 8A. NARROW SPAN SSB CHARACTERISTICS

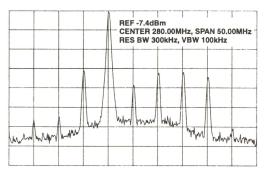


FIGURE 8B. WIDE SPAN SSB CHARACTERISTICS

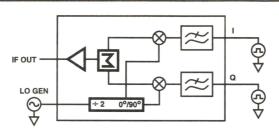


FIGURE 9A. SIMPLIFIED MODULATOR BLOCK DIAGRAM

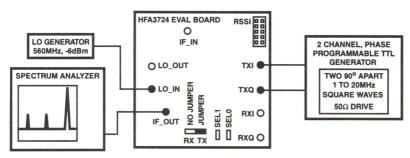


FIGURE 9B. TYPICAL MODULATOR TEST SET UP

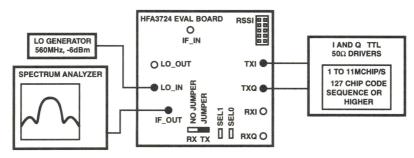


FIGURE 10. SPREAD SPECTRUM CHARACTERISTICS TEST SET UP

Carrier suppression as in Figure 8A is typically better than Figure 13 of the data sheet as the evaluation board does not make use of the LO buffer (Pin 50 is left floating). The built-in capability of the buffer causes a little carrier suppression degradation due to the high currents involved driving a  $50\Omega$  load.

NOTE: The HFA3724 modulator generates a lower sideband signal when the "I" input LEADS the "Q" input by 90 degrees.

During the SSB evaluation the user can change the square wave frequency and LPF filters setting, and observe the spectrum showing the typical bandpass filtering actions by a change in the "plateau" of noise floor. The user can also

observe the attenuation of the harmonically related spectrum lines generated by a square wave when the fundamental lies within a desired passband (Figure 8B).

#### Transmit LPF Evaluation by Spread Spectrum Signals

The spread signal test set up is depicted in Figure 10.

The LPF filter characteristics can also be evaluated by a network analyzer with a test set up to be explained later. As the LPF filters are multiplexed between Transmit and Receive, most of the data like 3dB points and group delay characteristics are similar when compared by the tests performed for the Receive section.

In transmission applications, modulators and shaping filters need to be evaluated by the spectral response or spectrum shaping characteristics which include any nonlinear behavior across the transmitting chain. In the case of the HFA3724, non linearities of both the LPF filters and the Up conversion mixers responses can be evaluated by using a spread sequence input which shows any abnormal spectral regrowth and expected pulse shaping characteristics. Band limiting action and related spectrum shaping tunability can be exercised during these tests.

A long length spread sequence TTL I/Q generator, higher than 2<sup>11</sup>-1 or 2047 in length can be used to display a good spread characteristic when observed by a spectrum analyzer. The side lobe to main lobe attenuation resulting from the LPF shaping can then be monitored. The user have the option here to use the Harris HSP3824 evaluation board as a suitable I/Q generator without any data at its input as the signal accordingly (the Spectrum shape looks just a little different than the ones depicted by Figure 11). Please refer to the HSP3824 Evaluation board application note.

The main lobe width of this signal is always twice the baseband frequency used for the "I" or "Q" signals whether they are in phase (same signal) or independent from each other as in quadrature input signals. The expected next upper and lower side lobes have a width of exactly the frequency of the baseband signals and have its peak dependent of the LPF characteristics and any nonlinearity in the chain. The LPF fine tuning characteristics can be evaluated by changing the value of  $R_{\rm TLINF}$  from  $\pm 20\%$  from its nominal value.

Figure 11 shows a typical 11Mchips/s (11MHz) "I" and "Q" signal spread signal output spectrum and the spectrum shape variation when both LPF settings and R<sub>TUNE</sub> are changed. Figure 11A shows the output spectrum of this signal with the highest setting of 17.6MHz (LPF17.6). Notice that little or no pre-shaping is taking place at that frequency and the spectrum resembles closely a sinx/x response. Figure 11B and Figure 11C show the variation of the sidelobe to main lobe characteristic for a R<sub>TUNE</sub> variation of  $\pm 10\%$  with the nominal setting of 8.8MHz (LPF8.8). Figure 11D shows the spectrum shape in case the 4.4MHz setting is used and R<sub>TUNE</sub> is set for a frequency higher than 4.4MHz.

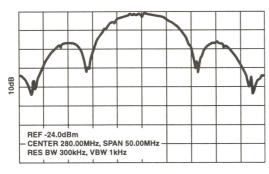


FIGURE 11A. SPREAD SPECTRUM RESPONSE AT LPF17.6 FOR AN 11MCHIPS/S BASEBAND SIGNAL

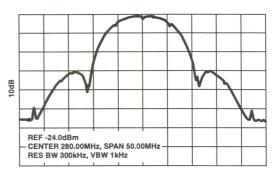


FIGURE 11B. RESPONSE AT LPF8.8, R<sub>TUNE</sub> TUNED LOW (11MCHIPS/S)

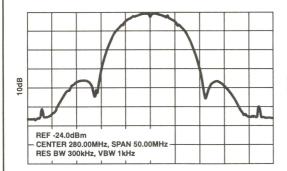


FIGURE 11C. RESPONSE AT LPF8.8, R<sub>TUNE</sub> TUNED HIGH (11MCHIPS/S)

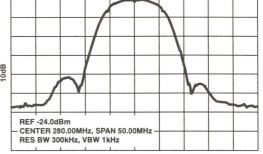


FIGURE 11D. RESPONSE AT LPF4.4, R<sub>TUNE</sub> TUNED HIGH (11MCHIPS/S)

#### Transmit LPF Characterization by a Network Analyzer

Because the "I" and "Q" filtered transmit baseband signals are not readily available to be tested in the evaluation board unless a differential probe is used at the output of the LPF filters, an indirect method as depicted in Figure 14 can be used. The TTL signal need to be generated by a comparator/buffer combination circuit that is fed by the network analyzer generator. This TTL signal will sweep as desired by the user. Only one of the channels must be evaluated at the time due to the summing of the upconverted "I" and "Q" signals. It is important to note that the input of a baseband signal of either "I" or "Q" by itself will generate a dual side band signal at the HFA3724 output. This dual side band signal is down converted back to the baseband by an external broad band doubly balanced mixer. The main restriction for the external mixer is its IF output frequency response which should cover from 500kHz and up. The external mixer receives its LO input from a 280MHz CW signal generator. The HFA3724 output signal is mixed down by this external mixer vielding a baseband signal to be monitored by the network analyzer. The HFA3724 2XLO is also generated by a doubler from the same 280MHz CW generator. Again, proper phase shift between the external 2XLO signal and the external mixer LO is required for proper operation of the down conversion process from a dual side band signal. A line stretcher is used and adjusted after the frequency doubler for maximum reading of the external mixer IF output.

#### **Other Test Setups**

Although most of the test set ups described earlier can evaluate the performance of the HFA3724, the reader is welcome to evaluate the device in a more system oriented manner with the common test procedures that follow:

Figure 15 depicts a common QPSK demodulation test set up for the HFA3724 using a Vector Signal Generator at a 280MHz carrier frequency, modulated by a spread digital sequence (Again, the HSP3824 evaluation board is more than suitable for this data generation). Coherence between the Carrier generator and the HFA3724 is done by the use of a line stretcher for the 2XLO signal and by tying the reference 10MHz signals often offered by these equipments. A modulation analyzer can be used for displaying the constellation characteristics and eye diagram results of the demodulation process. Figure 12 shows a typical Baseband QPSK constellation (Vector States) as the input to the Vector modulator used in Figure 15.

Figure 13A and Figure 13B depicts the constellation and eye diagram of the device for a 11MHz symbol rate with the LPF8.8 filter setting at 8MHz. The Carrier generator output signal has been set to -60dBm.

Another method, more realistic, which accounts for prefiltering before transmission (spectrum shaping) is using a second HFA3724 evaluation board as the generating signal carrier (The reader may ask "Why not use the same board in analog loop back mode?" As the LPF filters are multiplexed between Transmit and Receive and the ref LO is the same, this application is not possible).

Figure 16A shows a Modulation/Demodulation test setup. Figure 16B depicts the same set up by using the HSP3824



FIGURE 12. TYPICAL 11MHz QPSK BASEBAND CONSTELLATION



FIGURE 13A. HFA3724 DEMODULATOR OUTPUT CONSTELLATION

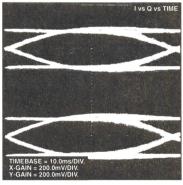


FIGURE 13B. HFA3724 DEMODULATOR EYE PATTERN

evaluation board as the baseband generator. Again, synchronization or coherence is needed for proper evaluation. Contrary to a vector generator, which can have its output level well controlled, it is necessary to provide an attenuation path (attenuator) from the output of the HFA3724 transmitting board to the IF input of the receiving board for sensitivity level evaluation. (The output signal is approximately -7dBm.)

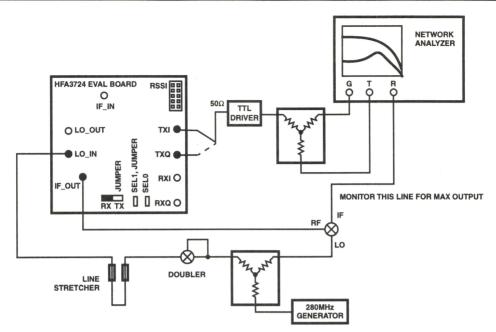


FIGURE 14. EVALUATING MODULATOR LPF CHARACTERISTICS AND GROUP DELAY

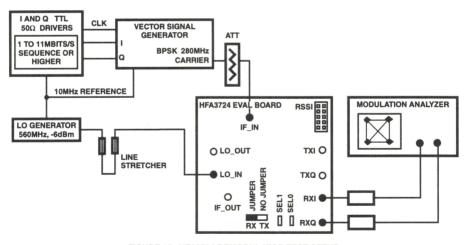


FIGURE 15. HFA3724 DEMODULATOR TEST SETUP

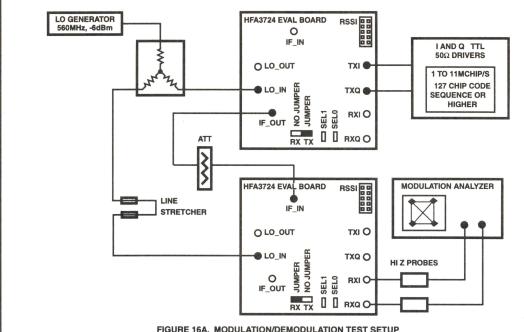
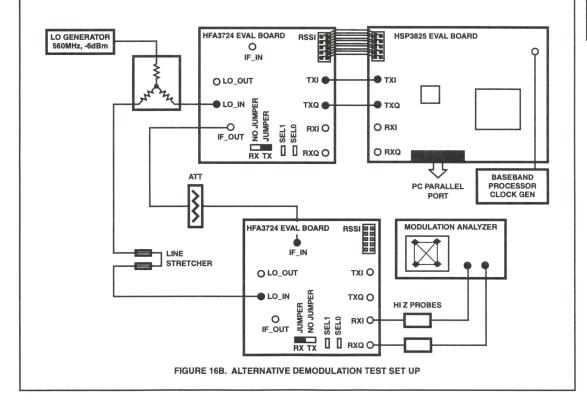


FIGURE 16A. MODULATION/DEMODULATION TEST SETUP



Figures 17A and 17B show the Constellation and Eye diagram for the set up of Figure 16A at 11MHz symbol rate (QPSK). Notice the impact on both diagrams when spectral shaping is required at the transmit output.

Figure 18 setup is used for BER testing using two HFA3724 evaluation boards and one full duplex HSP3824 evaluation board.

The output signal from the Transmitting board can be summed with noise and bandlimited for proper Eb/No or C/N evaluation versus BER. Please refer to the HSP3824 application notes.

#### **Final Comments**

The HFA3724 evaluation board is shipped and tuned for an IF of 280MHz at the output of the Modulator. The interstage limiter

TIMEBASE = 10 0ms/DIV.

VECTOR
Q vs I

TIMEBASE = 10 0ms/DIV.
X-GalN = 100 0mv/DIV.
Y-GalN = 100 0mv/DIV.

band pass filter has also been tuned for a 280MHz center frequency and 47MHz of bandwidth. Modifications to the evaluation board for different IF frequencies and bandwidths are very straightforward (Please refer to the HFA3724 data sheet for IF bandlimiting component calculations and S22 data for the IF modulator output). Data rates and data formats must be carefully analyzed when dealing with coupling capacitors between each one of the HFA3724 stages. A compromise of TX/RX switching times and high pass characteristics of these coupling schemes need to be assessed for proper operation of the device depending on the final application. High value coupling capacitors are used for low data rates with the expense of switching times although the HFA3724 has keep alive circuits to hold fixed DC levels to both ends of the coupling capacitors.

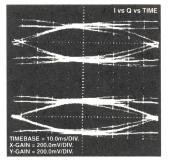
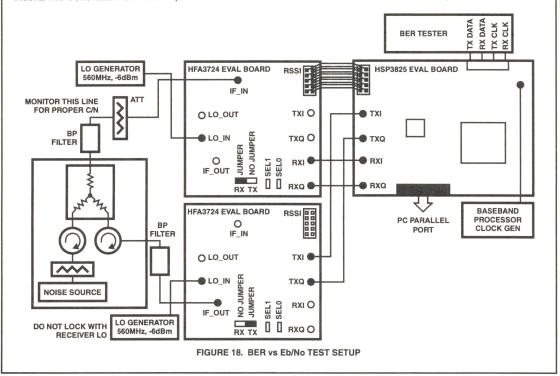


FIGURE 17A. CONSTELLATION DIAGRAM, SETUP OF FIGURE 16A FIGURE 17B. CONSTELLATION DIAGRAM, SETUP OF FIGURE 16A



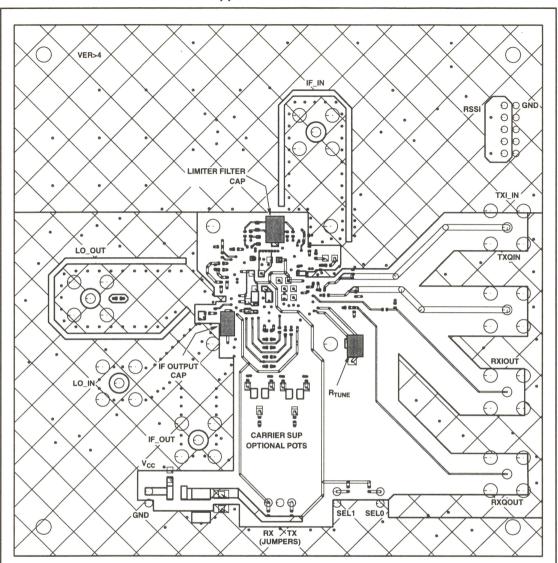


FIGURE 19. HFA3724 EVALUATION BOARD COMPONENT SIDE. USER ACCESS TO ALL PORTS AND ADJUSTMENTS

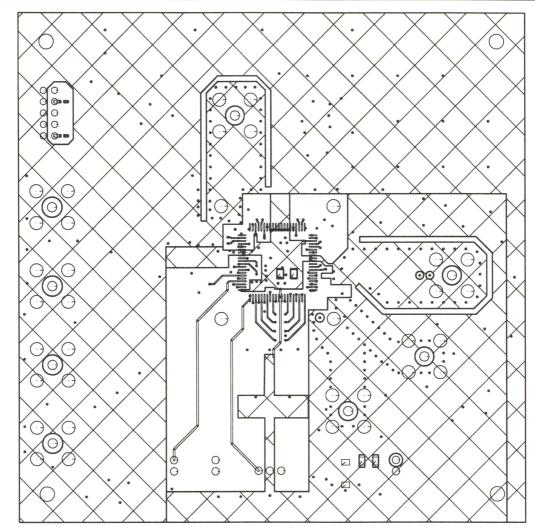


FIGURE 20. HFA3724 IC SIDE

#### HFA3724 VER. 5 EVALUATION BOARD PARTS LIST - 6/1/96

PART NUMBER	DESCRIPTION	MFG/VENDOR	TOTAL
PCC470CQCT-ND (0402)	CAP, FXD, 47pF NPO	PANASONIC/DIGIKEY	3
PCC101CQCT-ND (0402)	CAP, FXD, 100pF NPO	PANASONIC/DIGIKEY	15
PCC103BQCT-ND (0402)	CAP, FXD, 0.01μF X7R	PANASONIC/DIGIKEY	10
MC-104M50-7U08-NI (0805)	CAP, FXD, 0.1μF	NIC COMPS/PRIDMORE	9
ECS-T1CY475R	CAP TANT, 4.7μF	PANASONIC/DIGIKEY	2
TZC03 R100A110	CAR VAR, 3-10pF	MURATA/NEWARK	1
GKG40067-07	CAP, VAR, 8-40pF	SPRAGUE-GOODMAN/DIGIKEY	1
ERJ-2GEJ0.0 (0402)	5% RES, FXD, 0Ω	PANASONIC/DIGIKEY	2

#### HFA3724 VER. 5 EVALUATION BOARD PARTS LIST - 6/1/96

PART NUMBER	DESCRIPTION	MFG/VENDOR	TOTAL
ERJ-2GEJ56 (0402)	5% RES, FXD, 56Ω	PANASONIC/DIGIKEY	4
ERJ-2GEJ220 (0402)	5% RES, FXD, 220Ω	PANASONIC/DIGIKEY	1
ERJ-2GEJ510 (0402)	5% RES, FXD, 510Ω	PANASONIC/DIGIKEY	1
ERJ-2GEJ560 (0402)	5% RES, FXD, 560Ω	PANASONIC/DIGIKEY	3
ERJ-2GEJ680 (0402)	5% RES, FXD, 680Ω	PANASONIC/DIGIKEY	2
ERJ-2GEJ1K (0402)	5% RES. FXD, 1K	PANASONIC/DIGIKEY	1
ERJ-2GEJ2K (0402)	5% RES, FXD, 2K	PANASONIC/DIGIKEY	2
ERJ-2GEJ4.3K (0402)	5% RES, FXD, 4.3K	PANASONIC/DIGIKEY	2
ERJ-2GEJ4.7K (0402)	5% RES, FXD, 4.7K	PANASONIC/DIGIKEY	4
RK73H1J-316 (0603)	1% RES, FXD, 316Ω	KOA/GARRET	1
EVM-1SSX50B501	ΡΟΤ- 500Ω	PANASONIC/DIGIKEY	1
LL1608-F10NK (0603)	IND, FXD, 10nH	TOKO/DIGIKEY	1
LL2012-F47NK (0805)	IND, FXD, 47nH	TOKO/DIGIKEY	1
EXC-CL3225U	SURFACE MT FERRITE BEAD	PANASONIC/DIGIKEY	1
DL4001	DIODE, RECT	DIODES INC/DIGIKEY	1
142-0701-211	WIDE-BODY CON-RCPT SMA	EFJOHNSON/NEWARK	4
142-0701-321	WIDE-BODY CON-RCPT, SMA (RIGHT ANGLE)	EF JOHNSON/NEWARK	4
MHB10G-ND	10 POS ST SHROUDED HEADER	3M/NEWARK	1
TSW-120-08GS	DEL POST TERMINAL PINS	SAMTEC/DEANCO	3
TSW-1 20-08GS	TERMINAL PINS	SAMTEC/DEANCO	1
SNT100BKT	SHORTING BAR FOR POSTS	SAMTEC/DEANCO	3
HFA3724	IC	HARRIS	1
HFA3724 VER.4	PC BOARD	AVANTI	1
ERJ-2GEJ1K (0402)	5% RES, FXD, 1K	PANASONIC/DIGIKEY	4 (Note)
ERJ-2GEJ43K (0402)	5% RES, FXD, 43K	PANASONIC/DIGIKEY	2 (Note)
ST5W503CT-ND	POT 50K	MEPCOPAL/PHILIPS/DIGIKEY	2 (Note)

NOTE: Indicates optional component may be used.

# M APROTE

No. AN9623 July 1996

# Harris Wireless Products

# Packet Error Rate Measurements Using the PRISM™ Chip Set

Author: John Fakatselis



## ™ Introduction

The Harris PRISM chip set has been designed to be used for both continuous and packetized data transmission applications.

System designers need the capability to evaluate and test the radio performance under their operating environments and by using their own transmission method and protocols. In the case of continuous transmission testing, there are commercially available Bit Error Rate (BER) testers that can be utilized to perform the required evaluation tests.

In contrast when it comes to packetized data evaluation, the availability of Packet Error Rate (PER) testers, to test a packetized radio, are not as readily available. In most cases the system evaluators are designing custom test beds to accomplish these performance measurements. This application note is an attempt to provide some guidance of how to design a PER test environment for the PRISM radio.

# Test Bed Description

The Test bed required is comprised of a TX and an RX set of PRISM radios, a PER Tester (PERT) and any other noise and interference equipment as required for the emulation of the channel environment. Figure 1, illustrates this top level test bed configuration. The focus of this note is to explore some possibilities for a custom designed PER tester.

The function of the tester is to generate the desired data packets at baseband (digital Data) and feed them to the PRISM radio for transmission through an interface with the PRISM HSP3824 Baseband Processor. The TX PRISM radio will transmit the packet through the channel. The RX radio will demodulate the baseband packet, which will be transferred to the PER tester via the HSP3824 interface. The PER tester will detect any errors within the received packets. In addition the PERT should be able to report any dropped transmitted packets that were not acknowledged at the receiver. These dropped packets will also be accounted as part of the PER measurement.

The test bed includes an interference source to add noise and interference at RF to accomplish the PER measurement as a function of SNR.

#### Test Packets

The format of the test packets to be transmitted must always have one of the formats as described in the HSP3824 data sheet. All of the packet formats include a preamble field, header fields, and data.

The preamble is programmable and can be up to 256 symbols long. The preamble is used for initial PN synchronization of the receiver.

The header can consists of various fields depended on the desired protocol mode. The header always includes the Start Frame Delimiter (SFD) field. This is true under any mode of

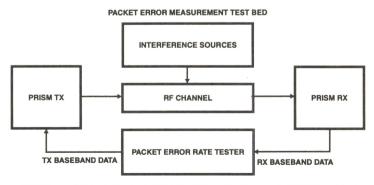


FIGURE 1. PRISM PER MEASUREMENTS TOP LEVEL TEST BED CONFIGURATION

operation. Other fields are optional per the mode in use. There is also a choice to either protect the header fields with CRC or not.

The PERT will be responsible for generating and appending the data portion of the packet to the preamble and header fields.

The example of this note will expand on the simplest possible header format that the HSP3824 is capable of self-generating. This format is shown on Figure 2, and it consists of the preamble bits and the SFD header field immediately followed by the externally provided data.

The transmit side of the PER tester generates the data, controls the data length and the packet transmission rate.

The receive side of the PER tester adds the number of errorless messages received for comparison with the number of actual packets transmitted to derive a PER performance figure.

# PER Tester Description

The PERT functional block diagram is illustrated in Figure 3. The PER functions are grouped into the TX, RX and modem interface functions.

The test philosophy requires that the data sent by the PER tester includes a CRC check field. The CRC is checked at the RX and it either declares a successful packet reception or a packet in error. If for some reason the packet is never seen at the receiver then the PER tester should be able to account for the missed packet. The PER tester should also be able to control the packet length and the frequency (rate) of the transmissions. The PER tester maintains a count of the transmitted vs. the successfully received packets. These counts will be used to calculate the PER performance of the experiment.

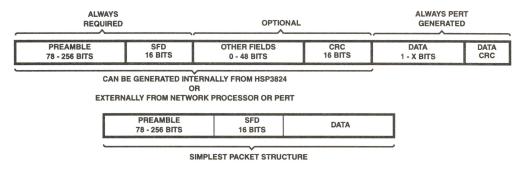
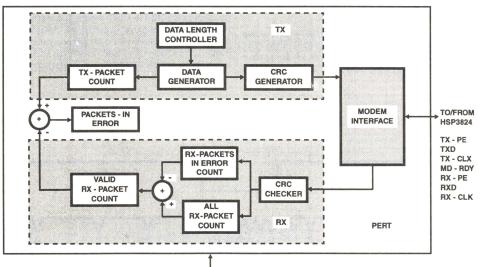


FIGURE 2. PACKET FORMAT DESCRIPTION



PULSE GENERATOR INPUT
(OPTIONAL TO GENERATE TX - PE AND CONTROL PACKET TRANSMISSION)

FIGURE 3. PERT TOP LEVEL BLOCK DIAGRAM

#### Modem Interface

The PERT is required to send the transmit packet to the PRISM radio and also to receive the demodulated received packet from the radio. The PERT will interface directly with the HSP3824 PRISM Baseband Processor. Details of the HSP3824 interface requirements are described in the HSP3824 data sheet. A timing diagram of the TX and RX interfaces are shown on subsequent figures of this note. The TX\_PE signal initiates the transmit operation of the radio. The actual rate and duty cycle of this signal will define the rate of packet transmission, as well as the length of the transmitted packet size. As shown on Figure 4. TX PE envelops the preamble, header and the packet data. The TX\_PE line can be driven directly from an external, off the shelf, pulse generator with a programmable duty cycle. The programmable pulse generator will provide a variety of packet lengths and transmission rates to adequately evaluate the radio performance.

#### **TX Function**

The PERT TX functions include the data generator, the data length controller, the CRC generator and the TX packet counter.

The data generator outputs the test data that needs to be appended to the header. The interface signal TX\_RDY indicates to the PER tester when it should start sending the data through the HSP3824 interface. The timing is shown on Figure 5. More details of this interface are described in the HSP3824 data sheet.

The data generator uses the data length defined by the data length controller. The data length controller can be simply a register that is programed to indicate the desired size of the data packet or it can be controlled directly from the signal of the external pulse generator that drives the TX\_PE line as described above.

The CRC generator appends a CRC check at the end of the data. The CRC will be checked at the RX portion of the PER tester after it has been transmitted and received through the channel. The RX will check the data for CRC errors and if in

error then the packet will be declared as such. The PER tester TX function maintains a count of all transmitted packets through the TX packet counter.

#### **RX Function**

The PERT RX functions include a CRC Check and the RX packet counter. The timing of the RX interface between the PRISM (HSP3824) and the PERT receiver is shown on Figure 6.

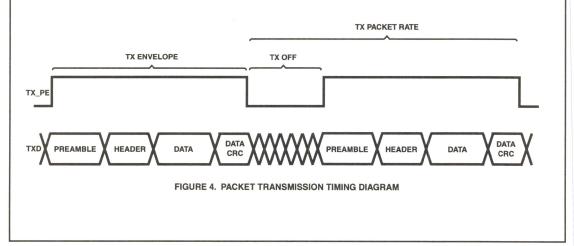
The PERT checks the data for the CRC calculation starting when MD\_RDY is asserted by the HSP3824. MD\_RDY envelopes the first data bit after the preamble and it is deasserted at the end of the data CRC.

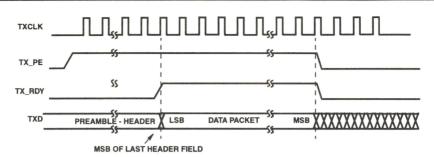
The PERT receiver counts all packets received and then subtracts from that count any packets that have been detected with a CRC error. This count, that is maintained by the PERTs receiver, in conjunction with the count that is maintained by the PERTs transmitter (which keeps track of the number of all transmitted packets) are used to derive the PER performance of the system under test.

This PERT design is capable to account for all packets in error.

- If a packet is never received, the transmitter will report it to its TX packet count and the error will be accounted for.
- If an error occurs within the PRISM (HSP3824) header, which has not been processed by the PERTs CRC circuit, the packet in error will not be received by the PERT. The HSP3824 will drop the packet (will not assert MD\_RDY), upon detecting a corrupt header.
- If an error occurs within the PERT generated data, it will be detected by the CRC check function of the PERT receiver. This packet will be subtracted from the received packet count.

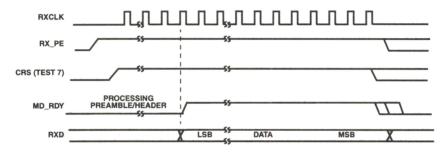
By utilizing the PERTs CRC checks in combination with the HSP3824 programmable features, the design can be simplified since no actual data comparisons need to be implemented. This design can lead to effective PER performance measurements for a PRISM based packetized system.





NOTE: Preamble/Header and Data is transmitted LSB first TX\_RDY is inactive Logic 0 when generated externally. TXD shown generated from rising edge TXCLK.

FIGURE 5. PRISM (HSP3824) DIGITAL TX INTERFACE



NOTE: MD\_RDY active after CRC16.

FIGURE 6. PRISM (HSP3824) DIGITAL RX INTERFACE



No. AN9624.3 February 1997

# Harris Wireless Products

# PRISM™ DSSS PC Card Wireless LAN Description

Author: Carl Andren, Mike Paljug, Doug Schultz



#### Introduction

The PRISM™ PC Card Wireless LAN Kit is provided with two reference wireless LAN PC Cards. This note will detail the

RF and analog design of these cards. The physical layer (PHY) sections of these PC Cards are described in detail in the following sections. The medium access control (MAC) section of the PC Cards is described in detail in the pending AMD application note titled "Wireless LAN DSSS PC Card Reference Design" [1].

Figure 1 shows a block diagram of the reference radio design. This radio has been designed to conform to the draft IEEE 802.11 specification but does not include the antenna diversity selection.

The specifications of the PC Card wireless LAN are as follows:

# Receive Specifications

• Frequency Range 2.4GHz - 2.4835GHz
• Step Size
Cascaded Noise Figure 6.8dB
• Sensitivity93dBm, 1 MBPS, 8E-2 FER (Note 1) -90dBm, 2 MBPS, 8E-2 FER (Note 1)
Input Intercept Point17dBm
• IF Frequency
• IF Bandwidth
Image Rejection80dB
Adjacent Channel Rejection >35dB
• Supply Voltage 2.7V - 5.5V

# Transmit Specifications

I	ransını əpecincations
•	Frequency Range 2.4GHz - 2.4835GHz
Ð	Step Size
	Output Power
	Spurious Outputs
	Transmit Spectral Mask32dBr at First Side-Lobe
9	IF Frequency
	Supply Voltage 2.7V - 5.5V

# General Specifications

•	Targeted Standard IEEE 802.11
•	Data Rate
•	Range

- RX/TX Switching Speed . . . . . . . . . . . . . . . . . 2  $\mu s$
- · Power Savings Modes
  - Mode 1: 190mA at 1µs Recovery (Notes 3, 4)
  - Mode 2: 70mA at 25µs Recovery (Notes 3, 4)
  - Mode 3: 60mA at 2ms Recovery (Notes 3, 4)
  - Mode 4: 30mA at 5ms Recovery (Notes 3, 4)
- Average Current (Without Power Savings Modes)298mA (Note 5)
- Average Current (With Power Savings Modes)60mA (Note 6)

#### NOTES

- 1. FER = Frame Error Rate or Packet Error Rate.
- 2. Range Test using AND-C-107 omnidirectional antenna.
- 3. Supply current includes AM79C930 MAC Processor.
- Recovery time is for the PRISM™ 2.4GHz Chip Set only and does not include programming latency of the AM79C930 MAC Processor.
- 5. Based on average current consumption for "typical" application.
- Power savings modes refer to AN9665. Average radio current consumption for "typical" application.

# Receive Processing

Referring to the block diagram in Figure 1, a single antenna is used. Up to two antennas are supported in the HSP3824[2] Baseband Processor to implement diversity, countering the adverse effects of multi-path fading. From the antenna, the received input is applied to FL1, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, which is used to provide image rejection for the receiver. The IF frequency is 280MHz, and low-side injection is used, thereby placing the received image 560MHz below the tuned channel. FL1 also provides protection for the RF front-end from out of band interfering signals.

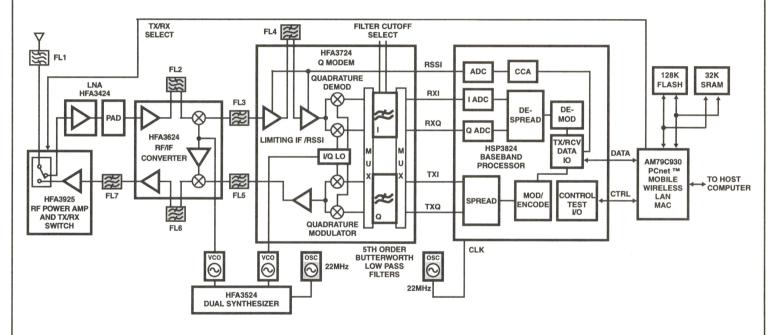


FIGURE 1. PRISM™ PC CARD BLOCK DIAGRAM

Cnet™ is a trademark of AMD, Inc.

TABLE 1. PRISM™ CASCADED FRONT-END ANALYSIS

STAGE	G	GC	F	FC	IP30	IP30C	IP3IC
FL1 RF FILTER	2.0	- 2.0	2.0	2.0	100.0	100.0	102.0
HFA3925 T/R SWITCH	- 1.2	- 3.2	1.2	3.2	34.0	34.0	37.2
HFA3424 LNA	13.0	9.8	2.0	5.2	11.1	11.0	1.2
ATTENUATOR	- 5.0	4.8	5.0	5.5	100.0	6.0	1.2
HFA3624 LNA	15.6	20.4	3.8	6.0	15.0	14.1	- 6.3
FL2 RF FILTER	- 3.0	17.4	3.0	6.0	100.0	11.1	- 6.3
HFA3624 MIXER	3.0	20.4	12.0	6.3	4.0	3.6	- 16.8
FL3 IF FILTER	- 10.0	10.4	10.0	6.4	100.0	- 6.4	- 16.8
HFA3724[6] IF STRIP	0.0	10.4	7.0	6.8	100.0	- 6.4	- 16.8

Cascaded Gain = 10.4dB Cascaded NF = 6.8dB Cascaded Input IP3 = -16.8dBm

NOTE: G (individual stage gain, dB), GC (cumulative gain, dB), F (NF, dB), FC (cumulative NF, dB), IP3O (individual stage output IP3, dBm), IP3OC (cumulative output IP3, dBm), IP3IC (cumulative input IP3, dBm)

The T/R switch is integrated in the HFA3925[3] RF Power Amplifier (RFPA). The HFA3925 RFPA operates from the unregulated 5V PC Card supply. Following the T/R switch, the HFA3424[4] Low Noise Amplifier (LNA) is used to set the receiver noise figure. The HFA3424 LNA operates from a regulated 3.5V supply.

A trade-off between noise figure and input intercept point exists in any receiver, to balance these conflicting requirements in the PRISMTM radio, an attenuator follows the HFA3424 LNA. The attenuation chosen is 5dB. To improve onise figure, this attenuation may be reduced; alternatively, to improve input intercept point, this attenuation may be increased. The cascaded front-end noise figure and input intercept point analysis is shown in Table 1.

Next, the signal enters the HFA3624[5] RF/IF Converter LNA section, which aids in setting receiver NF. FL2 is used to suppress image noise generated in both the HFA3424 LNA and the HFA3624 LNA, and is a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. Only modest attenuation at the image frequency is required. The insertion loss is not critical, since at this point in the receiver, component loss or NF is offset by the preceding gain stages. All sections of the HFA3624 RF/IF Converter operate from a regulated 3.5V supply.

Down-conversion from the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter mixer section. As previously mentioned, the IF center frequency is 280MHz, and low-side local oscillator (LO) injection is used. A discrete LC matching network is used at the mixer output to differentially combine the IF outputs, as well as impedance match to a 50 $\Omega$  environment. A trimmer capacitor is used as part of the narrow-band matching network. An alternative, broadband matching network is described in the HFA3624 RF/IF Converter application note, and does not require any tunable

elements. A direct impedance match to the IF filter, FL3 could be implemented if desired. The  $50\Omega$  environment was chosen to allow ease in measurement of portions of the radio with external test equipment.

The IF receive filter, FL3, is a Toyocom TQS-432 SAW bandpass filter. The center frequency is 280MHz, the 3dB bandwidth is 17MHz, and the differential group delay is less than 100ns. Insertion loss is typically 6dB, making it ideal for single-conversion systems. The impedance of the SAW is 270 $\Omega$ , and a series 33nH inductor is used to match the filter input to  $50\Omega$ . The SAW output is matched directly to the IF input of the HFA3724 Quadrature IF Modulator/Demodulator, using a shunt 56nH inductor. This presents a 250 $\Omega$  source impedance to the limiter input, thereby optimizing the limiter's NF.

In the receive mode, the HFA3724 Quadrature IF Modulator/ Demodulator provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. All sections of the HFA3724 operate from a regulated 3.5V supply. The first limiting amplifier establishes the NF of the IF strip at approximately 7dB. A discrete one pole LC differential filter. FL4, is placed between the two limiters to restrict the noise bandwidth of the first limiter. As both limiters exhibit a broadband response, with over 400MHz bandwidth. a noise bandwidth reduction filter is appropriate to ensure that the second limiter is fully limiting on the front-end noise within the signal bandwidth, as opposed to the broadband noise generated by the first limiter. This filter has a center frequency of 280MHz, and a 3dB bandwidth of 50MHz. It consists of a fixed 10nH inductor and a fixed 20pF capacitor. as described in the HFA3724 data sheet.

At the output of the limiters, a  $200 \text{mV}_{\text{P-P}}$  differential signal level is maintained under all input conditions. This limited signal is then mixed in quadrature to baseband in the HFA3724 Quadrature IF Modulator/Demodulator. The LO needed for

the quadrature mixing is applied at twice the IF frequency, or 560MHz. A divide by two circuit then provides an accurate quadrature LO for the mixers. The baseband outputs of the quadrature mixers are AC coupled off-chip to the integrated fifth order Butterworth filters. The output levels of the low pass filters are nominally  $500mV_{P,P}$  single-ended, and are intended to be AC coupled to the HSP3824 Baseband Processor. The AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with  $0.01\mu F$  series capacitors. These coupling capacitors must be taken into account, however, when estimating the time it takes to power up or awaken from sleep mode.

At the input to the HSP3824 Baseband Processor, the quadrature signals are analog to digital converted in wideband 3 bit converters. The signals are spread spectrum with no DC term, so it is feasible to AC couple the signals to the ADCs and avoid DC bias offsets. The signal at this point has been limited to a constant IF amplitude and then passed through two separate mixer and low pass filter paths. The component variations in these two paths can introduce offsets in amplitude and phase and can also use up some of the headroom in the ADCs. The maximum amplitude variation is 2dB and the maximum phase balance variation is 4 degrees. Since the signal is limited, the IF signals will have low peak to average ratios even with noise as an input. The I and Q signals will have sinusoidal properties with PSK modulation imposed. It is their combined vector magnitude that is limited, not their individual amplitudes. To optimize the demodulator's performance, the ADCs are operated at the point where they are at full scale on either I or Q one third of the time. To maintain this operating point in the face of component variations, there is an active adjustment of the ADC reference voltage by feedback. This avoids the necessity of allowing extra headroom for the variation. The adjustment circuit is very slow and averages the energy from the two channels over both packet and noise conditions.

The HSP3824 Baseband Processor correlates the PN spreading to remove it and to uncover the differential BPSK or QPSK data. The processor initially uses differential detection to identify and lock onto the signal. It then makes measurements of the carrier and symbol timing phase and frequency and uses these to initialize tracking loops for fast acquisition. Once demodulating and tracking, the processor uses coherent demodulation for best performance. Since this radio uses a spread spectrum signal, the signal to noise ratio (SNR) in the chip rate bandwidth is about 0dB when the demodulator is at the desired bit error rate in BPSK. The radio operates with about 2.5dB of implementation loss relative to theoretical performance and achieves a sensitivity of -93dBm with BPSK.

The HSP3824 Baseband Processor provides differential decoding and descrambling of the data to prepare it for the Media Access Controller (MAC). The MAC is an AMD AM79C930 PCnet™-Mobile controller. All packet signals have a preamble followed by a header containing a start frame delimiter (SFD), other signal related data and a cyclic redundancy check (CRC). The MAC processes the header data to locate the SFD, determine the mode and length of the incoming message and to check the CRC. The MAC

then processes the packet data and sends it on through the PC Card interface to the host computer. The MAC checks the packet data CRC to determine the data purity. If corrupted data is received, a retransmission is requested by the MAC which handles the physical layer link protocols.

# Transmit Processing

Data from the host computer is sent to the MAC via the PC Card interface. Prior to any communications, however, the MAC sends a Request to Send packet to the other end of the link and receives a Clear to Send packet. The MAC then formats the data by appending it to a preamble and header and sends it on to the HSP3824 Baseband Processor which clocks it in. The HSP3824 Baseband Processor scrambles the packet and differentially encodes it before applying the spread spectrum modulation. The data can be either DBPSK or DQPSK modulated at 1 MSPS and is a baseband quadrature signal with I and Q components. The spreading is an 11 chip Barker sequence that is clocked at 11MHz and is modulated with the I and Q data components. These are then output to the HFA3724 as CMOS logic signals.

Transmit quadrature single-bit digital inputs are applied to the HFA3724 Quadrature IF Modulator/Demodulator from the HSP3824 Baseband Processor. These inputs are attenuated by 1/7 and DC coupled to the fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is -30dBc at the first side-lobe relative to the main-lobe. An unfiltered PSK waveform would have the first side-lobe suppressed only -13dBc. The fifth-order filters are tuned to an approximate 7.7MHz cutoff, using a  $909\Omega$  resistor external to the HFA3724.

In the PC Card wireless LAN, the goal is to control the regrowth of the side-lobes, with the HFA3925 RFPA dominating the regrowth. This will result in maximum transmitted power available. To achieve this goal, once the PSK waveform is filtered at baseband, all remaining transmit elements are operated at a 6dB back-off from compression, except for the HFA3925 RFPA, which is operated at less back-off.

The low pass filters provide initial shaping of the PSK waveform. Final shaping is provided by a transmit IF filter, FL5, a Toyocom TQS-432 SAW bandpass filter. The low pass filter outputs are off-chip AC coupled to the quadrature up-converter in the HFA3724. As in the receive mode, the baseband AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with  $0.01\mu F$  series capacitors. The same twice IF frequency LO used previously is also used in this up-conversion. The IF output of the HFA3724 is reactively matched to FL5, with a  $250\Omega$  resistive load presented to the HFA3724. A shunt 47nH inductor, in parallel with a  $316\Omega$  resistor, is used to provide this match, negate the effects of board and component capacitance, and provide a DC return to  $V_{CC}$  to prevent saturation in the IF output stage of the HFA3724.

The output of FL5 is terminated in a  $200\Omega$  potentiometer that is used for transmit gain control. A shunt 47nH inductor is used to negate the effects of parasitic board and component shunt capacitance, as well as match the SAW output to the

potentiometer. This potentiometer has it's center wiper connected to the HFA3624 RF/IF Converter transmit IF input, which has an input resistance of approximately  $3k\Omega$ . By varying the potentiometer, the gain of the transmit chain is controlled, allowing for precise control of the signal back-off at the HFA3925 RFPA. Therefore, this potentiometer is adjusted to achieve the desired compromise between transmit output power and the main-lobe to side-lobe ratio of the output PSK waveform, typically -32dBc to -35dBc.

Upconversion to the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter transmit mixer. The mixer output is filtered with FL6, a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. This filter suppresses the LO feedthrough from the mixer, and selects the upper sideband. The transmit buffer in the HFA3624 RF/IF Converter preamplifies the selected sideband, easing the requirement for HFA3925 RFPA gain.

FL7, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, is used to further suppress both the transmit LO leakage and the undesired sideband.

The HFA3925 RFPA amplifies the transmit signal to a level of approximately +20dBm, as measured at the T/R switch output. This represents a back-off from 1dB compression of approximately 4.5dB. Transmit side-lobe performance is approximately -32dBc to -35dBc with this level of back-off.

The HFA3925 RFPA is the only physical layer component that operates directly from the 5V PC Card supply. To supply the needed negative gate bias to the HFA3925 RFPA, a ICL7660SIBA[7] charge pump is used. A second potentiometer is used to adjust the drain current on the third stage of the HFA3925 to a quiescent operating current of 90mA, as measured through a one ohm sense resistor.

A logic-level PMOS switch, RF1K49093[8], is used to control the drain supply voltage to the HFA3925 RFPA, and implement a power down mode when receiving. As the RF1K49093 is a dual device, the other PMOS switch is used to control the supply voltage to the HFA3424 LNA and implement a power down mode when transmitting. A 2N2222 NPN transistor is used to level shift the 3.5V logic level from the AM79C30 MAC to drive the 5V PMOS switch gates, as well as the 5V HFA3925 RFPA T/R control gate.

Following the T/R switch, FL1 is reused in the transmit mode to attenuate harmonics generated in the HFA3925 RFPA, as well as providing additional suppression of the LO. As the loss of FL1 is approximately 2dB, the amount of transmit power available at the antenna is approximately +18dBm.

## Synthesizer Section

The dual frequency synthesizer section uses the HFA3524[9] Synthesizer and two voltage controlled oscillators to provide a tunable 2132MHz - 2204MHz first LO, and a fixed 560MHz second LO. Both feedback loops use a 1MHz reference frequency that is derived from a 22MHz MF Electronics T3391-22.0M crystal oscillator. This crystal oscillator currently limits the operating temperature range of the radio to 0°C to 70°C. Both passive loop filters were designed to have loop bandwidths of 10kHz, and phase margins of 50

degrees. The feedback loop analysis is described in the HFA3524 Synthesizer evaluation board documentation. All components in the synthesizer section operate from a regulated 3.5V supply.

The tunable 2132MHz to 2204MHz first LO oscillator is a Z-Communications SMV2100L VCO. To ensure operation at low tuning voltages, a start-up circuit was added to force the tuning voltage from the HFA3524 Synthesizer RF charge pump to a high state for a short period (~1ms) following HFA3524 programming. A 2N2907 PNP transistor was used to implement this function, and the AM79C930 MAC device provides the control signal. The output level of the first LO to the HFA3624 RF/IF Converter is attenuated to approximately -3dBm.

The fixed 560MHz second LO oscillator is a discrete design, using a Phillips BFR505 transistor and a Siemens BBY51 varactor, as described in the HFA3524 Synthesizer evaluation board documentation. The output level of the second LO to the HFA3724 Quadrature IF Modulator/Demodulator is attenuated to approximately -6dBm and a three pole low pass filter is included to preserve the duty cycle of the output. High even order components in the second LO can result in offsets from a 50% duty cycle, and will degrade the quadrature phase accuracy of the HFA3724. A transconductance network is used at the HFA3724 LO input to convert the second LO voltage into a current, as recommended in the HFA3724 data sheet. As the HFA3524 Synthesizer auxiliary IF input covers the 560MHz range, the internal divideby-two LO buffer output of the HFA3724 is disabled, as recommended in the HFA3724 data sheet.

# Regulator Section

Linear voltage regulators are used to provide filtering and isolation from the 5V PC Card input supply. An additional advantage of using voltage regulators is a savings in overall supply current, as all of the components that are regulated consume less current at a 3.5V operating point, as opposed to a 5V operating point. The only components operating directly from the 5V supply are the HFA3925 RFPA, in order to maximize RF output power, and the PC Card interface. Sections of the AM79C930 MAC controller, as well as the host computer may use 5V logic levels.

A total of three regulators, 3.5V Toko TK11235MTL, are used in the PC Card wireless LAN. One regulator is devoted to the HSP3824 Baseband Processor and AM79C930 MAC devices. The remaining two regulate the RF and IF sections of the radio. One regulator supplies voltage to the synthesizer section, the HFA3424 LNA, and the HFA3624 RF/IF Converter. The second regulator supplies voltage to the HFA3724 Quadrature IF Modulator/Demodulator.

### References

- [1] AMD Application Note, Wireless LAN DSSS PC Card Reference Design; application note # pending.
- [2] HSP3824, data sheet, AnswerFAX document #4064, 407-724-7800.
- [3] HFA3925, data sheet, AnswerFAX document #4132, 407-724-7800.
- [4] HFA3424, data sheet, AnswerFAX document #4131, 407-724-7800
- [5] HFA3624, data sheet, AnswerFAX document #4066, 407-724-7800.
- [6] HFA3724, data sheet, AnswerFAX document #4067, 407-724-7800.
- [7] ICL7660S, data sheet, AnswerFAX document #3179, 407-724-7800.
- [8] RF1K49093, data sheet, AnswerFAX document #3969, 407-724-7800.
- [9] HFA3524, data sheet, AnswerFAX document #4062, 407-724-7800.

# M APROTE

No. AN9627 July 1996

Harris Linear

# **Using the HFA3424 Evaluation Board**

Author: Tim Bozych



# Introduction

The HFA3424 is a highly integrated Low Noise Amplifier for use in the 2.4GHz ISM band. The LNA features include on-

chip matching and DC blocking on the RF input and output ports. The HFA3424 is packaged in an 8 pin SOIC (Figure 2) which will facilitate its use in PCMCIA type RF front end applications.

### **Board Description**

An electrical schematic of the demo board is shown in Figure 1 below. The typical test diagrams shown on page 2 (Figures 3 & 4) of this document will guide you in your evaluation setup. The Vdd line is connected to a power supply set to the correct value (3-5.5V). In Figure 3 the RF Signal Input is connected to port 1 on the Network Analyzer S-parameter unit. The RF signal Output is connected to port 2 on the S-parameter unit. In this configuration all four S-parameters

can be measured and verified to the stated datasheet numbers and any additional points or bands of interest can be evaluated as well.

Two-tone IP3 measurements (see Figure 4) can be made by replacing the S-parameter unit with a Spectrum Analyzer on the output and two sine wave generators connected with isolators through a combiner to the input.

Pin 2 ( $V_{bias}$ ) of the HFA3424 is used to implement an optional high bias mode of operation when connected. By grounding the  $V_{bias}$  pin through  $30\Omega$  to  $35\Omega$  the device will consume approximately 20mA bias current. The benefits of this operational mode are increased gain, reduced noise figure and increased IP3.

The evaluation board is manufactured from standard FR4 circuit board materials. It incorporates an internal ground layer 8 mils below the surface trace layer. The RF IN and RF OUT traces are 16 mils wide to provide the  $50\Omega$  transmission lines required on these ports.

 V<sub>BIAS</sub> (PIN 2)

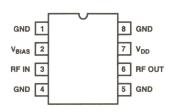
 NORMAL BIAS
 EXTENDED BIAS

 Open
 30Ω to 35Ω To Ground

The state of the s

FIGURE 1. EVALUATION BOARD SCHEMATIC

PIN 2 ALLOWS FOR AN EXTERNAL RESISTOR RS TO BE USED TO GROUND FOR AN OPTIONAL 20mA CURRENT OPERATION. RECOMMENDED VALUES FOR THE CHIP RESISTOR ARE  $30\Omega$  TO  $35\Omega$ .



**FIGURE 2. PINOUT** 

# HFA3424 Demo Board (Preliminary Version)

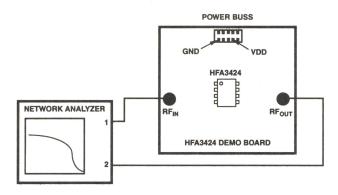


FIGURE 3. TYPICAL S-PARAMETER TEST SETUP

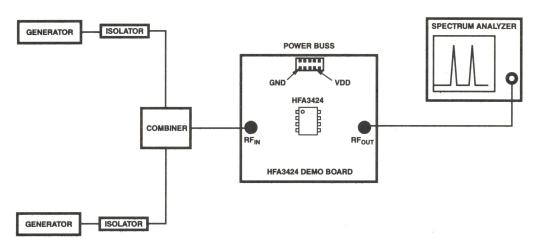


FIGURE 4. TYPICAL IP3 TEST SETUP

HFA3424 PRELIMINARY VERSION EVALUATION BOARD PARTS LIST				
PART NUMBER	PART NUMBER DESCRIPTION		TOTAL	
HFA3424IA	HFA3424 Low Noise Amplifier	Harris Semiconductor	1	
PCC201CQCT-ND	(0402) 5% RES, FXD, 30 -35Ω	Panasonic/Digikey	2	
PCC471CQCT-ND	(0402) CAP, FXD, 470pF NPO	Panasonic/Digikey	1	
0805CS-150XMBC	150nH RF Choke	Coilcraft/Digikey	1	
	Right Angle SMA Connector	Ma/Com	2	

# M APPOTE

No. AN9630 November 1996

# Harris Wireless Products

# **Using The HFA3524 Evaluation Board**

Author: Tim Bozych



### TM Introduction

The HFA3524 is a highly integrated Dual Frequency Synthesizer ideally suited for use in communications applications.

The Synthesizer features include a dual modulus prescaler for simultaneous RF and IF local oscillator generation using a very stable digital phase locked loop technique. The HFA3524 is packaged in an 20 pin TSSOP (Figure 3) which will facilitate its use in PCMCIA type applications. For additional information see individual datasheet spec number 4062.

# **Board Description**

The HFA3524 evaluation board comes assembled and tested from our factory. The eval kit includes documentation such as this to help make your evaluation of our product a success. The HFA3524 eval board is shipped with a PC parallel interface cable and a 3.5" floppy disc containing the DOS driver software. Simply plug in the disc, load the soft-

ware, make the connections to the eval board and you are ready to run.

The HFA3524 eval board comes preset from the factory optimized and built to run at +3.5VDC from a single supply. Please see page two, Figure 2 and inset. As you can see in the inset of Figure 2, to run from a single supply you must install the  $0\Omega$  resistor RSP and connect the 4 PC jumper switches between pins 2-4 and 1-3 on each of the two PC jumper switch pin headers. This is how your evaluation board comes from the factory. Connections are available on the board to run from separate supply sources if so desired. If you must run from separate sources you must change the PC jumper switch positions and also you may have to remove component RSP.

To minimize noise it is highly recommended that a shielded cable be used, such as an SMA or BNC type to connect DC power to the evaluation board.

Figure 1 below shows a functional block diagram of the HFA3524 Dual Synthesizer.

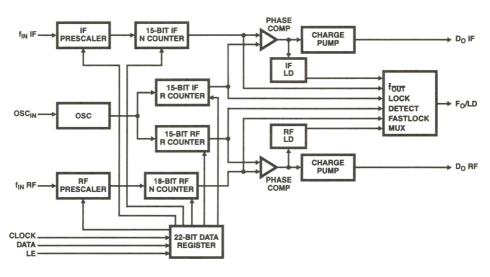
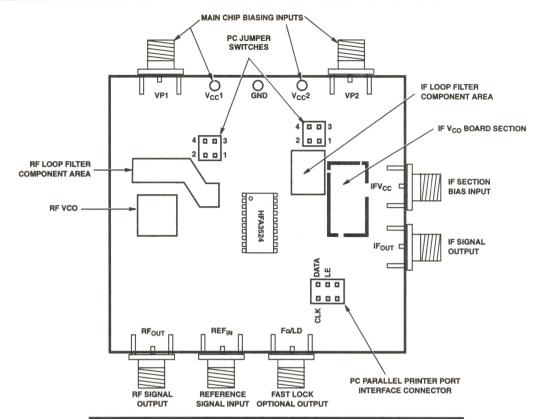


FIGURE 1. HFA3524 FUNCTIONAL BLOCK DIAGRAM



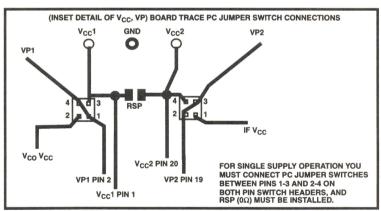
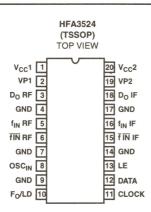


FIGURE 2. HFA3524 EVALUATION BOARD COMPONENT AND SECTION DETAILS

### **EVALUATION BOARD SPECIFICATIONS**

PARAMETER	RF SYNTHESIZER	IF SYNTHESIZER	UNITS	
Output Frequency	2132 to 2204	560	MHz	
Output Power	-6 to 0	-6 to 0	dBm	
Reference Frequency	10	10	MHz	
Reference Level Input	-35 to +15	-	dBm	



PART NUMBER	TEMP. RANGE (°C)	PACKAGING	PKG. NO.
HFA3524IA	-40 to 85	20 Ld TSSOP	M20.173
HFA3524IA96	-40 to 85	Tape and Reel	

FIGURE 3. HFA3524 PINOUT AND PACKAGING INFORMATION

The eval board RF section is setup and tested to cover the RF band from 2132MHz to 2204MHz and is guaranteed to be functional across this band using the driver software to tune to your selected frequency. Although it may be possible to tune and lock to a frequency outside of this band, it is not recommended due to the fact that the loop filters are designed for the aforementioned band. The IF section is setup to be a fixed frequency LO of 560MHz. Some limited tuning of this frequency may be possible with the driver software but none is implied nor tested.

Typical operation and test setups are shown in Figures 4 and 5. Figure 4 shows the connections necessary to study the RF output of the HFA3524 Eval board. Figure 5 shows the equivalent IF output setup. The outputs may be programmed up and monitored simultaneously if so desired. Typical output power levels for both the IF and RF section are on the order of -5dBm to 0dBm and the typical total current consumption of the eval board is approximately 30mA with both outputs programmed and running. There is no output power adjustment available on the HFA3524 eval board for either output. As always an external pad or amplifier may be used to obtain your desired level.

The reference input on the evaluation board (REF $_{\rm IN}$ ) is a capacitively coupled 50 $\Omega$  terminated input. A very stable crystal derived 10MHz sinusoidal signal needs to be applied here. The REF $_{\rm IN}$  signal level range is -35dBm to +15dBm. This signal can be supplied from the 10MHz reference output available on most pieces of test equipment. The phase noise of this signal will be multiplied and included in the total phase noise you would measure on the evaluation board output so the integrity of this signal is very important.

### Software Description

The HFA3524 DUAL SYNTHESIZER EVALUATION BOARD SOFTWARE: Using your PC's 3.5" floppy drive you can load and run the driver software and also access complete instructions. The user instructions are contained in the "INSTRUCT.TXT" file. A hardcopy of this file is contained in your evaluation kit documentation package. Harris Semiconductor recommends reading the instructions file. Some quick start-up instructions are included here. Please refer to the HFA3524 data sheet for explanations of modes, registers, etc.

### DRIVER SOFTWARE QUICK START INSTRUCTIONS:

#### Type HFA3524 Press Return

The first screen you will see will request your parallel printer output port address, supply your address, or, accept the default by pressing the RETURN key.

### **Using the Software**

See the "HFA3524 Evaluation Board Software Quick Start Guide" included in this document.

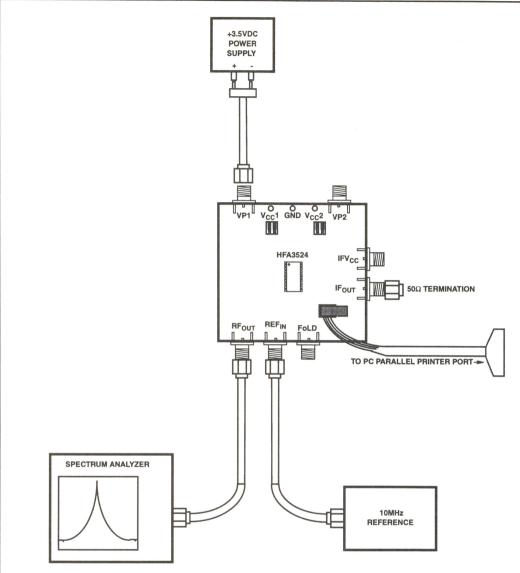


FIGURE 4. TYPICAL HFA3524 EVAL RF OUTPUT TEST SETUP SHOWING PC JUMPER SWITCHES INSTALLED AND COMPUTER INTERFACE CABLE CONNECTED

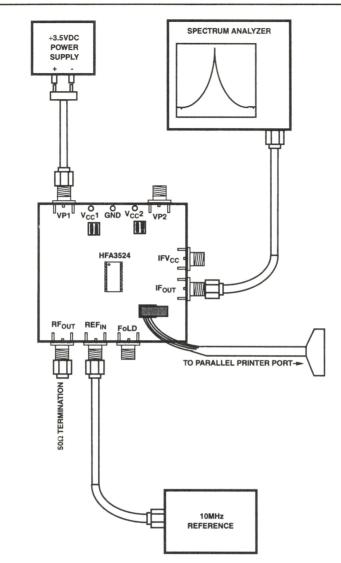
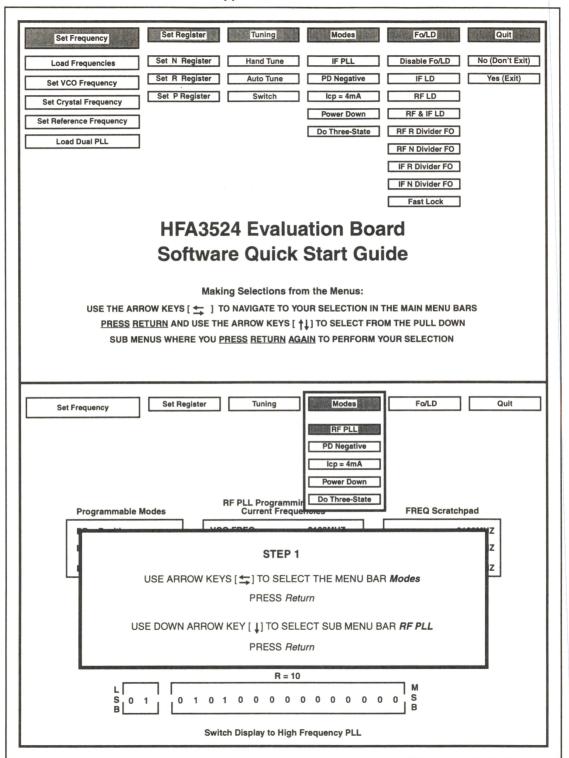
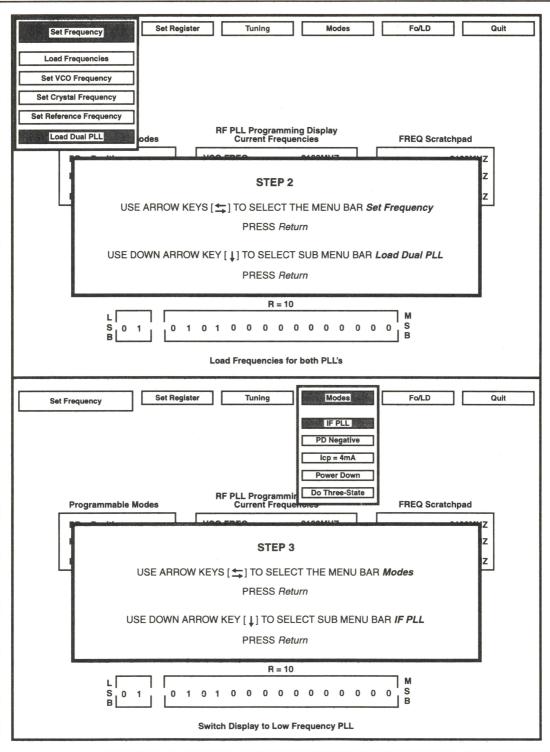
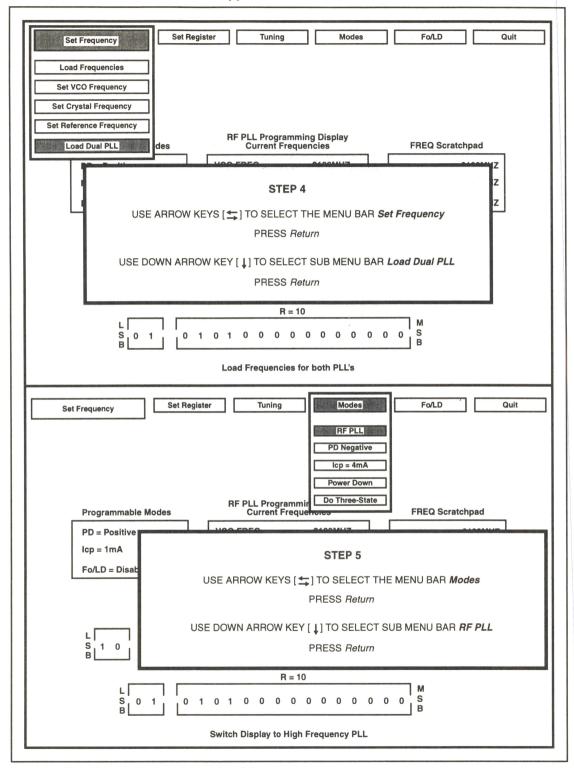
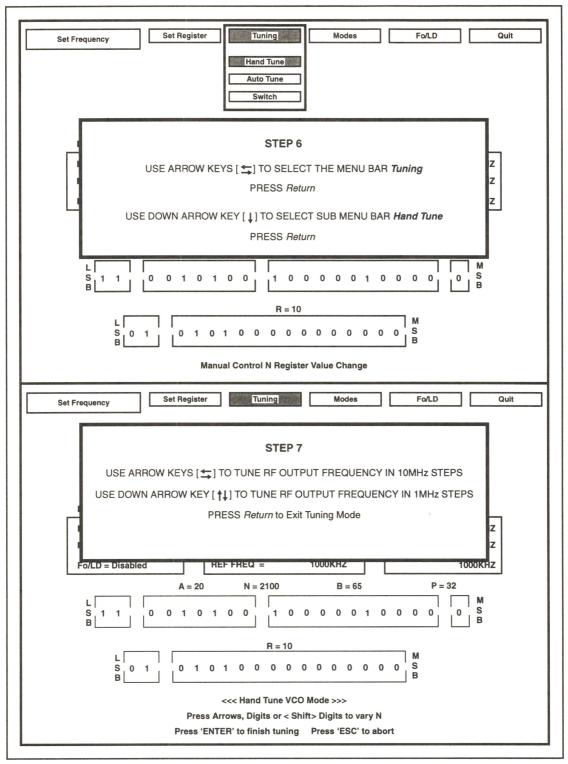


FIGURE 5. TYPICAL HFA3524 EVAL IF OUTPUT TEST SETUP SHOWING PC JUMPER SWITCHES INSTALLED AND COMPUTER INTERFACE CABLE CONNECTED



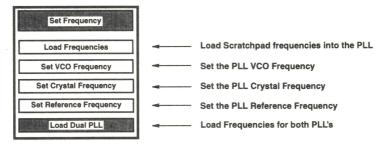




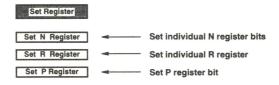


### **Software Pulldown Menu Description**

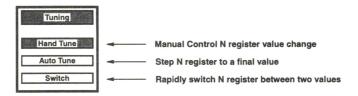
The Set Frequency Main Menu Bar and its submenus

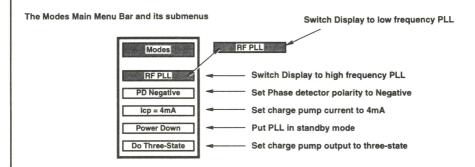


The Set Register Main Menu Bar and its submenus



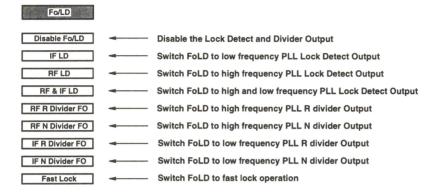
The Tuning Main Menu Bar and its submenus





### Software Pulldown Menu Description (Continued)

#### The Fo/LD Main Menu Bar and its submenus



The Quit Main Menu Bar and its submenus



# Parts List for BOM HFA3524 Eval

PART	DESCRIPTION	VALUE	QUANTITY	SMD SIZE	MANUFACTURER	PART NUMBE
U1	2.4GHz PLL		1	20 ld TSSOP	Harris Semiconductor	HFA3524IA
VCO1	2.1-2.4GHz VCO		1		Z-Communications	SMV2100L
C1	Chip Capacitor	0.01μF	1	0805		
C13	Chip Capacitor	0.1μF	1	0603		
C2, C14, C19, C21, C25	Chip Capacitor	0.1μF	5	0805		
C3	Chip Capacitor	1800pF	1	0603		
C6	Chip Capacitor	1000pF	1	0805		
C7, C9, C15, C18, C22, C24, C26, C35, C31a	Chip Capacitor	100pF	9	0603		
C8, C12, C130	Chip Capacitor	100pF	3	0805		
C10	Chip Capacitor	1.0μF	. 1	1206		
C11, C16, C17, C20	Chip Capacitor	0.01μF	4	0603		
C27	Chip Capacitor	4.7pF	1	0603		
C28, C29	Chip Capacitor	15pF	2	0603		
C31	Chip Capacitor	5600pF	1	0805		
C32	Chip Capacitor	0.056μF	1	0805		
C33	Chip Capacitor	1000pF	1	0603		
CF1, CF2	Chip Capacitor	5.6pF	2	0603		
RA1, RA3, RES1	Chip Resistor	10Ω	3	0603/0402		
RA2	Chip Resistor	120Ω	1	0603/0402		
RA4, RA5	Chip Resistor	20Ω	2	0603/0402		
RA6, Rref	Chip Resistor	51Ω	2	0805		
R2	Chip Resistor	430Ω	1	0603/0402		
R3	Chip Resistor	910Ω	1	0603/0402		
R4, RSP	Chip Resistor	0Ω	2	0603/0402		
R8	Chip Resistor	100Ω	1	0805		
R16	Chip Resistor	100Ω	1	0603/0402		
R10	Chip Resistor	30Ω	1	0603/0402		
R13	Chip Resistor	75Ω	1	0603/0402		
R14, R17, R21, R23, R25	Chip Resistor	10kΩ	5	0603/0402		
R15	Chip Resistor	8.2kΩ	1	0603/0402		
R19	Chip Resistor	750Ω	1	0603/0402		
R20	Chip Resistor	1.5kΩ	1	0603/0402		
R22, R24, R26	Chip Resistor	22kΩ	3	0603/0402		
L1, L2	SMD Inductor	12nH	2			
LF1	SMD Inductor	15nH	1			
SMA1-SMA7	End Launch Small Connector		7		Newark Electronics	142701851
J1-J6	Dual Row Header		7		Semtec	TSW13607GD
V1	SMD Varactor Diode		1		Seimens	BBY51
Q1	SMD NPN Transistor		1		Phillips	BFR-505

# APPROTE

No. AN9633 August 1996

# Harris Wireless Products

# Processing Gain for Direct Sequence Spread Spectrum Communication Systems and PRISM™

Authors: John Fakatselis, Harris Corporation Semiconductor Sector Madjid A. Belkerdid Electrical and Computer Engineering Department University of Central Florida Orlando, FL 32816



### ™ Introduction

This application note addresses the concept of processing gain (PG) of Direct Sequence Spread Spectrum (DSSS)

systems. The PRISM chipset is used to implement DSSS radio designs. The processing gain provides the unique properties to the DSSS waveform primarily in terms of interference tolerance. The PG of a DSSS system is centered around the utilization of random codes which are used in conjunction with the data. These random codes are referred as Pseudo Noise (PN) codes. The HSP3824 provides this coding capability for the PRISM.

# Description

In a DSSS system random binary data with a bit rate of  $r_b$  bits per sec (bps) is multiplied (Exclusive Ored) by a pseudorandom binary waveform, which is at much higher rate and it provides the frequency spreading operation. This pseudorandom (PN) binary source outputs symbols called chips at a constant chip rate  $r_{\rm C}$  chips per sec (cps). This is a random, noise like signal and hence the name PN signal. The chip rate is always higher than the bit rate, and the ratio of the chip rate to the bit rate is defined as the processing gain (PG) [2]. The PG is a true signal to jammer (interference) ratio at the receiver after the despreading operation (removal of PN).

The rate of the PN code is the one that defines the bandwidth of the transmitted spread waveform.

The receiver of a DSSS system must remove the spreading as the first step in the demodulation process.

During the despreading operation the receiver must generate a phase locked exact replica of the pseudorandom spreading waveform to match the transmitted signal. This is achieved by the code acquisition, and code tracking loops embedded in the HSP3824. The receiver PN sequence must be exactly in phase with the transmitted PN sequence, and this is achieved by correlation techniques.

### DSSS Transceiver

A DSSS transmitter is shown in Figure 1. The data is denoted by d(t), the spreading signal is denoted by c(t), and the spread waveform q(t) is fed to the BPSK modulator operating at a carrier frequency  $f_C$ , and the transmitted signal is denoted by x(t).

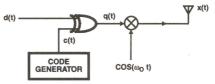


FIGURE 1. DSSS TRANSMITTER

A text book conceptual block diagram of a DSSS receiver is depicted in Figure 2. Note that PRISM is architected to perform the despreading function at baseband (HSP3824) rather than at RF as shown on Figure 2. This example is used for illustration of the concept and not to reflect the actual PRISM implementation.

The received signal for this text book example is the combination of the transmitted spread spectrum signal and a narrow band jammer  $x_J(t)$ . The locally generated despreading sequence is denoted by c'(t), and should be equal to c(t). The despread signal is then band pass filtered before data demodulation and d'(t) should be equal to d(t).

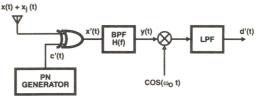


FIGURE 2. DSSS RECEIVER

### PG Benefits

The primary benefit of processing gain is its contribution towards jamming resistance to the DSSS signal. The PN code spreads the transmitted signal in bandwidth and it makes it less susceptible to narrowband interference within the spread BW. The receiver of a DSSS system can be viewed as unspreading the intended signal and at the same time spreading the interfering waveform. This operation is best illustrated on Figure 3.

Figure 3 depicts the power spectral density (psd) functions of the signals at the receiver input, the despread signal, the bandpass filter power transfer function, and the band pass filter output. Figure 3 graphically describes the effect of the processing gain on a jammer. The jammer is narrow, and has a highly peaked psd, while the psd of the DSSS is wide and low. The despreading operation spreads the jammer power psd and lowers its peak, and the BPF output shows the effect on the signal to jammer ratio.

If for example, BPSK modulation is used and an Eb/No of lets say 14dB is required to achieve a certain BER performance, when this waveform is spread with a processing gain of 10dB then the receiver can still achieve its required performance with the signal having a 4dB power advantage over the interference. This is derived from the 14dB required minus the 10dB of PG.

The higher the processing gain of the DSSS waveform the more the resistance to interference of the DSSS signal.

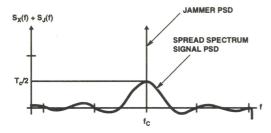


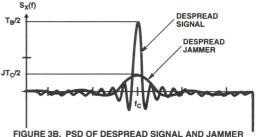
FIGURE 3A. PSD OF SPREAD SPECTRUM SIGNAL AND NAR-ROWBAND JAMMER

The classical definition of processing gain is the 10 Log number [r<sub>C</sub>/r<sub>B</sub>] in dB. By this definition a system that has a data rate of 1MBPS and a chip rate (rate of PN code) of 1MCPS will have a PG of 10.41dB. Using the PRISM chip set each data bit is x-ored with an 11 bit sequence for this particular example. The processing gain can be then viewed as the 10Log[11]dB where 11 is the length of the PN code. If a code with a length of 16 bits is to be used then the processing gain is equivalent to 10 Log[16] dB or 12.04dB.

To this end these PN signals must posses certain mathematical properties to be useful as part of a DSSS system. Primarily the PN codes that are useful must have very good autocorrelation and crosscorrelation properties as well as maintaining some randomness properties.

The DSSS receiver is utilizing a reference PN sequence which is a replica to the transmitted sequence and when it detects correlation between the reference and the incoming sequences it declares initial acquisition and it establishes initial symbol timing. Any partial correlations can result to false acquisitions and degradation to the receiver performance. This is why the PN code must have good correlation properties. Some of the PN code classes with such properties are described next.

This paper highlights the Barker codes, Willard codes and m-sequences with 7 and 15 chips per period which are implementable using the HSP3824.



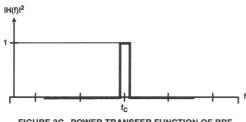


FIGURE 3C. POWER TRANSFER FUNCTION OF BPF

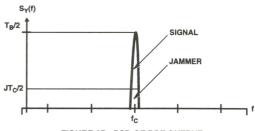


FIGURE 3D. PSD OF BPF OUTPUT

FIGURE 3. PROCESSING GAIN EFFECT ON NARROW BAND JAMMING

### PN Codes

PN codes with the mathematical properties required for implementation of a DSSS radio are:

### **Maximum Length Sequences**

Maximum length sequences (m-sequences), are PN sequences that repeat every 2<sup>n</sup>-1, where n is an integer, they are implemented by shift registers and Exclusive Or gates, they are governed by primitive polynomials, and possess good randomness properties including a two-valued autocorrelation function [3].

For example the 7 chip PN sequence is governed by the primitive polynomial generator

$$c_7(x) = 1 + x^2 + x^3$$

and the output chips are given by:

**0010111** 0010111 **0010111** 00101110...

Figure 4 depicts the d(t), c(t) with the above m-sequence, and with q(t) the x-or of d(t) and (ct).

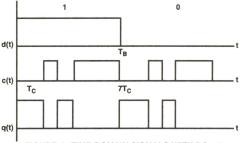


FIGURE 4. TIME DOMAIN SIGNALS WITH PG = 7

Figure 5 depicts the 7 chip sequence and its autocorrelation function. Note that the autocorrelation also repeats every 7 chips, or once per bit of the actual data if each of the data bits is spread by the entire sequence.

As another example, the 15 chip PN sequence is governed by the primitive polynomial generator

$$c_{15}(x) = 1 + x^3 + x^4$$

and the output chips are given by:

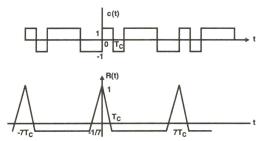


FIGURE 5. SEVEN CHIP M-SEQUENCE AND ITS AUTOCOR-RELATION FUNCTION

#### **Barker Codes**

**Application Note 9633** 

Barker Codes are short unique codes that exhibit very good correlation properties. These short codes with N bits, with N=3 to 13, are very well suited for DSSS applications and can all be generated by the HSP3824. A list of Barker Codes is tabulated in Table 1.

### Willard Codes

Willard Codes, found by computer simulation and optimization, and under certain conditions, offer better performance than Barker Codes. They can all be generated by the HSP3824, as was done for the Barker Codes. A list of Willard Codes is provided in Table 1.

The inverted or bit reversed versions of the codes listed on Table 1 can be used since they still maintain the desired autocorrelation properties.

**TABLE 1. BARKER AND WILLARD CODES** 

N	BARKER SEQUENCES	WILLARD SEQUENCES
3	110	110
4	1110 or 1101	1100
5	11101	11010
7	1110010	1110100
11	11100010010	11101101000
13	1111100110101	1111100101000

# Configuring the HSP3824 to Implement Various PN Codes

The HSP3824 is the baseband processor of the PRISM chipset and it generates the PN sequence. The device is programmable to any desirable sequence of up to 16 bits.

### **PN Generator Description**

The spread function for the radio is the same sequence and is applied to every symbol as BPSK modulation. PN generation is performed by parallel loading the sequence from a configuration register (CR) within the HSP3824 and serially shifting it out to the modulator.

### **PN Generator Programmable Registers**

A maximum of 16 bits can be programmed into the configuration register. Registers CR13 and CR14 contain the high and low bytes of the sequence for the transmitter. The corresponding registers for the receiver are CR20 & CR21. Bits 5 & 6 of CR3 set the sequence length in chips per bit. The sequence is transmitted MSB first. When fewer than 16 bits are in the sequence, the MSBs are truncated.

### **PN Correlator Description**

The PN correlator is designed to handle BPSK spreading. Since the spreading is BPSK, the correlator is implemented with two real correlators, one for the I and one for the Q channel. It has programmable registers to hold the spreading sequence and the sequence length for both the receiver and the transmitter. This allows a full duplex link with different spreading parameters for each direction.

The correlators are time invariant matched filters otherwise known as parallel correlators.

# References

- [1] R. L. Pickholtz, D. L. Schilling, and L. B. Milstein, "Theory of Spread-Spectrum Communications - A Tutorial", IEEE Trans. Comm., vol COM-30, May 1982.
- [2] R. C. Dixon, "Spread Spectrum Systems". New York: Wiley-Interscience, 1984.
- [3] R. L. Peterson, R. E. Ziemer, and D. E. Borth, "Introduction to Spread Spectrum Communications". Inglewood Cliffs, NJ: Prentice Hall, 1995.

WIRELESS

# APPIOTE

No. AN9638 August 1996

# Harris Wireless Products

# **Using The HFA3925 Evaluation Board**

Authors: Tim Bozych



### Introduction

The HFA3925 is a highly integrated three stage Power Amplifier (see Figure 1.) for use in the 2.4GHz ISM band. The

PA features include high gain and an on-chip Transmit/ Receive switch with the associated control line. The HFA3925 is packaged in a convenient to use 28 pin SSOP plastic package. (see Figure 2).

### **Board Description**

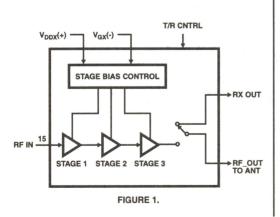
An electrical schematic of the demo board is shown in Figure 3. Figure 4 shows a pictorial representation of the HFA3925 Evaluation board which details the locations of the major components. Figure 5 details the operation of the transmit/receive switch. The typical test diagrams shown in Figures 6 & 7 of this document will guide you in your evaluation setup.

On the schematic of the HFA3925 Evaluation board, notice that all power and control connections to the device are accomplished through the 20 pin connector (P1). The associated assignments for each pin on the connector are denoted in parenthesis on the schematic as well as having the signal name listed next to the representations of the pins themselves. All RF connections are made via SMA connectors.

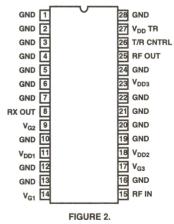
**REMEMBER:** Always apply Negative power to the  $V_G$  pins before applying the Positive  $V_{DD}$  bias. Failure to do so may result in the destruction of the HFA3925 Power amp.

Measuring the current drawn by each individual VDD line and adjusting its associated VG voltage value is a good way to start your HFA3925 Power Amplifier evaluation. The VG lines are connected to power supplies set to the correct value (-3 to -5.5V). Harris Semiconductor recommends a value of approximately -3.5VDC on each of the VG pins as a starting value. This will allow the quiescent stage current adjustment described. The V<sub>DD</sub> bias is then connected to +5VDC and subsequently powered up. For best performance in our Prism reference radio design we have found that the desired quiescent V<sub>DD</sub> stage currents should be adjusted as follows: I<sub>DD</sub> Stage 1 = 20mA, I<sub>DD</sub> Stage 2 = 50mA and I<sub>DD</sub> Stage 3 = 90mA Harris Semiconductor recommends you begin your evaluation here and we encourage you to adjust the amplifier and fine tune its response for your application and your particular waveform.

# **Block Diagram**



### **Pinout**



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In Figure 8 of this Appnote we include a schematic of a typical dual positive supply, single stage current adjustment circuit that will help control variations with temperature and simplify your design and production procedure. This circuit allows a single adjustment to stage 3 I<sub>DD</sub> of the Power amplifier while slaving the other two stages to it. Harris Semiconductor further recommends that an adjustment procedure be performed on stage 3 (such as this) in any production usage of the HFA3925 Power Amplifier, using your particular output waveform. Of course if you wish to use a single positive supply you may add an appropriate voltage regulator deriving the +3.5VDC from the +5V single supply.

In Figure 6 the RF Signal Input is connected to Port 1 on the Network Analyzer Sparameter unit, while RF OUT is connected to Port 2. Moving your Port 1 analyzer connection from RF IN to RX OUT and bringing the T/R CTRL line to +5V will allow you to evaluate the Sparameter performance of the Transmit/Receive switch in the receive mode.

In Figure 7 the RF input signal is a composite Direct Sequence Spread Spectrum (DSSS) from a generator and

the HFA3925 Power Amplifier output is analyzed with a spectrum analyzer. You will find in this type of test setup you can control the amount of distortion of the output (Spectral Regrowth) by adjusting the  $V_{\rm G}$  voltage value for each stage. By adjusting the  $V_{\rm G}$  values you can modify the linearity of the associated stage and control the distortion created from the amplifier given your particular input waveform. With the compression point mostly controlled in stage 3 of the amplifier, the fine tuning of  $V_{\rm G}3$  will have the most effect on spectral regrowth during this part of your evaluation. Spectral Regrowth values of -30dBc or better are achievable using this adjustment.

The HFA3925 evaluation board is manufactured from standard FR4 circuit board materials. It incorporates an internal ground layer under an 8mil substrate below the surface trace layer. The RF IN, RF OUT and RX OUT traces are 16mils wide to provide the 500hm transmission lines required on these ports. All other components are commonly found surface mount devices available from many sources.

### **Evaluation Board Schematic**

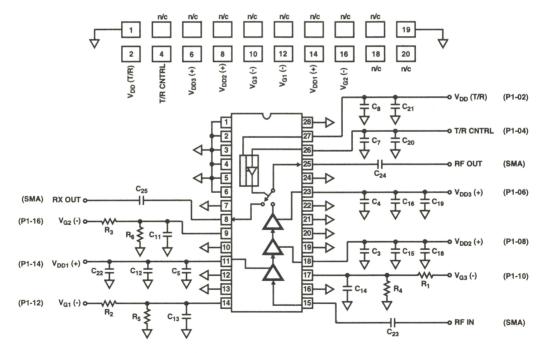


FIGURE 3. 20 PIN BOARD CONNECTOR (P1)

**TABLE 1. EXTERNAL CIRCUITRY PARTS LIST** 

LABEL	VALUE	PURPOSE
C <sub>3</sub> -C <sub>5</sub>	22pF	Bypass (GHz)
C <sub>23</sub> -C <sub>25</sub>	22pF	DC Block
C <sub>11</sub> -C <sub>16</sub>	1000pF	Bypass (MHz)
C <sub>18</sub> -C <sub>22</sub>	0.01μF	Bypass (kHz)
R <sub>1</sub> , R <sub>6</sub>	1.5kΩ	FET Gate Divider
R <sub>3</sub> , R <sub>5</sub>	5kΩ	Network
R <sub>2</sub>	12kΩ	
R <sub>4</sub>	1kΩ	

NOTE: All off-chip components are low cost surface mount components obtainable from multiple sources. (0.020in x 0.040in or 0.030in x 0.050in.)

# Demo Board (Preliminary Version)

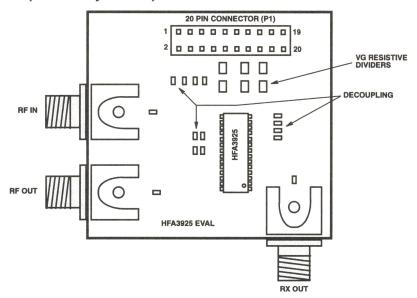
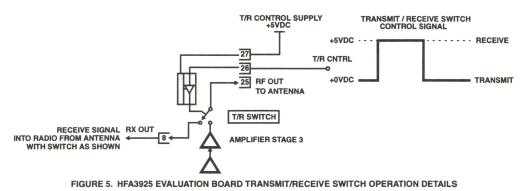


FIGURE 4. HFA3925 EVALUATION BOARD COMPONENT & SECTION DETAILS



# Demo Board (Preliminary Version) (Continued) | The state of the state

FIGURE 6. TYPICAL SPARAMETER TEST SETUP

**RX OUT** 

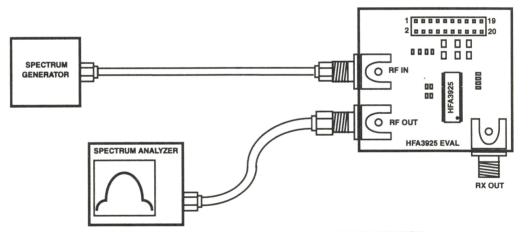
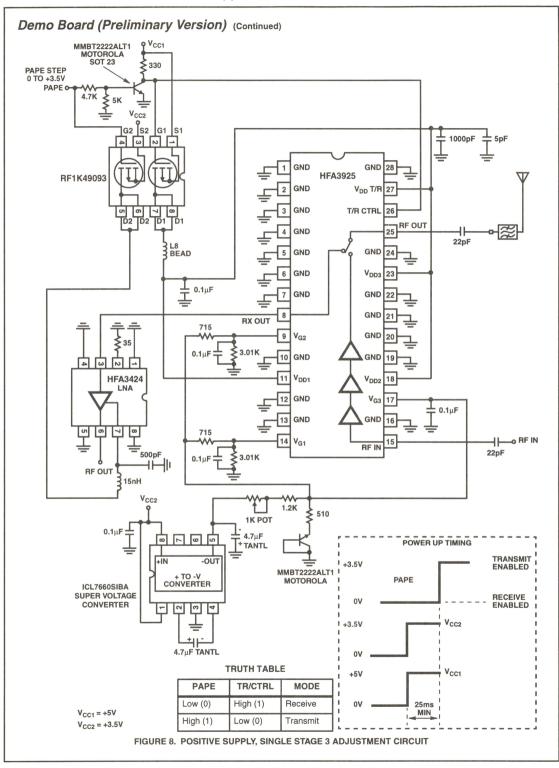


FIGURE 7. TYPICAL SPREAD SPECTRUM SPECTRAL REGROWTH TEST SETUP



# MAPROTE

No. AN9639 August 1996

Harris Wireless

# Harris PRISM Wireless LAN Network Connectivity and Utility SW (non IEEE802.11) For the WLAN Evaluation Kit

Authors: Mike Paljug, John Fakatselis (Harris Semiconductor) Eric Turner ( Squires Engineering)



### Introduction

This application note describes the firmware and software necessary to demonstrate limited network capabilities or to mea-

sure Packet Error Rate (PER) of the PC Card WLAN Evaluation Kit cards, that are based on the Harris PRISM chip set and the AMD Am79C930 MAC. This SW does not implement an IEEE802.11 network but it is a simplified protocol that can demonstrate ad-hoc connectivity and communications. In addition, a utility program is provided for evaluating the performance of the physical layer in terms of Packet Error Rate (PER) and loading MAC executables.

The SW referred to in this application note is distributed on two disks:

- A. The "Harris PRISM Wireless LAN Utility Software" disk.
- B. The "Harris PRISM Wireless Network Drivers" disk.

Network connectivity is provided by an NDIS 2.01 (Real-Mode) driver supporting MSDOS Version 6.22 and Windows for Workgroups (Windows 3.11). Two different MAC executables are provided to support either the NDIS driver or the PER application contained within the utility software. The PER software is one of the options contained in the utility SW which is a DOS application.

The PER program can be used to evaluate performance at the physical layer level but does not estimate performance of a complete IEEE802.11 network.

# Wireless LAN Connectivity

### Installation

Before Windows for Workgroups (WFW) connectivity can be established, the proper MAC executable must be loaded into the Flash memory device of the adapter. The adapter is shipped with the Flash device pre-loaded with 'cmdx40bp.bin' (Network Firmware). The Network Firmware allows network connectivity under WFW. If you have done any PER testing and need to reload the Network Firmware refer to Utility Software Usage.

Installing the network components necessary to establish WLAN connectivity in WFW will require the WFW installation CD or diskettes and the "Network Drivers" diskette provided with this Kit. Before you begin installing the adapter it is very important to backup your hard drive. Once the backup is complete, copy the autoexec.bat and config.sys files contained on the root of your C drive to a separate floppy. Copy system.in, win.ini, and protocol.ini (if it exists) from your Windows directory to this same floppy. Label and save these backups in a safe place.

Now you are ready to begin installing the network components. The goal is to provide connectivity between 2 or more laptop computers. To accomplish this objective the adapter driver must be loaded, several WFW networking components must be in place, and WFW must be configured properly. The following steps assume that WFW has already been installed on your PC and that you do not have any other network installed on your PC. Users with preexisting network adapters should be able to follow these instructions also, but should remove the preexisting adapter and any associated drivers using the "Network Setup" dialog.

- 1. Launch "Windows Setup".
- 2. Select the "Options" Pull-Down Menu.
- 3. Select "Change Network Settings".
- 4. The Network Setup dialog will appear.
- 5. Select "Networks".
- 6. The Networks dialog will appear.
- Select the "Install Microsoft Windows Network" button and click OK.
- 8. Select "Sharing".
- 9. The Sharing dialog will appear.
- Click the "I want to be able to give others access to my files" check box and click OK.
- 11. Select "Drivers".
- 12. The Network Drivers dialog will appear.
- 13. Select "Add Adapter"
- 14. Select "Unlisted or Updated Network Adapter".
- Follow the instructions in the next dialog box and click OK.

- Select the "Xircom CreditCard Netwave NDIS 2.01 Real Mode" driver and click OK.
- 17. The adapter default settings for IRQ, IO, etc. are accessible via the setup button. They may need to be changed from their defaults if a conflict occurs during subsequent operation.
- Click Close and follow WFW's directions on inserting the WFW diskettes necessary to complete the network installation.

### Description

This is network connectivity SW that is used to set up a demonstration ad-hoc network. Wireless connectivity is provided through Windows for Workgroups (Windows 3.11). Upon establishing a network connection, applications such as "chat" or "file manager" may be used to communicate files and other information.

It is suggested that no more than 4 network nodes are used with this SW installation. The protocol used is a demonstration network and does not fully utilize the capabilities of the hardware. This protocol is not to be used to estimate IEEE802.11 performance. It simply provides connectivity.

After installation of the SW any network aware Windows for Workroups application can be used to demonstrate network connectivity.

### **Utility Software**

### Introduction

The Wireless LAN Utility SW, a DOS application, provides the capability to evaluate the performance of the Physical Layer of the radio in terms of PER and to load MAC executables into the Flash device on the adapter card.

The PER tool configures a transmit node and one or more receive nodes to perform PER measurements. The receive nodes can be placed at various distances and areas relative to the transmitter. In addition, these receivers can be subjected to various sources of interference. An experiment with multiple receivers will provide data to compare radio PER performance of the various topologies and under different interference sources.

The transmitter sends data packets with user-programmable data length. The data is random and protected by a CRC. The receiver checks the CRC and if the CRC is in error a packet error is declared. In addition each packet has a sequence number and the receiver can determine any missed packets by accounting for the missing sequence numbers. The receiver calculates the PER based on the missed packets and the packets that were detected with errors.

#### Installation

To install the PRISM WLAN Card utility software load the "Wireless LAN Utility Software" floppy into your floppy disk drive and type a:\setup at the DOS promt.

You will be given the opportunity to select the source and destination directories. The defaults are almost always adequate. To select the default, simply press ENTER. To change source or destination directories, type in the complete path of the directory you wish to override.

The selected source and destination directories will be displayed and you will be asked whether or not to proceed. To cancel installation, select "N". To proceed with the installation, select "Y".

The installation routine will create target directories and copy source files to their proper locations.

### Usage

To run the PRISM WLAN Card Utility, change directory into the installation directory (default is c:\prism), type "PRISM" and press ENTER.

Once in the program, you will be presented with the main screen which will allow you to perform several functions.

Selecting the "Load Diagnostic Firmware" option will automatically turn on the card, load the diagnostic firmware and turn off the card. You will then return to the main screen.

Selecting the "Load Network Firmware" option will automatically turn on the card, load the network firmware and turn off the card. You will then return to the main screen. While the program is loading the Network firmware it will ask you for a 7-digit serial number. Enter a random 7-digit number and follow any other directions when prompted.

Selecting the "Start Packet Transmitter" will call up the transmit screen. This turns on the card (which should be loaded with the diagnostic firmware) and prepares to transmit data packets. The desired radio channel on which to transmit and the desired packet size should be selected. Once the transmitter has been configured properly, start the transmitter. The program immediately starts to transmit packets and updates the screen to reflect how many packets have been sent. To stop the packet transmitter, select "Stop Tx". To exit transmit mode, select "Exit Packet Tx". This will turn off the card and return to the main screen.

Selecting the "Start Packet Receiver" on another PC/radio setup will call up the receive screen. This turns on the card (which should be loaded with the diagnostic firmware) and prepares to receive data packets. The desired radio channel on which to receive packets should be selected at this point. Once you are satisfied with the receiver setup, start the receiver. At this point, the program waits for a good packet to arrive. Once the program has a good packet it begins packet error rate calculation and starts updating the screen. To stop the packet receiver, select "Stop Rx". To exit receive mode, select "Exit Packet Rx". This will turn the card off and return to the main screen.

As mentioned above several parameters are user programmable for the transmit and receive nodes.

When "Packet Error Rate Transmitter" is selected from the main menu the following parameters can be set to configure the transmit mode.

### 1. "Transmit Channel" (1-11)

These are the transmit RF channels defined for Direct Sequence Spread Spectrum (DSSS) in the IEEE802.11 draft 4.0. The default value is Channel 1

"Packet Size". This is the packet length and can be anything from 6 bytes to 2040 bytes. The default value is 256 bytes

When "Packet Error Rate Receiver" is selected from the main menu then the receiver node can be configured. The parameter that needs to be set is:

 "Receive Channel". This can be Channel 1-11 and it should be identical with that of the intended transmitter for this receiver. The default value is channel 1.

The remaining fields on the "Packet Error Rate Receiver" screen are display-only and are listed below.

- 1. "Good Packet Count" Count of all errorless packets.
- 2. "Bad Packet Count" Count of all packets with bit error(s).
- "Missed Packet Count" Count of all packets never received.
- 4. "Total Packet Count" The sum of 1,2,3 above.
- "Packet Error Rate" (Total Packets Good Packets)/Total Packets.
- "Elapsed Time" The time since the first valid packet was received. This first packet initiates the calculation of the PER.

Note that the duty cycle of the transmissions as well as the rate of the screen updates are pre-programmed and they are not user selectable. These values are approximately 120 msec for the transmit duty cycle and 750 msec for the screen updates.

#### Description

On the transmit side, a packet of the specified length is generated. There are two embedded fields as part of the packet; a 16-bit length field and a 32-bit sequence number field. These fields are followed by the random data of the user specified length and the 32-bit CRC of the data.

The packet is then broadcast on the specified channel with the hardware generated CRC32 appended to the end of the packet. The 32-bit sequence field is incremented in preparation for the next transmitted packet.

The receiver waits for an errorless packet to begin processing. Upon reception of this initial packet, the receiver starts the elapsed time counter and generates a correct expected sequence number. This allows the receiver to synch up to any existing packet transmission stream.

The program continuously polls for a good CRC-32 reception. The receiver is using the length field from the packet header to determine the location of the CRC bits and subsequently determine whether the received packet is error-less or not. A false CRC will increment the "bad packet" count. In addition, the sequence number is checked against the expected sequence number. If the most recent sequence number received is not the next increment of the last one received then, a delta is calculated and the missed packet counter is incremented by the appropriate amount.

Packet error rate is defined to be the sum of the bad and missed packets divided by the total number of packets received. This number is continuously recalculated and redisplayed each screen update.

# APPIOTE

No. AN9665

February 1997

# Harris Wireless Products

# PRISM™ Power Management Modes

Authors: Carl Andren, Tim Bozych, Bob Rood and Doug Schultz



The PRISM™ chip set and reference radio are capable of reduced power operation in many circumstances where communications is not expected for some period of

time. These are controlled by the MAC and involve both sleep modes of the baseband processor and power shutdowns of various RF parts of the radio. The degree to which the radio can be put to sleep depends on the time needed for awakening. The deeper the sleep mode, the less power it takes and the longer it takes to awaken. Some of the reasons for the lengthy awakening time are charging of capacitors and settling of oscillators. For the deepest sleep mode, the baseband processor and synthesizer registers will lose their programming and will need to be reloaded.

The power management function has to take into account the need for imminent communications. In IEEE 802.11 networks. in Point Coordination Function operation, the Access Point (AP) will periodically broadcast Beacon frames to implement the Timing Synchronization Function and to inform various nodes of impending traffic. The beacon period is a field of Beacon and Probe Response frames and is in units of kilomicroseconds where 1kµs is 1024µs. There can be 1kµs to 2007kus in the period, but a typical beacon period is 100kus. It also uses this message to poll for incoming traffic. If a station determines that it is not needed for upcoming traffic, it can enter a power management mode by informing the AP of this fact using Power Management bits within the Frame Control field of transmitted frames. The station must get a response from the AP acknowledging the mode change before entering it. In a power management mode it can doze until the next poll or until awakened by its own host for outgoing traffic. In an extreme power saving mode, the station is given a listen interval where it can skip a number of beacon periods before it needs to awaken and check one. The PRISM™ radios have the capability to use various doze modes depending on the interval between awakenings. Since the 802.11 only specifies one mode with various sleep times, the MAC needs to decide which PRISM™ sleep mode to use.

One additional factor in power management is the need for staying awake long enough to receive the Beacon frame. If a station is transmitting when the Beacon time arrives, the AP will defer until the medium is clear. This means that the station must stay awake for a period which can be much longer than the Beacon frame itself. This awake period is dependent on the operating mode of the network, but is much shorter than the Beacon interval. Since this occurrence is a random event, the station will stay awake until it hears a Beacon and then resume sleep mode.

PRISM™ radios used in non-802.11 networks or applications can use more of the power management modes than can those constrained by 802.11 network considerations. In particular, the radio can be used in high rate TDMA burst modes to send relatively low average data rates efficiently. In these modes, the radios can have more tightly constrained awakening times and do not need to be awake for as long a period.

The power consumed by the PRISM™ radios is also determined by the traffic patterns. In a typical network with 10 stations per AP, the AP can be assumed to be transmitting at least 80% of the time. This is based on the usual case of transferring programs and graphics from the server to the user with a smaller amount of return traffic. This return traffic will most likely be files sent to printers and files saved to a network hard drive. With this scenario, and the assumption that each user will get an equal share of what's left, the transmit time of each user is about 2%. Thus, the total power consumption can be averaged as 98% receive and 2% transmit. This tends to minimize the impact of the transmit current on the battery life of a laptop. This is further reduced by the power management modes.

The PRISM™ radio can have various circuits powered off depending on the sleep mode. The Baseband processor has additional sleep modes that involve turning off clocks or portions of the circuitry. These are detailed below. First, we will examine the circuits that are drawing power. Figure 1 below shows the radio in the normal receive mode. The transmit sections are in the off state. Circuits shown in the shaded blocks are drawing power by virtue of being powered and clocked. This paper is based on the PRISM™ Reference Radio Schematic, Revision 10, dated December 13, 1996. The implementation of Power Savings Modes may differ for various schematic revisions.

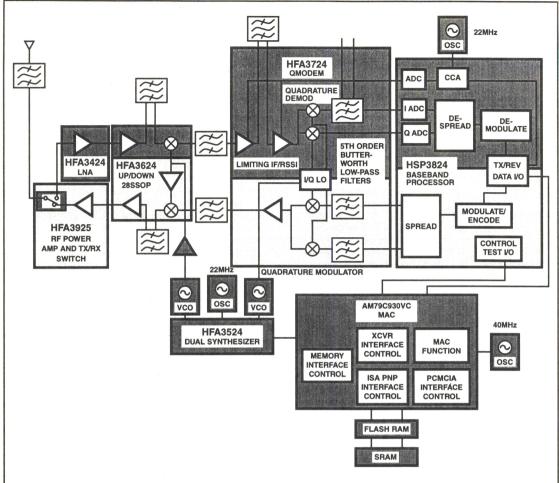


FIGURE 1. PRISM™ PCMCIA REFERENCE RADIO RECEIVE MODE

The power consumption in the various modes are:

TX Current (continuous)	488mA
RX Current (continuous)	287mA
Average Current	
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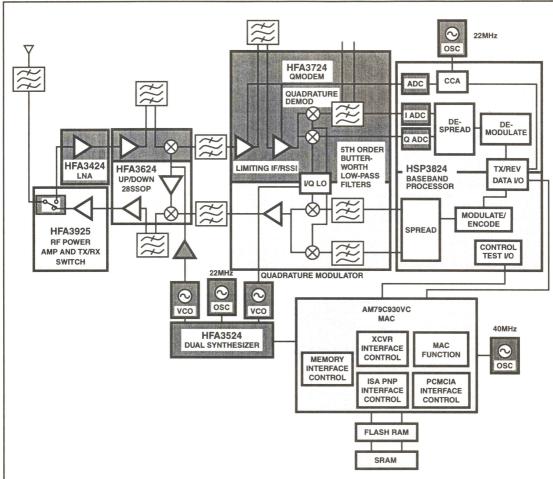
Average Current
Without Power Saving Modes (Note 2) 290mA
With Power Saving Modes (Note 3) 60mA
Power Saving Mode 1 (1µs recovery) (Note 1) 190mA
Power Saving Mode 2 (25µs recovery) (Note 1) 70mA
Power Saving Mode 3 (2ms recovery) (Note 1) 60mA
Power Saving Mode 4 (5ms recovery) (Note 1) 30mA
NOTES:

- 1. Power Savings Mode currents are estimates based on component measurements, estimated power down currents for the AM79C930 and AM29F01055EC, and assuming the removal of the 3 LEDs.
- 2. Average current calculated with 2% transmit current and 98% receive current without power savings modes.
- 3. Average radio current with power savings mode is caculated with 2% transmit, 8% receive, and 90% Power Saving Mode 4.

There are six discrete power control lines in the reference radio that come from the MAC. These are shown below along with their MAC pin connections:

PRISM™	MAC NAME	MAC PIN
PA_PE	TXMOD	131
TX_PEbb	TXMOD	131
RX_PEbb	RX_PE	122
RESET	LPFPE	118
RADIO_PE	USER3	002
RX_PE	TXCMD	126
TX_PE	TXCMD	142

Note that RX\_PEbb and PA\_PE are connected together and of opposite sense. That is, when one is on, the other is off. This makes for a reduction from 7 to 6 control lines.



NOTE: Dark shading indicates full power, while light shading indicates Sleep Mode.

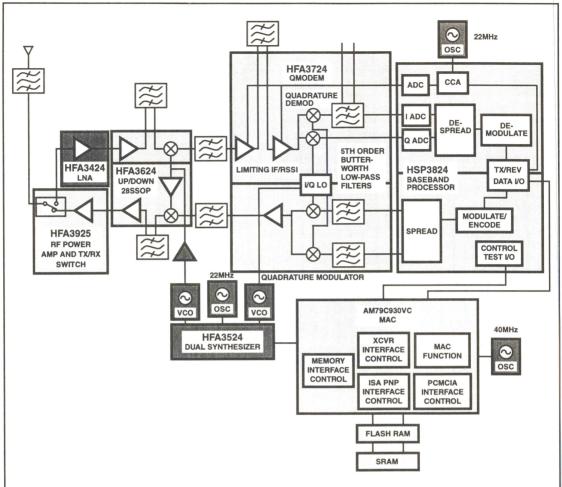
FIGURE 2. PRISM™ PCMCIA REFERENCE RADIO POWER SAVING MODE 1

The power down modes of the radio are controlled by the control signals as follows:

- Receiver Power Enable (RX\_PE and RX\_PEbb) disable the radio receiver functions when inactive.
- Transmit Power Enable (TX\_PE and TX\_PEbb) disable the radio transmitter functions when inactive.
- Reset puts the Baseband Processor into a standby mode when it is asserted after RX\_PEbb goes low.
- Radio Power Enable (RADIO\_PE) disables the entire synthesizer section of the radio which includes the 22MHz Voltage Crystal Oscillator, IF and RF VCOs, HFA3524 Synthesizer, LO Buffer, and Regulator U16.
- In addition, the HFA3524 synthesizer can be put into a power down mode via the synthesizer serial control bus.

CONTROL	STATE
PA_PE	LOW
TX_PEbb	LOW
RX_PEbb	LOW
RESET	HIGH
RADIO_PE	HIGH
RX_PE	HIGH
TX_PE	LOW

Power Saving Mode 1 shown in Figure 2 is where RX\_PEbb and TX\_PEbb are set low to the Baseband Processor (BBP) and the MAC is put in standby mode. This turns off most of the digital logic to save about 100mA of current. Recovery from this mode is 1µs since the previous state of all logic is retained.



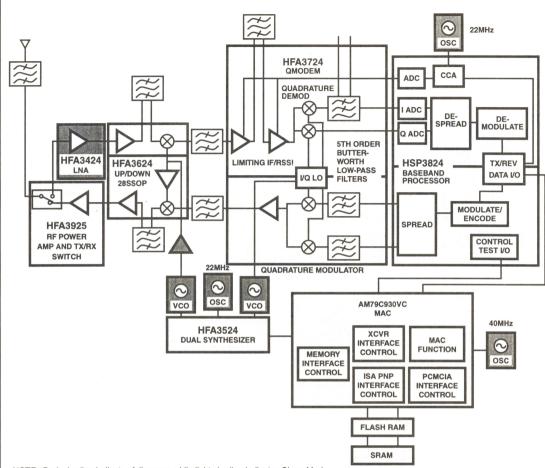
NOTE: Dark shading indicates full power, while light shading indicates Sleep Mode.

FIGURE 3. PRISM™ PCMCIA REFERENCE RADIO POWER SAVING MODE 2

CONTROL	STATE
PA_PE	LOW
TX_PEbb	LOW
RX_PEbb	LOW
RESET	LOW
RADIO_PE	HIGH
RX_PE	LOW
TX_PE	LOW

Figure 3 shows Power Saving Mode 2 that takes  $25\mu s$  to recover. In this mode, the MAC and BBP clocks are stopped as above which reduces the BBP and MAC power consumption to maintenance levels. Additionally, the RESET and RX\_PE lines are set low to put to sleep the BBP ADC section, the 3724 IF to baseband converter and the 3624 RF to IF downconverter.

The AC coupling capacitors must be taken into account when figuring the time it takes to awaken from Power Saving Mode 2. The circuitry in the analog sections has been designed to fast charge these capacitors within  $25\mu s$  and this sets the minimum awakening time. In this mode the lightly shaded blocks have power but their chip control lines have been set to the power down state.



NOTE: Dark shading indicates full power, while light shading indicates Sleep Mode.

FIGURE 4. PRISM™ PCMCIA REFERENCE RADIO POWER SAVING MODE 3

CONTROL	STATE
PA_PE	LOW
TX_PEbb	LOW
RX_PEbb	LOW
RESET	LOW
RADIO_PE	HIGH
RX_PE	LOW
TX_PE	LOW

Power Saving Mode 3 saves an additional 10mA.

The synthesizer has a power down mode that can be controlled by sending a serial control message over the control bus. In this mode, the synthesizer powers down its charge pumps and dividers. It retains essential frequency tuning information, but must be restarted via the serial control bus which takes 2ms. See Application Note 9617 for details.

In addition to setting the seven control lines for Mode 4, one must insure that a low state is programmed on 5 digital lines from the MAC. These digital control paths may cause voltages to be fed through inactive devices and cause undesirable currents to flow. Ensure that the following lines are at a low state in Power Saving Mode 4.

CONTROL	MAC PIN #
Synth L/E	3
Synth CLK	101
Synth Data	102
Sel 0	132
Sel 1	141

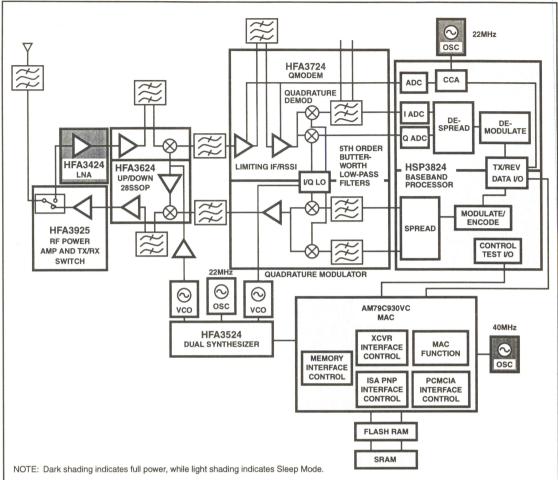


FIGURE 5. PRISM™ PCMCIA REFERENCE RADIO POWER SAVING MODE 4

CONTROL	STATE
PA_PE	LOW
TX_PEbb	LOW
RX_PEbb	LOW
RESET	LOW
RADIO_PE	LOW
RX_PE	LOW
TX_PE	LOW

Power Saving Mode 4, shown in Figure 5, powers down most of the radio in addition to the above. This is done by bringing RADIO\_PE low. This turns off the synthesizer voltage regulator, which causes the synthesizer and its crystal oscillator to power off. In addition, the RF and IF VCOs and the LO Buffer are powered off. The only circuits left with power are the MAC, BBP, RF/IF converter, and 2 crystal oscillators. With the synthesizer unpowered, it looses its frequency tuning register

information. This plus the long settling times of the synthesizer VCOs and crystal oscillators, makes it take 5ms to bring it back up. The MAC and BBP are still powered to maintain register values, but much of the circuitry is static. The MAC oscillator is left running to allow it to respond when the sleep mode changes. The HFA3824 crystal oscillator is still running, although its output is disabled. The HFA3624 is left powered although it is in an inactive mode.

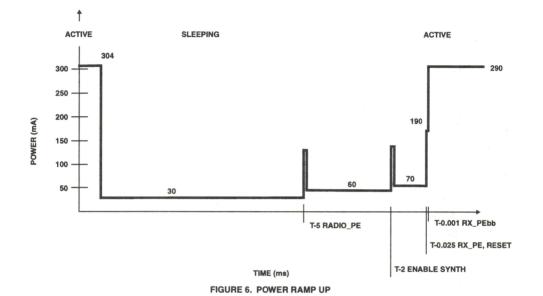
Although this version of the reference radio is not connected for it, one additional mode is available and that is to turn off power to the remaining circuits except the MAC. This mode requires the MAC to spend 1ms to program the BBP registers but this is well within the 5ms time it takes for the oscillators to stabilize.

If the MAC is also powered down to where it is not able to respond to traffic on the PCMCIA Bus, it will miss access on the Bus to which it must respond within 12µs. Circuitry can be added to give a response to the host that the card is not available.

It can be assumed that the power consumption rises as soon as the awakening is started, but the power saving mode can be transitioned slowly back to the fully awake state. With this staging process, it is feasible to enter a given power saving mode whenever the sleep duration is at least as long as the time it will take to awaken. This is of course dependent on the MAC having sufficient processor time to perform the staged awakening.

Figure 6 graphically shows the awakening process. If in PS Mode 4, the awakening process is started at T- 5ms where T

is the time the radio needs to be awake and receiving. First, RADIO\_PE is brought high which transitions the radio to PS Mode 3. There, the synthesizer can be programmed while the various oscillators start up and settle. Then, at T-2ms, the synthesizer is brought out of its standby state. At T-25 $\mu$ s the RX\_PE and RESET lines are brought high. Finally, at T-1 $\mu$ s, the RX\_PEbb line is brought high to enable the demodulation functions. There will be short (10 $\mu$ s) bursts of power here and there while the MAC programs the synthesizer or awakens other circuits.



3-125

# M APPOTE

No. AN9666 January 1997

# Harris Wireless Products

# Wireless LAN Evaluation Kit SW Installation and Usage

Authors: Mike Paljug and Eric Turner (Squires Engineering)



### Introduction

This Application Note describes the driver and application software necessary to demonstrate the 802.11 network capabilities

of the PC Card WLAN Evaluation Kit cards. These cards are based on the Harris PRISM™ Chip Set and the AMD Am79C930 Media Access Controller. Ad hoc network connectivity is provided via alpha 802.11 firmware and an alpha NDIS3 driver. In addition, Windows® 95 application software is provided for evaluating the performance of the physical layer in terms of Packet Error Rate (PER). At this time, the alpha firmware and driver are only able to support 1 Mbit/second operation. Updates will be provided (as they become available) via the Harris Semiconductor World Wide Web page at http://www.harris.com.

## Wireless LAN Connectivity

### Installation

Before installing the adapter it is strongly recommended that you update the BIOS for your PC. The new BIOS should ease the task of resource management for Windows95 and maximize your chances of having a clean installation. First, determine the PC's current BIOS revision. The BIOS revision number is usually displayed during system start-up or in the CMOS Setup. Consult your PC documentation for more information on determining the BIOS revision. Once the current BIOS revision number is known, scan the PC Manufacturer's Website or call the PC Manufacturer in order to determine the most recent BIOS revision for your PC model. If the Manufacturer has a newer revision, download/order it and follow the Manufacturer's instructions for loading it onto your system.

Initial installation of the hardware and software is described in Chapter 2 of the "PC Card Wireless LAN User Guide [1]." During initial installation, Windows95 will attempt to automatically assign the hardware resources required by the adapter (i.e., IRQ, I/O, etc.). Windows95's Resource Manager usually assigns resources appropriately. However, the task is complicated by the absence of a Plug 'n Play BIOS, lack of a PCI bus, and/or the presence of legacy hardware. Error messages encountered during installation should be taken seriously. Consult Microsoft™ Windows95 Resource Kit, call Microsoft Technical Support, or visit the Microsoft Website at http://www.microsoft.com.

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If there are no error or warning messages during installation. you may verify that the card is operating properly by viewing the adapter setup in System Manager. Open Control Panel and then double-click the System icon. This opens up the System Manager, Select the Device Manager index tab. One of the listed items should be Network adapters. If Windows95 thinks there's a problem with the adapter, the adapter will be listed under Network adapters and there will be a vellow exclamation visible next to it. Whether there is a yellow exclamation visible or not, you may view Windows95's resource allocation for the adapter by double clicking its listing. (If the adapter listing isn't visible, double-click the Network adapters listing to toggle between expanding and collapsing the Network adapters list.) If you choose to change the settings for the assigned resources then you do so at vour own risk. Harris does not assume anv liability for hardware or software malfunction.

If a problem exists as evidenced by the vellow exclamation or by an inability to connect or sporadic behavior in Windows95 (machine locks-up during normal operation, screen displays errant behavior, etc.) then you might be experiencing a problem with Windows95 resource management. The minimal testing that has been performed suggests that certain platforms are at less risk than others for these types of problems. Since the software and firmware are in alpha form, Harris Semiconductor is unable to support resource management problems at this time. However, the solution to the majority of problems that have been experienced to date involve changing the Input/Output Range setting. Usually changing this setting to 0200-020F is successful. To do this open Control Panel and double click the System icon. Select the Device Manager tab and then double click the 'Network adapters' listing. Now double click the 'AMD...' adapter listing. Select the 'Resources' tab and highlight Input/Output Range setting. Uncheck the box titled "Use automatic settings" and then select "Change Setting..."

Another rare problem involves the configuration accepted by Windows95's Resource Manager. Two configurations are possible, but in this alpha release both do not work equally well. Configuration 0000 is preferred. To view which configuration has been selected by resource management, open Control Panel and select the System icon. Select the Device Manager tab and then select 'Network Adapters'. Select the 'AMD...' adapter listing and select the 'Resources' tab. The configuration is shown in this window. You may select it by

clicking the arrow next to the configuration listing box. If you have to change this make certain that the memory range is usable. It should range somewhere between C0000h and FFFFh. If it doesn't, you must find an area in this range that does not conflict with any other device. Take the steps outlined in the paragraph above only change the memory setting instead of the Input/Output setting.

#### Usage

After installing the hardware and software as outlined in the User Guide, verify your Windows95 Network setup via the Network icon in Control Panel. Be sure to configure each computer with a unique Computer Name but identical Workgroup. Also, be sure that a client is configured with at least the TCP/IP protocol and that File Sharing is selected. After installation, my setup included the Microsoft Network client with the IPX/SPX. NetBEUI, and TCP/IP protocols and File Sharing.

Once installed and configured properly, the PCs should be visible to each other. Since all networks need time to establish a link database, it is suggested that you wait about 1 minute after entering Windows95 so that the network has time to synchronize. After waiting for this period, double click on Network Neighborhood. You should be able to see the other computer. If the other computer is not visible, try refreshing the view (F5) in Network Neighborhood a few times on both computers.

Now that the other computer is visible, you must share its resources in order to access its hard drive. This is accomplished by entering Explorer, highlighting the drives, folders, or files that you wish to share and right clicking. This will bring up a context menu with a "Sharing..." option. Click the sharing option and make the appropriate selections to give restricted or unrestricted access. The other machine is now able to "see" these shared items and access them according to your wishes.

#### Wireless LAN Evaluation Software

#### Introduction

The Wireless LAN Evaluation Software provides the capability to evaluate the performance of the Physical Layer of the radio in terms of PER and Throughput.

There are two modes: Packet Broadcast and TCP Stream Point-to-Point. The latter mode will gauge throughput under normal full 802.11 protocol conditions. Packet Broadcast mode is used to evaluate PER performance. This mode configures a transmit node and one or more receive nodes to perform PER measurements. The receive nodes can be placed at various distances and areas relative to the transmitter. In addition, these receivers can be subjected to various sources of interference. An experiment with multiple receivers will provide data to compare radio PER performance of the various topologies and with different sources of interference.

It should be noted that current revisions of the firmware and driver do not implement MAC management features and thus attempt transfers at a 1 MBPS rate only without dynamic fragmentation. Furthermore, the current driver defaults to a maximum packet size of 1000 bytes.

#### Installation

Initial installation of the Evaluation software is described in Chapter 2 of the PC Card Wireless LAN User Guide.

Before running the application, you must first verify that the TCP/IP protocol software is installed. To determine this, select "Network" from the "Control Panel". Under the configuration page, the TCP/IP protocol should be present. If it is not present, add it by pressing the "Add" button, selecting "Protocol", selecting "Microsoft" and "TCP/IP".

To configure the TCP/IP protocol, select "Network" from the "Control Panel". Under the configuration page, select the TCP/IP protocol and press the "Properties" button. Under the "IP Address" page, select the "Specify an IP Address" radio button. Enter a valid IP address (we suggest "1.1.1.x," where x = 2 through 200) and a valid subnet mask (we suggest 255.255.255.0). The IP address that you select must not conflict with any other Wireless LAN IP address. The LAN Evaluation software will not establish point-to-point communication if the nodes are not on the same subnet. This requires that the first three fields of the IP address be identical on all Units Under Test (UUTs).

#### Usage

The Lan Evaluation software allows the user to test performance of the 802.11 Wireless Lan evaluation cards. There are two basic modes of operation and under each mode the user must elect to be a transmitter or a receiver. The user must also select the "Test Port". The default value (1025) is usually appropriate and the transmitter must match the receiver.

The two operational modes are:

#### **Packet Broadcast**

Under this mode, the transmitter continuously broadcasts packets with embedded sequence numbers and the receiver automatically synchronizes to the data stream. Missing packets are detected by comparing the embedded sequence number with the expected sequence number. Packet error rate is also continuously calculated and displayed.

#### Stream Point-to-Point

Under this mode, the receiver must be set up to listen for incoming connections and the transmitter must specify the target address before beginning transmission. Once the connection is established, the transmitter begins transmitting data. When using this mode (which relies on the TCP protocol), data is not separated into packets (hence the name "stream") so a measurement of "Packet Error Rate" is meaningless. Instead, what is displayed is a throughput rate. This mode simulates network traffic such as would be encountered during normal network operations (such as file/printer sharing).

#### **Application Note 9666**

Once you have selected a test mode and a test port, you must be a receiver or a transmitter. This calls up the appropriate window.

#### **Common Characteristics**

Both the "Receive Data" and the "Transmit Data" windows have a section at the top which display static information. This information includes the local host name and address, the test mode and test port as selected from the main window, and the remote host address. The remote host address field represents the identity of the remote side of the communication link once it is established. During broadcast transmission, it remains blank since there is no specific destination.

In addition, there is a field which indicates the current state of the communication link. Possible values for this field are:

- 1. Idle
- 2. Listening
- 3. Connecting
- 4. Sending
- 5. Receiving

#### **Receive Data Window**

Below the common section, the receive data window contains two columns of metrics. The number of metrics displayed depends on whether packet or stream mode was selected. The first column of metrics represent "Current" values and the second column represents the "Cumulative" values. The current values are a snapshot of the metrics over the last two seconds and the cumulative values are the metrics since the start of the test.

The following metrics are displayed (only the first three are displayed for stream mode):

- 1. Elapsed Time
- 2. Byte Count
- 3. Kbit/Second
- 4. Good Packet Count
- 5. Bad Packet Count
- 6. Total Packet Count
- 7. Packets/Second
- 8. Packet Error Rate %

To begin receiving data, press the "Start Rx" button. Note that the "Start Rx" button and the "Done" button are disabled and the "Stop Rx" button is enabled. You must press the "Stop Rx" button to terminate the test before you can close the window.

#### **Transmit Data Window**

Below the common section, the transmit data window contains an input section. In the input section are two input fields:

- 1. Remote Address
- 2. Packet Size

Below the input section, the transmit data window contains two columns of metrics. The number of metrics displayed depends on whether packet or stream mode was selected. The first column of metrics represent "Current" values and the second column represents the "Cumulative" values. The current values are a snapshot of the metrics over the last two seconds and the cumulative values are the metrics since the start of the test.

The following metrics are displayed (only the first three are displayed for stream mode):

- 1. Elapsed Time
- 2. Byte Count
- 3. Kbit/Second
- 4. Packets/Second
- 5. Packet Error Rate %

To begin transmitting data, press the "Start Tx" button. Note that the "Start Tx" button and the "Done" button are disabled and the "Stop Tx" button is enabled. You must press the "Stop Tx" button to terminate the test before you can close the window.

#### Reference

For Harris documents available on the web, see http://www.semi.harris.com/ Harris AnswerFAX (407) 724-7800.

[1] "PC Card Wireless LAN User Guide", Celestica Inc., Cy. 1996

## APPIOTE

No. AN9700 March 1997

#### Harris Wireless Products

### Interfacing the CDP68HC05 Microcontroller Family with PRISM™ Wireless Products

Authors: Al Petrick, Kent Rollins, Paul K. Sferrazza



#### Introduction

This application note describes how to interface an inexpensive microcontroller to the PRISM™ chip set to add data communi-

cations capability to a variety of embedded controller applications. The PRISM chip set was designed to provide an integrated solution for Wireless Local Area Network's (WLAN) that are targeted for the IEEE802.11 standard. In this application the Media Access Controller (MAC) must be a high performance part to meet the data rate and the protocol timing requirements. For many wireless communications applications a less expensive microcontroller chip such as the CDP68HC05 family can provide a cost effective solution for both data link control and the embedded application. Such applications include; hand held terminals, consumer remote controllers, motor controllers, data acquisition and low data rate wireless networks for industrial environments.

The CDP68HC05 is an 8-bit microcontroller that can be integrated with the PRISM chip set to create embedded controllers and EDP systems with wireless communications capability. Two options are described in this applications note for interfacing the controller and the radio. The first requires the minimum hardware to implement and directly reads and writes data bits to the data link under software control. This provides a maximum data rate of approximately 300 KBPS. The second option uses a FIFO memory to buffer packets of data that can be transmitted at data rates up to 4 MBPS.

For additional information about the interface and control of the HSP3824 and the overall PRISM chip radio design please see these applications notes and data sheet.

AN9614 "Using the PRISM™ Chip Set for Low Data Rate Applications"

AN9616 "Programming the HSP3824"

AN9617 "Hardware/Software Interface Description for PRISM™ Radio Design with an Example Using

the AM879C930 Media Access Controller"

HSP3824 Data Sheet

Described in this application note is the hardware digital control interface between PRISM chip set and the CDP68HC05

microcontroller. The digital lines controlling PRISM are explained in detailed and illustrated in variety of configurations for data rates up to 4 MBPS.

#### MAC-PHY Digital Control Interface Signals

The MAC-PHY digital control interface to the PRISM chip set consists of 21 digital I/Os. The digital interface is controlled by MAC layer network controller. The network controller uses this interface to configure the internal registers of the HSP3824, perform DC power management, clear channel assessment and transmitting serialized packet data. Table 1 lists the digital signals used in the control interface, as illustrated in Figure 1. The port bits assigned to the CDP68HC05 are arbitrary and user definable. The first column lists the PHY signal name, the second column indicates whether the signal is an output or an input to the CDP68HC05. The next column indicates the port bit assigned, to the control signal. The last column indicates the hardware component description and part number.

#### Data Rate Performance

The data rate performance for the CDP68HC05 is set by the internal bus processing clock. The processing bus clock for the CDP68HC05 is given as:

Internal bus clock = FCLK/2

where: FCLK is external input clock frequency or the clock oscillator frequency.

The maximum input clock frequency for the CDP68HC05 is 8MHz. The internal bus clock more commonly known as machine cycle clock is calculated as 4MHz. The 4MHz clock is used to calculate the minimum time required to transmit or receive a data bit to/from the HSP3824. The HSP3824 has two independent serial communications interfaces (SCI) ports, one for transmit the other for receive. The CDP68HC05 only has one SCI port and is data rate limited. We recommend the bidirectional I/O ports be used for data transmission. Using the bidirectional ports provides flexibility in adapting to the protocol used by the HSP3824 and reducing the need for external timing glue logic. The maximum data rate using the bidirectional ports is 300 KBPS. This assumes an internal bus clock of 4MHz, approximately 12 machine cycles or 4 instructions to read a single bit of data from the RXD line.

#### **Application Note 9700**

TABLE 1. SUMMARY LIST OF DIGITAL CONTROL SIGNALS

SIGNAL NAME	I/O FROM/TO CDP68HC05	PORT ON CDP68HC05	DESCRIPTION		
RXCLK	I PD0		Receive Clock (HSP3824 Receive Port)		
RXD	I	PD1	Receive Data (HSP3824 Receive Port)		
MD_RDY	I	IRQ	MAC Data Ready (HSP3824 Receive Port)		
TX_PE_BB	0	PA5	Transmit Power Enable (HSP3824 and HFA3924 power amp)		
RX_PE_BB	0	PC3	Receive Power Enable (HSP3824)		
TXD	0	PA7	Transmit Data (HSP3824 Transmit Port)		
TXCLK	0	PA6	Transmit Clock (HSP3824 Transmit Port)		
TX_RDY	ı	PA3	Transmit Ready (HSP3824 Transmit Port)		
CCA	I	PA4	Clear Channel Assessment (HSP3824)		
R/W	O PB6 O PC1 I/O PC0		Read/Write Strobe (HSP3824 Control Port)  Chip select (HSP3824 Control Port)  Bidirectional Serial Data Bus (HSP3824 Control Port)		
CS					
SD					
SCLK	0	PB7	Serial Control Port (HSP3824)		
AS	0	PB5	Address Strobe (HSP3824 Control Port)		
SYNTH_LE	0	PC4	Load Enable (HFA3524)		
SYNTH_DATA	0	PC6	Serial Data Bus (HFA3524)		
SYNTH_CLK	0	PC5	Serial Control Clock (HFA3524)		
SYNTH_PE	0	PC7	Synthesizer Circuit Power Enable		
TX_PE	0	PA2	Transmit Power Enable for HFA3724 and HFA3624)		
RX_PE	0	PA1	Receive Power Enable for HFA3724 and HFA3624)		
RESET_BB	0	PC2	HSP3824 Master Reset		

#### Microcontroller Options

The CPD68HC05 8-bit microcontroller family is available in a variety of packaging options from Harris Semiconductor. Harris Semiconductor CDP68HC05C4B CDP68HC05C8D and CDP68HC05 are microcontroller versions that provide 4K/8K of internal mask ROM, 176 bytes of internal RAM, 24 input output signals (I/Os) and a serial communication interface. The CDP68HC05C4B/C8B is available in 44 lead MQFP and PLCC surface mount packages, as well as in a 40 lead PDIP. Figure 1 shows the digital control interface between the CDP68HC05C4B/C8B and the PRISM chip set. This arrangement illustrates the distribution of I/Os between the HSP3824, HFA3524 [5], keypad and display driver. This configuration provides a complete solution for most low cost applications. Various pins from Port A, B, C and D are assigned to control the HSP3824 baseband processor. Port A is used to transmit packetized data and to control the power enable signals of the PRISM. Port B is shared between the HSP3824 control port (used to configure the internal registers) and the keypad interface (Port B pins can be programmed to have internal pullup resistors making them ideal for keypad interfacing). Port C is shared between the HFA3524 Dual Synthesizer circuit, the

HSP3824 control port, and the RX\_PE (receiver power enable) pin of the HSP3824. Port D (a receive only port) is used to receive packetized data. The clock for the CDP68HC05 is an external clock divided down to a frequency of 8MHz from the reference clock. The external clock is fed into the OSC1 input. IRQ is the only active low external hardware interrupt available on the CDP68HC05. Because of the critical timing of MD\_RDY, it is recommended that this signal be connected to the IRQ interrupt pin. MD RDY is an output signal from the HSP3824 indicating a valid data packet was received and is ready to be transferred to the CDP68HC05. MD\_RDY when active, envelopes the data packet on the RXD line excluding the radio synchronization preamble field. The timing for the MD\_RDY signal relative to the RXD line is illustrated in the HSP3824 data sheet. The default polarity of the MD\_RDY signal, as shown in the HSP3824 data sheet, is positive logic - active high. Use of MD\_RDY with the IRQ interrupt requires that the level of MD\_RDY be inverted from its default polarity. To change the level to active low, bit-6 of control register CR9 of the HSP3824 must be programmed to a logic 1.

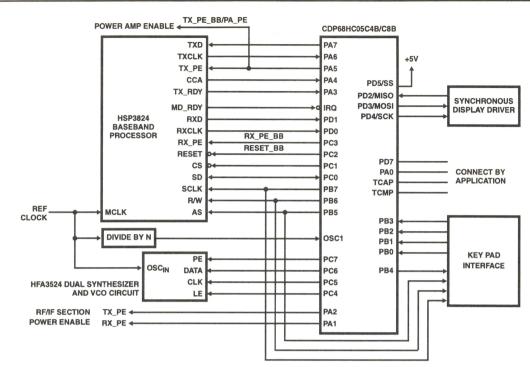


FIGURE 1. CDP68HC05C4B/C8B INTERFACE DIAGRAM

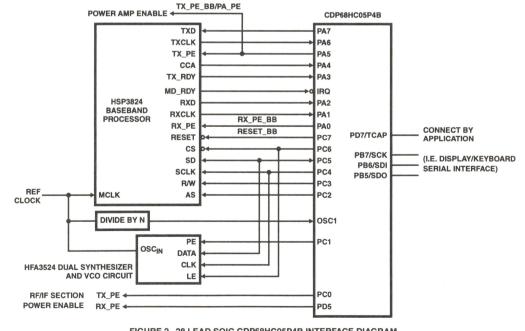


FIGURE 2. 28 LEAD SOIC CDP68HC05P4B INTERFACE DIAGRAM

For applications requiring fewer I/Os the CDP68HC05P4B is an alternative solution. Figure 2 illustrates the digital interface to the PRISM chip set. The device is packaged in a 28 lead SOIC and DIP packages. In this configuration, Ports A and C are shared between HSP3824 and the HFA3524. The signals sharing I/Os are serial data bus, data clock and chip select. Figure 2 illustrates the control signals shared when using the limited I/O version of the CDP68HC05. Selecting between the HSP3824 and the HFA3524 is made by the chip select signal from PC6. When PC6 is low, the HSP3824 baseband processor is selected for configuration. If PC6 is high, the data on PC5 is clock with PC4 into the HFA3524. This configures the synthesizer to the desired frequency.

### Using the CDP68HC05 for High Data Rate Applications

Using the CDP68HC05 8-bit microcontroller with PRISM for data rates between 300 KBPS to 4 MBPS, requires the use of an external FIFO memory between the HSP3824 and microcontroller. Figure 3 illustrates the interface. When using the CPD68HC05 microcontroller in high data rate applications, external FIFO memories is the most efficient interface for transmitting data. The FIFO memories are used to capture a burst of packetized data. Because of the processing bandwidth required for higher data rates and speed limitations of the CDP68HC05, continuous data transmission is not permitted. Packetized data messages like those used in the IEEE802.11 WLAN MAC layer protocol is preferred. The format of the PHY header in the data message is selected by selected by configuring the internal control register CR0 bits 3 and 4 of the HSP3824. There are four PHY header options to choose from. For complete details on field descriptions and programming, refer to the HSP3824 data sheet.

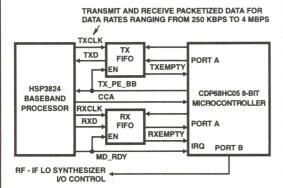


FIGURE 3. EXTERNAL TRANSMIT AND RECEIVE FIFO MEMORY INTERFACE

Two FIFO memories are used, one for the transmit path and the other for receive. The size of the FIFO is determined by the maximum length of the transmitted packet. For most industrial control applications a 512 byte FIFO memory is sufficient. The transmit message consists of a preamble header and data. The data length of the message is variable and counted in bytes. The incoming preamble is used in the acquisition algorithm, synchronizing the HSP3824

demodulator and timing recovery loops. The header is used to determined the start of frame delimiter, modulation type, and the length of incoming message. The CDP68HC05C4B [6], C8B and P4B are limited to 176 bytes of internal RAM. Other family members have more or less RAM (e.g. - 128 bytes for the CDP68HC05J3 [7] and 352 bytes for the CDP68HC05C16B [8]).

The RAM size should be taken into consideration when determining the maximum length of a packet. For most industrial applications the data packets making up a message are relatively short, on the order of 60 bytes. The data in the short packets may represent keypad entry, changes in the display, or motor PWM positioning information. Reserving 100 bytes of the internal RAM for the transmit and receive message buffer in the CDP68HC05 should be sufficient. The data protocol is half duplex and the buffer is shared between the transmit and received messages.

#### Transmitting Data Using FIFO Memories

The protocol used for data transmission is half-duplex. The CDP68HC05 pre-loads the TXFIFO with a data message. The HSP3824 supports two possible data transfer scenarios, one where the preamble and header fields are generated by the baseband processor, and one where the CDP68HC05 generates the preamble and header fields contiguous with data message. If the HSP3824 generates the preamble and header fields, then TX\_RDY is used to enable data transfer from the TXFIFO memory. For this example ignore TX\_RDY and assume the preamble and header fields are combined contiguous with data message. CCA is polled by the CDP68HC05 to determine when RF channel is clear of energy and the transmission will not be subject to collisions. When the channel is clear to transmit, TX\_PE\_BB is asserted by the CDP68HC05 enabling the transmit power amplifier. The HSP3824 begins transferring data from the TXFIFO serially synchronous to TXCLK. During the data transfer TX PE BB envelopes the entire message. The CDP68HC05 is free to perform other tasks during the data transfer. The transfer of data from the TXFIFO memory continues until the CDP68HC05 determines the end of message. The CDP68HC05 determines the last byte of a message by polling the TXEmpty signal from the TXFIFO. TXEmpty becomes active just prior to the last byte transfer from the TXFIFO after the last byte is transferred from the TX FIFO. The occurrence and timing of TXEmpty is depended upon the FIFO memory selected. Once the CDP68HC05 determines the TXFIFO is empty, TX\_PE\_BB is deactivated by the CDP68HC05 disabling the transmit power amplifier, indicating the end of a data transmission.

#### Receiving Data Using FIFO Memories

Receiving a message is independent of transmitting. To receive a message, the CDP68HC05 asserts the RX\_PE\_BB signal. This enables the HSP3824 to acquire, and demodulate an incoming message from the RF medium. Data activity and clock timing become valid on RXD and RXCLK just prior to the detection of the Start of Frame Delimiter (SFD). The HSP3824 checks for a valid SFD, and validates the PHY header fields by performing CRC calcula-

tions. MD\_RDY is an output from the HSP3824 that envelopes the valid data on RXD. MD\_ RDY is programmed to occur after SFD or the CRC field. This is selected by programming CR3, bit-7. MD\_RDY is connected to the enable (EN) on the RXFIFO and the IRQ interrupt on the CDP68HC05. MD\_RDY when active enables the RXFIFO to clock data into the memory from RXD using RXCLK. During the interrupt, the CDP68HC05 transfers data from the RXFIFO memory to the internal RAM. Data transfer continues until the RXEmpty become active or MD\_RDY becomes inactive. If a data collision occurred over the RF medium, MD\_RDY becomes inactive indicating loss of data in the packet, corrupting the message. The user has the option to MD\_RDY during the interrupt cycle for inactivity on MD\_RDY while receiving an incoming packet.

RXEmpty indicates the last byte of incoming message was transferred. After transferring the entire message from the RXFIFO memory, the CDP68HC05 may elect to disable the receiver and go into a power savings mode and process the incoming message. Disabling the PRISM chip set into a power savings mode is controlled by the RX\_PE\_BB, TX\_PE and RX\_PE signals. For details on the timing for transmitting and receiving a message, and power saving options refer to the HSP3824 Data Sheet and Application Note AN9617.

#### References

For Harris documents available on the web, see http://www.semi.harris.com/ Harris AnswerFAX (407) 724-7800.

- AN9614, Harris Semiconductor Application Note. AnswerFAX doc. #99614.
- [2] AN9616, Harris Semiconductor Application Note. AnswerFAX doc. #99616.
- [3] AN9617, Harris Semiconductor Application Note. AnswerFAX, doc. #99617.
- [4] HSP3824, Harris Semiconductor Data Sheet. AnswerFAX doc. #4064.
- [5] HFA3524, Harris Semiconductor Data Sheet. AnswerFAX doc. #4062.
- [6] CDP68HC05C4B/8B, HCL04C4B/8B, HSC05C4B/8B, Harris Semiconductor Data Sheet. AnswerFAX doc. #4157.
- [7] CDP68HC05J3, Harris Semiconductor Data Sheet. AnswerFAX doc. #2757.
- [8] CDP68HC05C16B, HCL0516B, HSC05C16B, Harris Semiconductor Data Sheet, AnswerFAX doc. #4249.



No. AN9701 February 1997

#### Harris Wireless Products

### CRC-16 Algorithm for Packetized WLAN Protocols on the HSP3824

Authors: Al Petrick, John Fakatselis

#### Introduction

In packetize RF data transmissions systems, transmitted messages are susceptible to various types of bit errors due to noise, interference, data collisions, and multipath in a given RF channel. The main purpose of error detection algorithms is to enable an RF receiver of a transmitted message to determine if the message is corrupted. There are various types of error detection algorithms to chose from. The most common method for detecting bits errors in messages is through the use of CRCs (Cyclic Redundancy Codes). CRCs are very useful in detecting single bit errors, multiple bit errors, and burst errors in packetized messages. In theory CRCs could be thought of as simply taking a binary message and dividing it by a fixed binary number, with the remainder being the checksum, or more commonly the CRC. The fixed binary number is the divisor commonly called the polynomial. The CRC-16 algorithm is specified by the IEEE802.11 for use in the direct sequence physical layer PLCP (Physical Layer Convergence Protocol). The CCITT CRC-16 is a standardized algorithm with origins to the CCITT standards body. The polynomial for the CRC calculation is a 16-bit function and is given as  $Gx = X^{16} + X^{12} + X^{5}$ +1. The mathematics performed on in calculating the CRC is binary modulo 2 arithmetic, and typically implemented with an XOR function.

#### CRC16 Algorithm Implementation

The HSP3824 implements the specified IEEE802.11 CRC function. The CRC can be programmed to protect the PLCP header fields. Any error detected by the CRC on the header will flag the MAC and the package will be dropped. The HSP3824 can be programmed to process the packet independent of the CRC indication. This mode may be applicable for non - IEEE802.11 applications.

In this mode the HSP3824 can is configured to pass the data to the MAC even when a CRC error has occurred. In this case the MAC can decide on how the packet data can be used.

There are various ways to implement a CRC algorithm in software and hardware. Processing the IEEE802.11 PLCP DS-PHY header is a time critical function, which favors a hardware approach. A typical implementation is illustrated in Figure 1. The CRC calculator illustrated uses a 16-bit D-Flipflop shift register an three XOR gates to perform the modulo

2 arithmetic. Only the coefficient taps in the polynomial are used with the XOR gates for modulo 2 arithmetic. The message is shifted in serially MSB first. The resultant 16-bit parallel output is the remainder, inverted and appended as the checksum of the message. The CRC checker at the receive end needs to be initialized with an all "1's" value. The CRC check engine will calculate the proper sum assuming that an all 1's value has been used as the initialization seed. The CRC generator will lock if it is initially seeded with a value of all zeros. This initial condition needs to be avoided.

#### CRC16 Protected Fields in the PLCP Header

The CCITT CRC-16 is calculated bit serially in the HSP3824 protecting the Signal, Service and Length fields of the PLCP header. Figure 2 illustrates the Preamble and PLCP header used for IEEE802.11 data transmission. This feature is enabled in the HSP3824 by asserting bits 3 and 4 of control register CR# 0 to a logic "1". Before the PLCP header is transmitted a CRC-16 checksum calculated and appended to the length field. The Signal, Service and Length fields of the PLCP header are clocked bit serially (MSB) first through a shift register, and multiplied by tapped branches corresponding to the polynomial  $Gx = X^{16} + X^{12} + X^{5} + 1$ . Typically CRC algorithms initialize their shift registers to some known value. For the IEEE802.11 algorithm a value of all ones has been chosen. The initialization value has no impact on the performance of the CRC calculation. Initialization only provides a starting point for processing the checksum. In some cases, it is possible for the data in the signal and service fields to be zero values.

After the 32 bits of the PLCP header are shifted into the CRC calculator, the remainder a 16-bit value is configured into a 16-bit word, logically inverted and appended to the length field as its own field. At the receiving DS-PHY, the incoming message, is processed through the same algorithm after the detection of a valid SFD (start-of-frame delimiter). The CRC-16 is recalculated on the PLCP header and compared against the transmitted value for bit error discrepancies. If the calculated checksum of the received message differs for the transmitted appended value, then the message is declared corrupt and discarded.

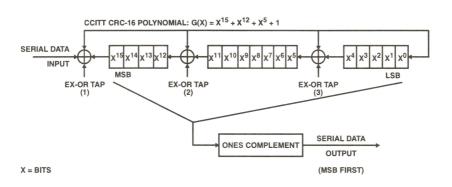


FIGURE 1. CCITT CRC-16 IMPLEMENTATION

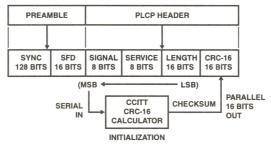


FIGURE 2.

## APPROTE

No. AN9711 March 1997

#### Harris Wireless Products

### Using the PRISM™ HFA3761 Evaluation Board (HFA3761EVAL) Preliminary Release



#### Introduction

The HFA3761 is a highly integrated IF AGC strip and baseband down converter for wireless data applications. It

features all the necessary blocks for baseband demodulation of "I" and "Q" quadrature multiplexing signals. It targets demodulation applications requiring high linearity and AGC capabilities. Four fully independent blocks adds flexibility for numerous applications covering a wide range of IF frequencies. Figure 1 depicts the simplified block diagram of the HFA3761.

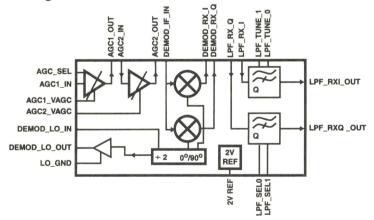
The HFA3761 has a two stage integrated AGC amplifier with frequency response to 400MHz. These amplifiers exhibit a cascaded voltage gain of 82dB and an AGC range of 76dB. A down conversion pair of quadrature doubly balanced mixers are available for "I" and "Q" baseband IF processing. These converters are driven by an internal quadrature LO

generator which exhibits a broadband response with excellent quadrature properties. For broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency for demodulation. A buffered, divide by 2, LO single ended  $50\Omega$  selectable output is provided for convenience of PLL designs. The receive down converter mixers "I" and "Q" outputs have a frequency response up to 30MHz for Baseband signals

A bank of baseband 5th order Butterworth low pass filters are also included in the design. The "I" and "Q" filters address applications requiring low pass and antialiasing filtering for external baseband threshold comparison or analog to digital conversion in the receive channel.

Four filter bandwidths are programmable, (2.2MHz, 4.4MHz, 8.8MHz and 17.6MHz) via a two bit digital or hardwired control interface. These cut off frequencies are selected and can be fine tuned for optimization of 3dB bandwidths.

#### Simplified Block Diagram



#### **Board Description**

An electrical schematic of the evaluation board is shown on Figure 2. The typical application diagram shown on page 3 of the HFA3761 Data Sheet has been implemented with few modifications to aid to the evaluation of the device in typical applications.

Pull up resistors to  $V_{CC}$  of 4.7K have been added to the control pins together with shorting jumpers to ground to facilitate setting up the device into the power standby mode as well as the programmable Low Pass Filters. Please refer to figure 2 and the pin description section of the Data Sheet.

The IF input to the AGC amplifier is internally matched to  $50\Omega$ .

The receive I/Q outputs are terminated on board with  $2k\Omega$  resistors

A potentiometer and a resistor totalling  $1k\Omega$  has been added to the Low Pass Filter fine tuning pins for convenience of the evaluation.

The layout addresses an option to connect pin 50 (LO\_GND) to ground. This pin has been left disconnected from ground in the present layout. A solder bridge must be placed from pin 50 to pin 51 when the LO\_OUT signal is required. In addition, the layout provides capabilities (shown as optional) for independent evaluation of the AGC amplifiers. The optional components have not been populated.

Some of the optional components are related to a interstage AGC filter which has been removed to enable broadband evaluation of the device. This filter adds very little to the performance of the device.

#### Description of Ports and Jumpers

**LO\_IN:** LO  $50\Omega$  input port. Typical input level of -6 to -15dBm and frequency twice the demodulation frequency. Frequency range from 20 to 800MHz.

**IF\_IN:** IF input Port terminated into  $50\Omega$ . Incoming frequency from 10MHz to 400MHz. Levels can vary from -86 to 0dBm with proper adjust of AGC voltage.

RXI\_OUT/RXQ\_OUT: Baseband output ports. Signals are after Low Pass filtering and must be adjusted by the AGC DC voltage to be limited to max 500mVpp for distortionless demodulation. These ports cannot drive loads lower than  $2K\Omega$ .

**AGC\_CTRL:** AGC control DC input. Typical values from 1 to 2V<sub>DC</sub>. Existing board bypass capacitor may limit AGC step response.

2V<sub>REF</sub>: 2V reference output.

JVCC: Jumper to monitor the supply current for the AGC amplifiers only. To be removed in next revision.

**RXPE:** Shorting this terminals will place the device in the standby mode (disabled).

**SEL1/SEL0:** Pull up terminals for filter cutoff setting. Shorting the terminals will set the respective input to low (GND).

#### Evaluation Notes (Version A)

Proper antistatic procedures must be used when handling the HFA3761 Evaluation Board.

This board has an open loop AGC characteristic. A clean DC voltage source from  $1V_{DC}$  to  $2V_{DC}$  range must be utilized in order to maintain constant 500mVpp output at the baseband. Notice that at full gain, the output may show distortion due to the saturation of the Low Pass filtersand improper AGC DC control level. Please consult the data sheet.

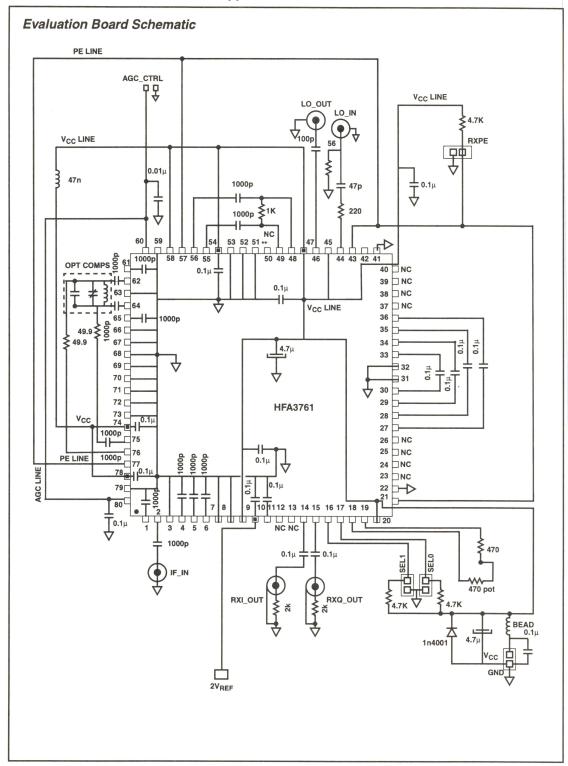
The HFA3761 DC voltage AGC control requires a DC source with sink and source capabilities. Please refer to Note 3 and reference DC Electrical Specification on page 6 of the HFA3761 Data Sheet.

Please terminate the LO\_OUT output port into  $50\Omega$  when enabling the LO\_OUT output option.

When evaluating power consumption in stand by mode, please remember that most of the jumpers are pull up resistors which can add up to the total I<sub>CC</sub> when jumpers are placed to ground.

Do not add significant external capacitive loading to the I/Q receive ports. Measure these ports with low capacitance scope probe adapters or high impedance low capacitance vector voltmeter probes. High impedance low capacitance active probes for network analyzers can also be used.

The pot  $R_{TUNE}$  can assume very low values when evaluating the tuning range. It is advisable to contain this value within a  $\pm 30\%$  of the center value. Too low values can cause power up problems to the LPF biasing scheme. The resistance value can be read with an ohmmeter when the device is turned off.



## APPIOTE

No. AN9712 March 1997

#### Harris Wireless Products

## Using the PRISM™ HFA3763 Evaluation Board (HFA3763EVAL) Preliminary Release



#### Introduction

The HFA3763 is a highly integrated baseband converter for quadrature modulation applications. It features all the

necessary blocks for baseband modulation of I and Q signals. An output AGC and Baseband shaping filters are integrated in the design. Four filter bandwidths are programmable via a two bit digital control interface. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. The modulator channel receives digital or analog I and Q data for processing. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency of modulation. A selectable buffered divide by 2 LO output and a stable reference voltage are provided for convenience of the user. The device is housed in a thin 80 lead TQFP package.

#### **Board Description**

An electrical schematic of the evaluation board is shown on Figure 2. The Block Diagram shown in the HFA3763 Data Sheet has been implemented with few modifications to aid to the evaluation of the device in typical applications.

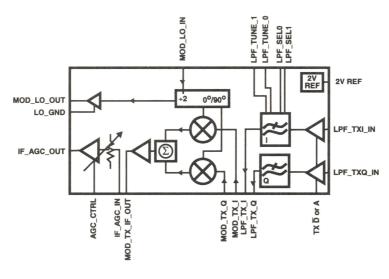
Pull up resistors to  $V_{CC}$  of 4.7K have been added to the control pins together with shorting jumpers to ground to facilitate setting up the device into standby mode, as well as the programmable Low Pass Filters.

The IF output from the AGC/Attenuator is matched to  $50\Omega$  using a low "Q" dual "L" stage network to a frequency of 105MHz. The device IF port is equivalent to a  $250\Omega$  resistor in parallel to 1.5pF.

The transmit inputs are set for analog mode only and the inputs are terminated on board with  $50\Omega$ . Please refer to the pin 20 description of the HFA3763 Data Sheet.

A potentiometer and a resistor totalling  $1k\Omega$  have been added to the Low Pass Filter fine tuning pins for convenience of the evaluation.

#### Simplified Block Diagram



#### **Application Note 9712**

This preliminary layout addresses an option to connect pin 50 (LO\_ GND) to ground. This pin has been left disconnected from ground in the present layout. A solder bridge must be placed from pin 50 to pin 51 when the LO\_OUT signal is required. In addition, the layout provides capabilities (shown as optional) for independent evaluation of the AGC output amplifier. The optional components have not been populated.

#### Description of Ports and Jumpers

**LO\_IN:** LO  $50\Omega$  input port. Typical input level of -6dBm to -15dBm and frequency twice the demodulation frequency. Frequency range can vary from 20MHz to 800MHz but is limited to the existing matching network at the IF\_OUT port.

IF\_OUT: Upconverted IF output. Output is matched to  $50\Omega$  by a low "Q" filter. The output level is a function of the DC voltage applied to the AGC\_CTRL terminal. Max output when AGC DC voltage is 1V or below. Level can be attenuated by means of the AGC\_CTRL voltage beyond 40dB.

**RXI\_IN/RXQ\_IN:** Baseband input ports. The present board has been set for analog input mode only. Please refer to the pin description section of the Data Sheet. Input signals have to be limited to max  $500mV_{P-P}$ . These ports are terminated on board to  $50\Omega$  resistors which can be removed for convenience.

**AGC\_CTRL:** AGC control DC input. Typical values from 1V<sub>DC</sub> to 2V<sub>DC</sub>. Existing board bypass capacitor may limit AGC step response.

2VREF: 2 volts reference output.

**TXPE:** Shorting this terminal will place the device in the standby mode (disabled).

**SEL1/SEL0:** Pull up terminals for filter cutoff setting. Shorting the terminals will set the respective input to low (GND).

#### Evaluation Notes (Version 5)

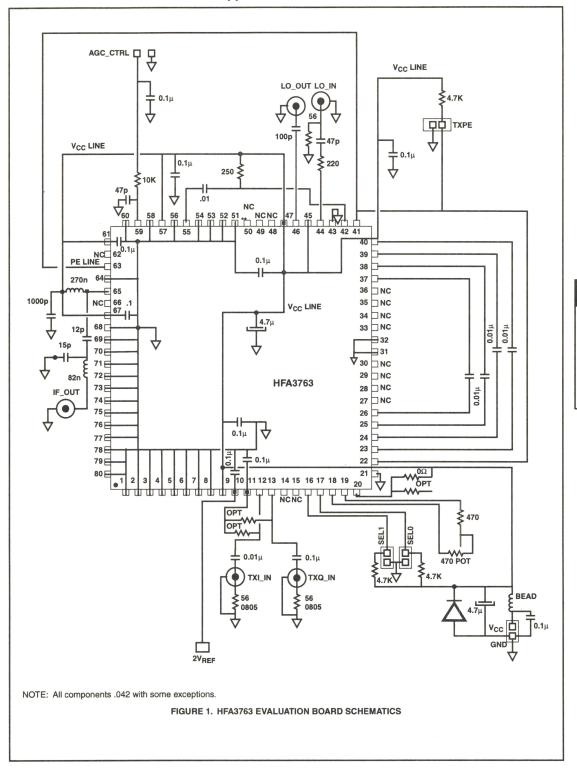
Proper antistatic procedures must be used when handling the HFA3763 Evaluation Board.

Please terminate the LO\_OUT output port into  $50\Omega$  when enabling the LO\_OUT output. Leaving this port mismatched reduces the carrier suppression of the transmit signal.

When evaluating power consumption in standby mode, please remember that most of the jumpers are pull up resistors which can add up to the total  $I_{CC}$  when jumpers are placed to ground.

Proper analog driving capability and rise and fall time balance is important for code leakage evaluation of spread spectrum signals.

The pot  $R_{TUNE}$  can assume very low values when evaluating the tuning range. It is advisable to contain this value within a  $\pm 30\%$  of the center value. Too low values can cause power up problems to the LPF biasing scheme. The resistance value can be read with an ohmmeter when the device is turned off.



## MAPPA OTE

No. AN9713 March 1997

#### Harris Wireless Products

## Using the HFA3663 and HFA3664 Evaluation Board (HFA3663EVAL, HFA3664EVAL) Preliminary Release



#### 

The HFA3663/64 UpConverter with Gain Control are monolithic bipolar devices for up conversion applications in the 2.0 to 2.3GHz

and 2.3 to 2.7GHz ranges. Manufactured in the Harris UHF1X process, these devices consist of a double balanced mixer followed by a variable gain power preamplifier. An energy saving, TTL Compatible, power enable input provides on/off bias current control to the mixer and amplifier. These devices require low drive levels from the local oscillator and are housed in a small outline 20 lead SSOP package ideally suited for PCMCIA card applications.

#### **Board Description**

An electrical schematic of the evaluation board is shown on Figure 2. Access to individual blocks has been given by means of SMA connectors.

Optional cascade paths have been implemented for either individual or cascaded performance evaluation by means of zero ohm surface mount resistors and the use of an on board commercial passband filter. This feature gives the user the ability to evaluate actual cascaded performance or individual blocks. The board is shipped with a HFA3764, a BPF of 2.45GHz and a couple of 3dB attenuator pads.

#### **Description of Ports and Jumpers**

**IF\_IN:** Upconverter mixer input port.  $50\Omega$  termination.

**TXM\_RF:** Upconverter mixer output port. This port is disabled at shipping as the board has been assembled for cascaded evaluation.

**RXM\_LO:** Mixer LO input port. Terminated on chip into  $50\Omega$ , it is optimized for -8dBm signal inputs.

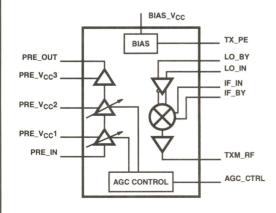
**PRE\_IN:** AGC Preamplifier input port. This port is disabled at shipping as the board has been assembled for cascaded evaluation.

**PRE\_OUT:** AGC Preamplifier output port.  $50\Omega$  termination. The output level is dependent on the DC voltage applied to the VAGC terminal.

VAGC: AGC control DC input. Typical values from 1VDC to 2VDC. Bypass capacitor may limit AGC step response. A shorting jumper on these terminals puts the device in its maximum gain.

**PE:** A shorting jumper connecting to  $V_{CC}$  placed into these terminals activates the device. Removing the jumper places the device into standby mode. Please refer to the HFA3663 and HFA3664 data sheets.

#### **Block Diagram**



#### **POWER CONTROL TRUTH TABLE**

STATE	TX_PE	
Power Down - Energy Saving Mode	Low	
Transmit Mode	High	

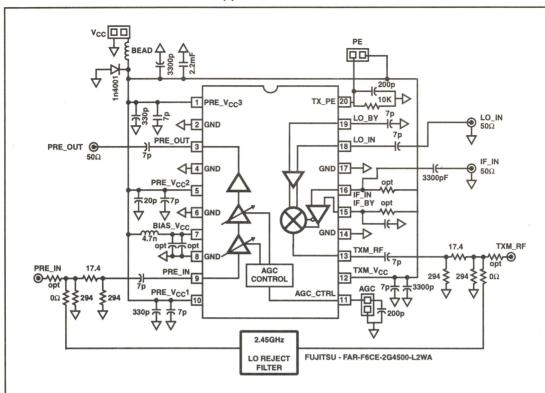


FIGURE 1. HFA3663/4 EVALUATION BOARD SCHEMATICS

#### **HFA3663/64 EVALUATION BOARD PARTS LIST**

PART NUMBER	DESCRIPTION	MFG/VENDOR	TOTAL			
		FLEACE				
DDEI IMINARY RELEASE						
1116	A ROLL OF THE PARTY OF THE PART					



No. AN9714 March 1997

#### Harris Wireless Products

### Using the HFA3661 Evaluation Board (HFA3661EVAL) Preliminary Release



#### Introduction

The HFA3661 RF/IF converter is a monolithic bipolar device for down conversion applications in the 2.0GHz to 2.7GHz

range. Manufactured in the Harris UHF1X process, the device consists of a low noise amplifier and down conversion mixer. An energy saving power enable control feature assures isolation between transmit and receive channels for TDMA and/or half duplex systems. The device is designed for a high Output IP3, while maintaining low current and true 2.7V minimum supply operation. It requires low drive levels from the local oscillator and is housed in a small outline 20 Lead SSOP package ideally suited for PCMCIA card applications.

#### **Board Description**

An electrical schematic of the evaluation board is shown in Figure 2. Access to individual blocks have been given by means of SMA connectors.

Pull down resistors are used for functions as device disable and LNA bypass mode. Please refer to the pin description in the HFA3661 Data Sheet,F/N AnswerFAX Document No. 4240.

#### Description of Ports and Jumpers

**RXA\_IN:** LNA input port.  $50\Omega$  termination.

**RXA\_OUT:** LNA output Port.  $50\Omega$  output termination. Although full individual evaluation of the LNA is possible, this port is often connected in cascaded mode by means of an external image rejection filter connected to the mixer input (RXM\_RF) at the frequency range of interest.

**RXM\_RF:** Mixer RF input port.  $50\Omega$  termination.

**RXM\_LO:** Mixer LO input port. Terminated on chip into  $50\Omega$ ; it is optimized for -8dBm signal inputs.

**RXM\_IF\_OUT:** Mixer IF output port. Existing matching network to  $50\Omega$  centered at 70MHz.

**JP1:** A shorting jumper connecting to  $V_{CC}$  placed into these terminals activates the entire device. Removing the jumper shuts down the entire device into standby mode.

**JP2:** A shorting jumper connecting to  $V_{CC}$  placed into these terminals activates the LNA bypass mode where the gain is switched to an attenuation for strong incoming input signals.

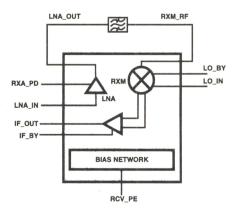


FIGURE 1. SIMPLIFIED APPLICATION DIAGRAM

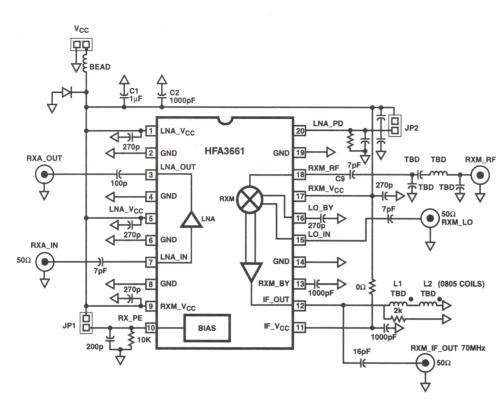


FIGURE 1. HFA3661 EVALUATION BOARD SCHEMATICS



No. TB337.1 May 1996

#### Harris Wireless Products

#### A Brief Tutorial on Spread Spectrum and Packet Radio

Author: Carl Andren



#### Introduction

The new communications standard for wireless local networks, IEEE 802.11, uses spread spectrum and packet

radio techniques and these are features which are not common knowledge. The first term, spread spectrum, indicates a radio frequency modulation technique where the radio energy is spread over a much wider bandwidth than needed for the data rate. We do this to get some benefits that are not readily apparent. The easiest spread spectrum technique to explain is frequency hop (FH). In this technique, the channel being used is rapidly changed in a pseudo random pattern so that the communications appears to occupy a wide bandwidth over time. See Figure 1. This spreads the energy out so that the average power in any narrow part of the band is minimized. Of course, the transmitting and receiving radios need to synchronize their hopping patterns so that they hop together.

As an example, 802.11 specifies that we use the ISM band at 2.4GHz. The ISM band is 83MHz wide and has been subdivided into 1MHz channels for the FH specification. The FCC insists that any spread spectrum FH radio operating in this band must visit at least 79 of the channels at least once every 30 seconds. This works out to a minimum hop rate of 2.5 hops per second.

The next form of spread spectrum is called Direct Spread (DS) and this is the other form of spread spectrum allowed by the FCC in this band. With DS, the data is mixed (XOR) with a high rate pseudo random sequence before being PSK modulated onto the RF carrier. This high rate sequence can be many orders of magnitude higher in rate than the data. In the ISM band, it is limited to not less than a 10:1 spreading ratio. This high rate phase modulation spreads the spectrum out while dropping the power spectral density. This means that this kind of signal will interfere less with narrow band users. It also has some interference immunity to those narrow band emitters. The receiver processing of DS signals begins with despreading the signals. This is done by mixing the spread signal with the same PN sequence that was used for spreading. See Figure 2A. This collapses the desired signal to its original bandwidth and form. It meanwhile spreads all other signals that don't correlate with the spreading signal. Thus a narrowband interference will get spread in this operation and will not fit through the narrow data filter. See Figure 2B. When the signal energy is collapsed to the data bandwidth, its power spectral density is increased by the amount of the processing gain which is proportional to the bandwidth reduction. Thus a signal that was received at or below the noise floor, is now above the noise and can be demodulated.

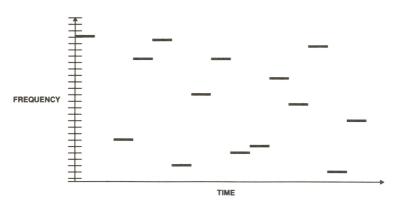


FIGURE 1. FH SPREAD SPECTRUM

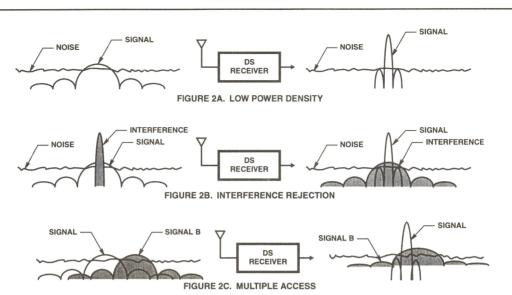
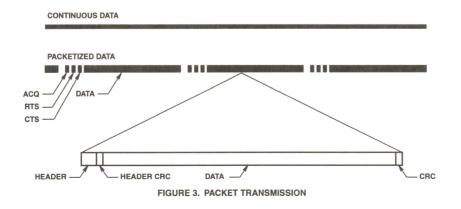


FIGURE 2. DIRECT SEQUENCE SPREAD SPECTRUM PROPERTIES

Finally, DS spread spectrum can allow more than one user to occupy the same channel through a feature called multiple access. Each DS receiver collapses only correlated signals to the data bandwidth. Other, non correlated signals will remain spread in this step. When the desired signal is filtered to the signal bandwidth, only a small fraction of the undesired signal remains. See Figure 2C.

The term packet radio or packet communications is common where the communications medium is not well controlled. There are numerous reasons why a radio communications link may be interrupted, such as the microwave oven. [1] The microwave oven radiates in the middle of the ISM band with a 50% duty cycle and a pulse rate locked to the power line. Thus it is off for 8ms every 16ms. These off periods allow the transmission of bursts (or packets) of 1000 bytes at a time. Frequency hopping also means that the radio communications is interrupted every 400ms while the sending and

receiving radios are retuned. The breaking up of a large block of data into small "packets" is a common technique in communications to insure that error free communications can take place even with interruptions. [2] If the medium is corrupted intermittently, a large block of data will never make it through without errors. In the packet technique this block is broken into small packets that each have some error detection bits added. Then, if an error is detected, a retransmission of the small packet that was corrupted will not unduly burden the network. This packet communications technique has short control packets that check to see if the medium is clear, the other end is ready to receive and, to request a retransmission if a packet did not get through correctly. See Figure 3. All of this requires some overhead expense that reduces the net system throughput. Packet length can be optimized to minimize overhead while insuring the greatest throughput with data integrity.



When continuous data is packetized, the instantaneous rate must increase since the time allowed for data transmission is reduced. This allows time for the packet protocol interchange, packet headers and other overhead. Packet communications can be used with various access protocols such as carrier sense multiple access (CSMA) or time division multiple access (TDMA). CSMA allows asynchronous communications, but requires each communicator to first establish that the medium is not busy. It then establishes the link with an interchange consisting of a request to send (RTS), followed by a clear to send (CTS), the data packet and acknowledgment or not (ACK/NAK). TDMA allows synchronous communications where each user is allocated a time slot to communicate in. The network overhead in this scheme is in the wasted time when some users have nothing to send and in the packets from the controller necessary to allocate the time slots.

The combination of spread spectrum and packet communications for the 802.11 wireless local area networks allows robust communications in a crowded and noisy band.

#### References

- [1] The 2.4GHz ISM band has been called the Junk band because it is already contaminated by oven emissions. Years ago, 2.43GHz was allocated to the microwave oven and it was felt that no one else would ever want to co-occupy this band. As pressure to allocate more spectrum to communications was felt, the FCC set up rules for unlicensed Instrumentation, Scientific and Medical (ISM) operation in this "worthless" band.
- [2] Remember the days of typewriters where typing a whole page without error was a trying experience. The first word processor that allowed you to look over and correct each sentence before committing it to paper was a real breakthrough.

## M Teas Brief

No. TB338 June 1996

#### Harris Wireless Products

#### Using the PRISM™ Chip Set for Timing Measurements (Ranging)

Authors: Carl Andren and Perry Frogge



Many applications use the properties of Direct Sequence Spread Spectrum to establish accurate timing which is useful for ranging and time dissemination. DS receivers use a wide

bandwidth and correlation techniques to measure the time of arrival of signals to a high degree of accuracy. While the PRISM™ chip set was not designed specifically for this, it does, however, have all the required assets to do medium accuracy time of arrival measurements.

It is quite simple to use the PRISM™ radio for accurate timing measurements. All of the timing information is available from the HSP3824 Baseband Processor. At the sending end, the asynchronous rising edge of TX PE will reset the counter of the internal transmit state machine which will output the header and data a fixed amount later. This is timed to within one MCLK (22MHz), so there is an ambiguity of 0.5 MCLK (45ns) in this time. Additionally, the setup to hold time of TX PE to MCLK is not specified in the data sheet. This can, however, be included in the calibration measurements. Thus, all you have know is the offset between MCLK and the source timing to get even better resolution. This offset can be sent in the data portion of the message. The length of the preamble and header is fixed (128 + 64 = 192), so the start of data is at a fixed offset in bits.

On the receive side, MD\_RDY is output after the CRC-16 check. Thus it indicates the precise time the first bit of the data part of the message is received. This is, of course, 192 bits after the arrival of the first bit of the packet. The MD\_RDY offset from MCLK also needs to be taken into account to resolve the overall offset between the correlation and the signal timing to within a fraction of MCLK. On the data sheet, this is listed as  $t_{\rm D3}$  which has a maximum value of 25ns.

The accuracy the receiver is going to get in capturing the asynchronous correlation peak in the header is ±0.25 MCLK or about 11ns. To improve on this, more heroic processing can be attempted. Over the length of the message, the timing can be refined further by averaging, as long as there is an offset between the RX and TX clocks. That is, the timing will slowly drift and be reset, allowing the external system to judge when in the process the timing was at the peak. Since this occurs half way between resets, it is not too hard to find. Thus, the ultimate receive time accuracy is probably about 0.1 MCLK or 5ns. This ultimate accuracy will take some extra computation to achieve.

To the time of arrival measurement you need to add the propagation delay of ~1ns per foot, delays in the RF and IF filters and in other devices in the path. The propagation delay could be longer if a multipath signal is the one chosen by the receiver due to the direct path being blocked.

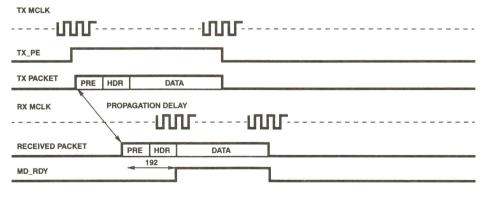


FIGURE 1.

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#### Tech Brief 338

In using this capability, the designer will need to take accurate measurements to calibrate the delays encountered in the PRISM<sup>TM</sup> hardware. Since the baseband processor is a state machine, its delays will be fixed offsets from the MCLK with minor variations over temperature and production tolerances.

Figure 1 shows some of the elements of the delay. The scale is not accurate; specifically, the clock rate is grossly under represented for clarity.

The total delay from initiation to response is as follows:

 $T_D = t_{T.M} + t_{D2} + t_{T.X} + t_{IF} + t_{RF} + 192\mu s + t_{PROPAGATION} + t_{RF} + t_{IF} + t_{RX} + t_{MCLK} + t_{D3}$ 

Where:

T<sub>D</sub> = total delay (TX\_PE to MD\_RDY)

t<sub>T-M</sub> = delay from TX\_PE to next rising edge of MCLK

t<sub>D2</sub> = MCLK to TXCLK delay

 $t_{Tx}$  = delay through the transmit state machine to IF

t<sub>IF</sub> = IF filter and amplifier delays

t<sub>RF</sub> = RF filter and amplifier delays

192µs = length of preamble and header

tpropagation loss due to speed of light (about 1ns per foot)

t<sub>RF</sub> = RF filter and amplifier delays

t<sub>IF</sub> = IF filter and amplifier delays

 $t_{\text{Rx}}$  = delay through the receive processing from IF

 $t_{\mbox{\scriptsize MCLK}}$  = accuracy of tracking the actual received timing to the local MCLK

t<sub>D3</sub> = MCLK to MD\_RDY delay

All processing operations are timed by the transmit and receive MCLKs (22MHz) which can be also slaved to or shared with the source's and sink's clocks. If 802.11 compliant operation is not needed the MCLK can be other than 22MHz to allow sharing with the application.

# APPLICATIONS FOR COMMUNICATION ICs

4

#### WIRED COMMUNICATIONS

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#### Harris Semiconductor

## M APPIOTE

No. AN9537.2 January 1997

#### Harris Telecom

## Operation of the HC5513, HC5526 Evaluation Board (HC5513EVAL, HC5526EVAL)

Authors: Don LaFontaine and Ed Berrios

#### **Features**

- · Includes the Ringing Relay
- Toggle Switch Programming for Logic States
- Convenient Monitoring of DET via LED or Banana Jack Output
- Provides Easy Interface of Transhybrid Circuit Using Off Board CODECs Internal Op Amp

#### **Applications**

 Solid State Line Interface for Digital and Analog Telephone Line Cards

#### Functional Description

The HC5513/26EVAL Subscriber Line Interface Circuit (SLIC) evaluation board has provisions for full evaluation of the voice and DC feeding characteristics of the HC5513 and the HC5526 line interface circuit including the ringing function.

SLIC functional control is provided using the toggle switches E0, E1, C1 and C2. Table 2 lists the states of the SLIC, active detector and  $\overline{\text{DET}}$  output.  $\overline{\text{DET}}$  is available at both a banana jack for monitoring with test instrumentation as well as an LED for visual verification.

#### Applying Power to the HC5513/26EVAL

#### **Power Supply Connections**

The HC5513/26EVAL requires three external power supplies for operation. The supply voltages are labeled on the HC5513/26EVAL as  $V_{\rm CC}$  +5V,  $V_{\rm EE}$  -5V and  $V_{\rm BAT}$ . The limits for all supply voltages are provided in Table 1. The table also includes the typical current of each supply when the SLIC is in the Active mode and terminated with a 600 $\Omega$  load.

**TABLE 1. POWER SUPPLY INFORMATION** 

SUPPLY	TYP (V)	TYP (mA)
V <sub>CC</sub> +5V	+5	11
V <sub>EE</sub> -5V	-5	1
V <sub>BAT</sub> , R <sub>SG</sub> is Open Circuit	-28	27
$V_{BAT}$ , $R_{SG}$ is 21.4k $\Omega$	-48	30

#### **Ground Connections**

The HC5513/26EVAL has two separate grounds designated as AGND and BGND. AGND is the analog ground reference for the SLIC. BGND is the battery ground reference, and is to be connected to zero potential. All loop current and longitudinal current flow from this ground. For proper SLIC operation, AGND and BGND must be connected to a common ground, with a potential difference not exceeding ±100mV.

#### HC5513/26EVAL Board SLIC Controls

The design of the HC5513/26EVAL board incorporates five SPDT switches. Four of the switches control the functional state of the HC5513/26 SLIC and the fifth controls the  $\overline{\text{DET}}$  output.

#### **Mode Control Switches**

The four switches labeled E0, E1, C1 and C2 are used to set the operational mode of the SLIC. Each switch is a Single Pole Double Throw (SPDT) switch.

The two inputs labeled E0 and E1 are enable pins. The two pins labeled C1 and C2 are used to select 1 of 4 operating states of the SLIC. Refer to the HC5513/26 Subscriber Line Interface Circuit electrical data sheet for a full description of the functionality of each pin.

#### **DET Select Switch**

A switch is provided on the evaluation board to direct the  $\overline{\text{DET}}$  signal to one of two outputs. With the switch positioned to the right,  $\overline{\text{DET}}$  will illuminate the LED, when positioned to the left,  $\overline{\text{DET}}$  may be monitored at the banana jack using an oscilloscope.

#### Verifying the HC5513/26EVAL Operation

The operation of the HC5513/26EVAL and sample part can be verified by performing five tests. The first four tests require a  $600\Omega$  load, an AC voltmeter and an oscilloscope. The last test requires a telephone and a battery backed AC source. All of the tests require three external supplies, one each for  $V_{CC}$ ,  $V_{EE}$  and  $V_{BAT}$ .

Verify that the sample HC5513/26 included with the evaluation board is oriented in its socket correctly. Correct orientation is with pin 1 pointing towards tip and ring.

Application Tip: When terminating tip and ring on the HC5513/26EVAL it is handy to assemble terminators using a Pomona MDP dual banana plug connector as the terminating resistor receptacle. Refer to Figure 1 for details.

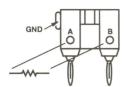


FIGURE 1. TERMINATION ADAPTER

Using the termination shown in Figure 1 provides an unobtrusive technique for terminating tip and ring while still providing access to both signals using the banana jack feature of the MDP connector. Posts are also available that fit into holes A and B, providing a solderable connection for the terminating resistor.

#### POWER SUPPLY CURRENT VERIFICATION

A quick check of evaluation board and the HC5513/26 sample is to measure the currents of each supply voltage. The readings should be similar to the values listed in Table 1. The measurements can be made using a series ammeter on each supply, or power supplies with current displays.

#### Setup

- 1. Connect the power supplies to the HC5513/26EVAL.
- 2. Set V<sub>BAT</sub> to -48V.
- 3. Connect AGND and BNGD to common ground point.
- 4. Connect RRX pin to common ground point.
- 5. Terminate HC5513/26 SLIC with  $600\Omega$  load.
- 6. Set the mode switches to E0 = 0. E1 = 1. C1 = 0. C2 = 1.

#### Discussion

Once setup is complete, apply power to the HC5513/26EVAL and verify the supply currents listed in Table 1. Note that special power supply sequencing is not required for the HC5513/26.

#### **ACTIVE MODE VERIFICATION**

This test will verify that the HC5513/26EVAL can successfully set the HC5513/26 SLIC to Active Mode and that Switch Hook Detect causes  $\overline{\text{DET}}$  to illuminate the LED.

#### Setup

- 1. Connect the power supplies to the HC5513/26EVAL.
- 2. Set V<sub>RAT</sub> to -48V.
- 3. Connect AGND and BNGD to common ground point.
- 4. Connect RRX pin to common ground point.
- 5. Terminate HC5513/26 SLIC with  $600\Omega$  load.
- 6. Set the mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.
- 7. Position the DET select switch to the right.

#### Discussion

When power is applied to the HC5513/26EVAL, loop current will flow from tip to ring and the LED will illuminate. If the LED does not illuminate, verify the mode control switch settings. Once the LED illuminates, remove the  $600\Omega$  termination. This will introduce an open circuit across tip and ring, preventing the flow of loop current and turning off the LED.

#### Verification

- 1. LED is on when tip and ring are terminated with  $600\Omega$ .
- 2. LED is off when tip and ring are open circuit.

#### STANDBY MODE VERIFICATION

This test will verify that the HC5513/26EVAL can successfully set the HC5513/26 SLIC to Standby Mode and that DET can be monitored using the banana jack interface.

#### Setup

- 1. Connect the power supplies to the HC5513/26EVAL.
- 2. Set V<sub>BAT</sub> to -48V.
- 3. Connect AGND and BNGD to common ground point.
- 4. Connect RRX pin to common ground point.
- 5. Terminate HC5513/26 SLIC with  $600\Omega$  load.
- 6. Set the mode switches to E0 = 0, E1 = 1, C1 = 1, C2 = 1.
- 7. Position the DET select switch to the left.
- 8. Connect an oscilloscope or DC voltmeter to the DET jack.
- 9. Monitor the V<sub>BAT</sub> supply current.

#### Discussion

When power is applied to the HC5513/26EVAL loop current will flow from tip to ring and the  $\overline{\rm DET}$  signal will be near zero volts. Disconnecting the 600 $\Omega$  termination will prevent the flow of loop current, and cause  $\overline{\rm DET}$  to be pulled to  $V_{CC}$  rail. In Standby Mode, the  $V_{BAT}$  current should be approximately 16.4mA with the 600 $\Omega$  termination and 0.8mA without the 600 $\Omega$  termination.

#### Verification

- 1.  $\overline{\text{DET}}$  is near 0V when terminated with 600 $\Omega$ .
- 2.  $\overline{\text{DET}}$  is near  $V_{CC}$  rail when not terminated with 600 $\Omega$ .
- 3. V<sub>BAT</sub> current is near 16.4mA when terminated.
- 4. V<sub>BAT</sub> current is near 0.8mA when not terminated.

#### SLIC GAIN VERIFICATION

This test will verify that HC5513/26 SLIC is operating properly and that the SLIC is exhibiting unity gain. Unity gain will only exist if the SLIC is properly terminated with  $600\Omega$ .

#### Setup

- 1. Connect the power supplies to the HC5513/26EVAL.
- 2. Set V<sub>RAT</sub> to -48V.
- 3. Connect AGND and BNGD to common ground point.
- 4. Terminate HC5513/26 SLIC with  $600\Omega$  load.
- 5. Set the mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.
- 6. Connect a sine wave generator to the RRX input.
- 7. Set the generator for 0.775V<sub>RMS</sub> and 1kHz.
- 8. Connect an AC voltmeter across tip and ring.

#### Discussion

When terminated with 600 $\Omega$ , the SLIC will exhibit unity gain from the RRX input pin to across tip and ring. The unity gain results from the matched impedance that the 600 $\Omega$  termination represents to the internally synthesized 600 $\Omega$  of the SLIC. When an open circuit exists, a mismatch occurs and the gain of the SLIC will double.

#### Verification

- 1. Tip to ring AC voltage of 0.775V<sub>RMS</sub> when terminated.
- 2. Tip to ring AC voltage of 1.55V<sub>RMS</sub> when not terminated.

#### RING TRIP DETECTOR VERIFICATION

This test will verify the ringing function of the HC5513/ 26EVAL. A telephone and an AC signal source are the only additional hardware required to complete the test.

#### Setup

- 1. Connect the power supplies to the HC5513/26EVAL.
- 2. Set V<sub>BAT</sub> to -28V.
- 3. Connect AGND and BNGD to common ground point.
- 4. Connect RRX pin to common ground point.
- 5. Set the mode switches to E0 = 0, E1 = 1, C1 = 1, C2 = 0.
- 6. Connect the telephone across tip and ring.
- Connect battery backed AC source to RINGING (V<sub>BAT</sub> + 90V<sub>RMS</sub>) banana jack.
- 8. Position DET select switch to the right (for LED).

#### Discussion

The  $600\Omega$  termination is not necessary for this test since the phone provides this nominal impedance when off-hook. Setting the mode switches as shown above will cause the RIN-GRLY pin of the HC5513/26 SLIC to energize the relay that is on the evaluation board. The D<sub>T</sub> and D<sub>R</sub> comparator inputs will sense the flow of DC loop current, causing the Ring Trip comparator to sense when the phone is either on-hook or off-hook. Refer to the HC5513/26 Subscriber Line Interface Circuit electrical data sheet for a full description of the functionality of the Ring Trip Detector.

#### Verification

- 1. Phone starts ringing when power applied to test setup.
- 2. While ringing and on-hook, DET LED is not illuminated.
- While ringing, going off-hook will illuminate the LED. CAUTION: Short time durations of off-hook should be maintained to protect R<sub>RT</sub>. In systems, the ring relay is software controlled to turn off milliseconds after off-hook is detected hence limiting power dissipated in R<sub>RT</sub>.
- 4. When phone is returned to on-hook, LED will turn off.
- 5. Configure SLIC in Active mode to stop phone from ringing. Set mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.

#### Passive Components

The HC5513/26EVAL design incorporates all of the external components necessary for using the HC5513/26 SLIC in normal applications. A brief description of each component is provided below. The components will be grouped by function to provide further insight to the operation of the HC5513/26EVAL board.

#### Two-Wire Side, Tip and Ring

Relay	Allows injection of ringing signal.
PTC	Provides thermal protection for relay to ground path during extended periods of use. The PTC is not provided with HC5513/26EVAL board.
R <sub>F1</sub> , R <sub>F2</sub>	Feed resistors that limit the current into the tip and ring inputs of the HC5513/26 SLIC.
D <sub>1</sub> D <sub>4</sub>	Provide transient protection on the tip and ring inputs.
C <sub>TC</sub> , C <sub>RC</sub>	Provide immunity against high frequency noise on tip and ring respectively.

The Two-Wire Side components are typical telephony values. Design equations are not used for these components.

#### **Ring Trip Detector**

R <sub>1</sub> , R <sub>2</sub>	Generate a bias voltage from $V_{BAT}$ to drive the $R_{D}$ pin.
R <sub>3</sub> , R <sub>4,</sub> R <sub>RT</sub>	Combine to sense off-hook condition and drive the $\ensuremath{R_T}$ pin.
C <sub>RT</sub>	Provides attenuation of the ring signal for stability of $D_T$ pin.

The component values for the Ring Trip detector circuit do not require design equations. For information concerning the functionality of this supervisory function refer to the "Supervisory Function" section of the HC5513/26 data sheet.

#### **Loop Current Detector**

R <sub>D</sub>	Sets the loop current detect threshold for the HC5513/26
	internal comparator function.

The value of  $R_D$  programs the loop current detect threshold for the HC5513/26 SLIC. Since the internal comparator has hysteresis, there are two equations that apply to the value of  $R_D$ . One equation is for on-hook to off-hook threshold and the other is for off-hook to on-hook threshold. The equations for each condition are as follows:

On-Hook to Off-Hook Threshold

$$R_{D} = \frac{465}{I_{(ON-HOOK TO OFF-HOOK)}}$$

Off-Hook to On-Hook Threshold

$$R_{D} = \frac{375}{I_{(OFF-HOOK\ TO\ ON-HOOK)}}$$

For details concerning the design equations refer to the "Supervisory Function" section of the HC5513/26 data sheet. As delivered, the HC5513/26EVAL is configured for a loop current detect level of 11.9mA for on-hook to off-hook and 9.6mA for off-hook to on-hook.

#### **Saturation Guard Resistor**

	Sets the saturation guard for the HC5513/26 SLIC.
_	

When operating in systems with a -28V battery,  $R_{SG}$  needs to be an open circuit. When operating in systems with a -48V battery,  $R_{SG}$  needs to be 21.4k $\Omega$  as per the following equation:

$$R_{SG} = \frac{5 \cdot 10^{5}}{(|V_{BAT}| - V_{MARGIN}) \times \left(1 + \frac{(R_{DC1} + R_{DC2})}{600 \cdot R_{I}}\right) - 16.66V}$$

For details concerning the design equations refer to the "Constant Loop Current (DC) Path" section of the HC5513/26 data sheet. As delivered, the HC5513/26EVAL is configured for a saturation guard of 4V on both the tip side and ring side, resulting in a  $V_{MARGIN}$  of 8V for  $V_{BAT} = -48V$  (on hook  $R_2 = \infty$ .

#### Four-Wire Side, SLIC Impedance Matching

	Sets the synthesized impedance across the tip and ring terminals.
1111	Performs a voltage to current conversion of the receive signal. Selected to maintain unity gain from 4-wire to 2-wire side when SLIC is terminated with $600\Omega_{\cdot}$

The values of  $R_T$  and  $R_{RX}$  have been selected for a  $600\Omega$  system. These values can be modified for different impedances. Also, complex impedance matching is possible using these components. For information on impedance matching of the SLIC, refer to the "(AC) 2-Wire Impedance" section of the HCS513/26 data sheet.

#### **Constant Feed Current Programming**

R <sub>DC2</sub>	Set the constant feed current that flows from tip to ring when a DC path is present during off-hook conditions. Resistance is split to allow capacitor for filtering ( $C_{DC}$ ).
	Filter capacitor to attenuate high frequency noise that is fed back from tip and ring.

The constant feed current is programmed using the sum of  $R_{DC1}$  and  $R_{DC2}$ . The design equation used to set the loop current is shown below.

$$I_{L} = \frac{2.5V}{R_{DC1} + R_{DC2}} \times 1000$$

For details concerning the design equations for loop current as well as the selection of C<sub>DC</sub> refer to the "Constant Loop Current (DC) Path" section of the HC5513/26 data sheet. As delivered, the constant feed current is set at 30mA.

#### **Transhybrid Balance**

R <sub>TX</sub> , R <sub>B</sub>	Used	as	part	of	transhybrid	balance	circuitry	that	is
	locate	d of	ff boa	rd.					

Transhybrid balance is fully discussed in the "Transhybrid Circuit" section of the HC5513/26 data sheet. As delivered, the HC5513/26EVAL does not include these components.

#### HC5513/26 SLIC Operating States Logic Truth Table

The logic truth table for controlling the HC5513/26 SLIC using the HC5513EVAL is provided in Table 2. The SLIC has four operating states. The states are Open Circuit, Active, Ringing and Standby. Each state, except Open Circuit, has options available selecting the supervisory signal that drives the DET pin. The supervisory signals are Ground Key Detect, Loop Current Detect and Ring Trip Detect.

**TABLE 2. LOGIC TRUTH TABLE** 

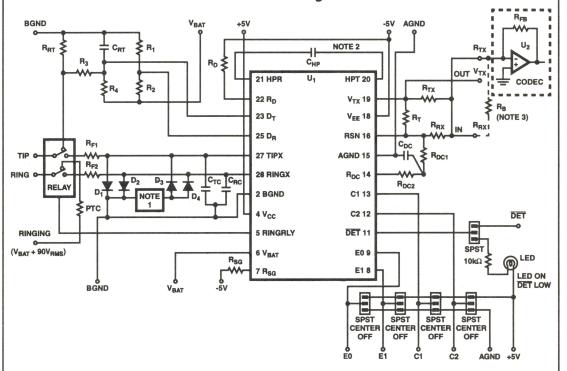
E0	E1	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	DET OUTPUT
0	0	0	0	Open Circuit	No Active Detector	Logic Level High
0	0	0	1	Active	Ground Key Detector	Ground Key Status
0	0	1	0	Ringing	No Active Detector	Logic Level High
0	0	1	1	Standby	Ground Key Detector	Ground Key Status
				T		
0	1	0	0	Open Circuit	No Active Detector	Logic Level High
0	1	0	1	Active	Loop Current Detector	Loop Current Status
0	1	1	0	Ringing	Ring Trip Detector	Ring Trip Status
0	1	1	1	Standby	Loop Current Detector	Loop Current Status
				I	I	T
1	0	0	0	Open Circuit	No Active Detector	]]
1	0	0	1	Active	Ground Key Detector	
1	0	1	0	Ringing	No Active Detector	
1	0	1	1	Standby	Ground Key Detector	]
						Logic Level High
1	1	0	0	Open Circuit	No Active Detector	
1	1	0	1	Active	Loop Current Detector	
1	1	1	0	Ringing	Ring Trip Detector	]
1	1	1	1	Standby	Loop Current Detector	J

#### Application Note 9537

TABLE 3. HC5513/26EVAL EVALUATION BOARD PARTS LIST

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	HC5513/26	N/A	N/A	R <sub>RT</sub>	150Ω	5%	2W
R <sub>F1</sub> , R <sub>F2</sub>	Short	N/A	1/4W	R <sub>SG</sub> , V <sub>BAT</sub> = -48V	21.4kΩ	1%	1/4W
R <sub>1</sub> , R <sub>3</sub>	200kΩ	5%	1/4W	R <sub>DC1</sub> , R <sub>DC2</sub>	41.2kΩ	5%	1/4W
R <sub>2</sub>	910kΩ	5%	1/4W	C <sub>DC</sub>	1.5μF	20%	10V
R <sub>4</sub>	1.2ΜΩ	5%	1/4W	C <sub>HP</sub>	10nF	20%	100V
R <sub>B</sub>	Not Installed Reference data sheet for calculation		C <sub>RT</sub>	0.39μF	20%	100V	
R <sub>D</sub>	39kΩ	5%	1/4W	C <sub>TC</sub> , C <sub>RC</sub>	2200pF	20%	100V
R <sub>FB</sub>	20.0kΩ 1% 1/4W		D <sub>1</sub> - D <sub>4</sub>	Diode with	Given Rating	100V, 3A	
R <sub>RX</sub>	300kΩ	1%	1/4W	D <sub>5</sub>	1N914	N/A	N/A
R <sub>T</sub>	600kΩ	1%	1/4W	PTC	Shorted	N/A	N/A
R <sub>TX</sub> 20kΩ 1% 1/4W		K <sub>R</sub>	2C Conta	acts, 12V Coil	N/A		
R <sub>LED</sub>	500Ω	10%	1/4W	Textool Socket	22	8-5523	N/A

#### HC5513/26EVAL Evaluation Board Schematic Diagram



#### NOTES:

- The anodes of D<sub>3</sub> and D<sub>4</sub> may be connected directly to the V<sub>BAT</sub> supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D<sub>3</sub> and D<sub>4</sub> be shorted to ground through a transzorb or surgector (SGT06U13).
- 2. To meet the specified 25dB 2-wire return loss at 200Hz, CHP needs to be 20nF, 20%, 100V.
- 3.  $R_B$  is required for transhybrid balance when using op amps internal to CODEC.  $R_B = R_{TX}$ .

#### FIGURE 2.

#### HC5513/26EVAL Evaluation Board Layout

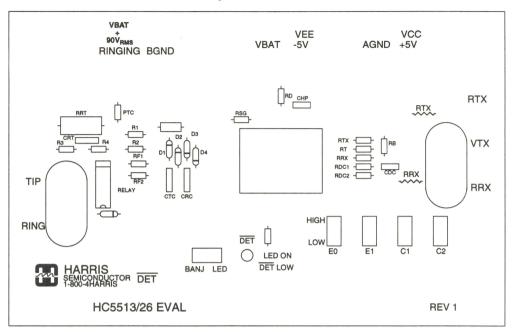


FIGURE 3. SILK SCREEN

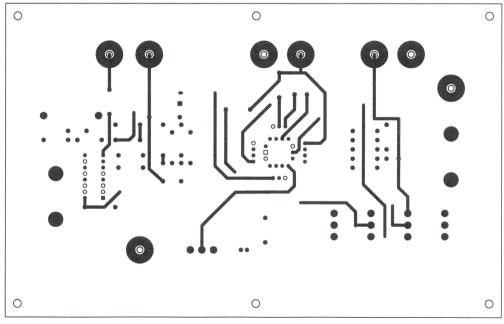


FIGURE 4. TOP SIDE

#### HC5513/26EVAL Evaluation Board Layout (Continued)

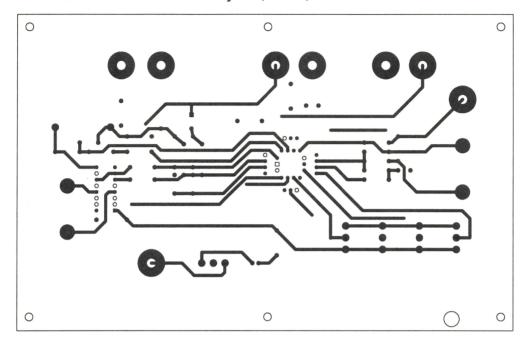


FIGURE 5. BOTTOM SIDE



No. AN9606.4 June 1997

#### Harris Telecom

#### Operation of the HC5517 Evaluation Board (HC5517EVAL)

Authors: Ed Berrios, Don LaFontaine

#### **Features**

- Thru-SLIC Ringing up to 44V<sub>RMS</sub> into 3 REN at 10% THD with a -80V Battery
- Sine Wave Capable for Ring Signal Purity
- Toggle Switch Programming for Logic States
- . Monitoring of SHD, RTD and ALM, via On-Board LEDs
- Includes Transhybrid Circuit for Voice and Pulse Metering
- Externally Controlled Selectable Battery Supply
- Logic Terminal Port for Easy Evaluation in Existing Systems
- Pulse Metering Capability up to 1V<sub>RMS</sub>

#### **Applications**

 Solid State Line Interface Circuit for Wireless Local Loop, Hybrid Fiber Coax, Set Top Box, Voice/Data Modems

#### Functional Description

The HC5517EVAL Subscriber Line Interface Circuit (SLIC) evaluation board has provisions for: Through SLIC balanced ringing up to 3 REN with a 1.2V<sub>RMS</sub> input AC signal, on-hook Maintenance Termination Unit (MTU) voltage between tip and ring with a supply voltage greater than -48V, complete transhybrid balance including pulse metering (Teletax) signals and full evaluation of the voice and DC feeding characteristics of the HC5517 SLIC. Functional control of the SLIC is provided using the toggle switches F1, RC and B1. See Table 7 for the logic states.

#### Power Requirements for the HC5517EVAL

#### **Power Supply Connections**

The HC5517EVAL requires four external power supplies for a complete evaluation of the application. The SLIC is powered by two different battery supply voltages (-24V, -80V) and a +5V supply. The fourth supply (-5V) powers an external op amp (CA741C) for the transhybrid balance circuit. This op amp is usually contained in the CODEC.

#### **Ground Connections**

The HC5517EVAL board has connected the analog and battery grounds to a common ground plane designated GND. It is recommended that the analog and battery grounds of the SLIC be tied together as close to the device pins as possible. The four external power supplies should each be grounded to the evaluation board.

#### HC5517EVAL Board SLIC Controls

The design of the HC5517EVAL board incorporates three SPDT center off switches. Two of the switches (F1, RC) control the functional state of the HC5517 SLIC and the third (B1) switches the battery supply between the talk battery (-24V) and the standby or ringing voltage (-80V). If off-board mode control of the SLIC is desired, the three switches can be set to center open position and driven by logic at the logic terminal port. The logic terminal port is located between the V-TELETAX and the F1 BNCs at the top of the board.

#### **Mode Control Switches**

Toggling F1 and RC towards the part places it in the logic "0" state; and toggling them away from the part places it in the logic "1" state.

A common ground must exist between the HC5517EVAL evaluation board and the off board logic. A differential ground voltage may result in erroneous logic states at the SLIC inputs.

#### Verifying the HC5517EVAL Operation

The operation of the HC5517EVAL and sample part can be verified by performing six tests.

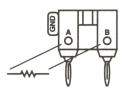
- 1. Battery Switch Verification
- 2. Power Supply Current Verification
- 3. Functional Verification
- 4. SLIC Gain Verification
- 5. Transhybrid Balance Verification
- 6. Through SLIC Ringing Verification

The first five tests require an AC voltmeter. The last test requires and AC signal source, AC voltmeter and up to 3 telephones.

#### **Application Note 9606**

Verify that the sample HC5517 included with the evaluation board is oriented in its socket correctly. Correct orientation is with pin 1 pointing towards the right hand side of the socket.

Application Tip: When terminating tip and ring on the HC55517EVAL it is handy to assemble terminators using a Pomona MDP dual banana plug connector as the terminating resistor receptacle. Refer to Figure 1 for details.



**FIGURE 1. TERMINATION ADAPTER** 

Using the termination shown in Figure 1 provides an unobtrusive technique for terminating tip and ring while still providing access to both signals using the banana jack feature of the MDP connector. Posts are also available that fit into holes A and B, providing a solderable connection for the terminating resistor.

#### **TEST #1 - BATTERY SWITCH VERIFICATION**

This test will verify the battery switch circuit is functioning properly. The BATTERY switch is the SPDT center off toggle switch located in the upper right hand side of the board.

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- 2. Set the mode switches to F1 = 1, RC = 0.
- Set the BATTERY switch (B1) to the -80V position and measure the voltage on ring referenced to ground.
- 4. Set the BATTERY switch (B1) to the -24V position and measure the voltage on ring referenced to ground.

#### Discussion:

The BATTERY switch is used to change the battery voltage between the talk battery of -24V and the standby or ringing voltage of -80V. The BATTERY switch is controlled one of three ways: (1) SPDT toggle switch, (2) external BNC connector (SPDT center off position), or (3) through the logic terminal port (SPDT center off position).

#### Verification:

Compare measured values with those in Table 1.

TABLE 1.

BATTERY SWITCH	-24V	-80V
Ring Voltage (Referenced to Ground)	≈ -19	≈ -48

#### **TEST #2 - POWER SUPPLY CURRENT VERIFICATION**

A quick check of evaluation board and the HC5517 sample is to measure the currents of each supply. The readings should be similar to the values listed in Table 1. The measurements can be made using a series ammeter on each supply, or power supplies with current displays.

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- Set the mode switches for "Active Mode": F1 = 1, RC = 0, B1 = -24V.
- 3. Terminate HC5517 SLIC with a  $600\Omega$  load.
- 4. Measure the supply currents.

#### Discussion:

The currents measured include those of the SLIC and supporting circuitry. For SLIC supply currents consult the HC5517 data sheet.

#### Setup:

- Set the mode switches for "Standby Mode" F1 = 1, RC = 0, B1 = -80V.
- 2. Disconnect the  $600\Omega$  load.
- 3. Measure the -80V supply current.

#### Verification:

Compare measured values with those in Table 2.

TABLE 2.

SUPPLY	R <sub>L</sub> (Ω)	MODE	TYP (mA)		
V <sub>CC</sub> = +5V	600	Active	20 (Note)		
V <sub>EE</sub> = -5V	600	Active	0.2 (Note)		
V <sub>BAT</sub> = -24V	600	Active	20 (Note)		
V <sub>BAT</sub> = -80V	00	Standby	3 ,		

NOTE:  $V_{CC}$  and  $V_{EE}$  supply currents are virtually independent of  $V_{BAT}$  and  $R_{I}$ 

#### **TEST #3 - FUNCTIONAL VERIFICATION**

This test will verify that the HC5517EVAL can successfully: (1) Set the HC5517 into the Ringing Mode, (2) Set the HC5517 into the on-hook Standby Mode, (3) Set the HC5517 into the off-hook Active Mode and (4) Set the HC5517 into the Power Denial Mode.

#### **Ringing Mode:**

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- 2. Set the mode switches for "Ringing Mode" F1 = 1, RC = 1, B1 = -80V
- 3. Verify that R<sub>I</sub> = ∞

#### Discussion:

This test will measure the tip and ring voltages, referenced to ground, to verify the SLIC is in the Ringing state. In this state both tip and ring voltages are approximately  $V_{\rm RAT}/2$ .

#### Verification:

Compare measured values with those in Table 3.

TABLE 3.

V <sub>BAT</sub> (V)	R <sub>L</sub>	TIP TO GND	RING TO GND
	(Ω)	(V)	(V)
-80	00	≈ -40	≈ -40

#### On-Hook Standby Mode:

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- 2. Set the mode switches for "Standby Mode" F1 = 1, RC = 0. B1 = -80V.

#### Discussion:

This test measures the voltage across tip and ring to verify that the SLIC is in the Standby state. In this state the tip to ring voltage is maintained within the MTU range of -42V and -56V.

#### Verification:

Compare measured values with those in Table 4.

TABLE 4.

V <sub>BAT</sub> (V)	R <sub>L</sub> (Ω)	MTU TIP TO RING (V)	
-80	00	≈ 46.0	

#### Off-Hook Active Mode:

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- 2. Set the mode switches for "Active Mode" F1 = 1, RC = 0, R1 = -24V
- Terminate HC5517 SLIC with a 600Ω load.

#### Discussion:

This test measures the voltage across tip and ring to verify that the SLIC is in the off-hook active state.

Note: The loop current can be set to a typical value of 25mA by adjusting the potentiometer ( $R_{28}$  located to the right of the tip and ring connector) and measuring the current from tip to ring with no load.

The loop current is detected at SHD when ever the internally set threshold of 12mA is exceeded.

#### Verification:

Compare measured values with those in Table 5. Verify that the  $\overline{SHD}$  LED is on, and then goes off when the 600 $\Omega$  load is removed.

#### TABLE 5.

V <sub>BAT</sub> (V)	R <sub>L</sub> (Ω)	TIP TO RING (V)	
-24	00	≈ 16.0	

#### Power Denial Mode:

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- 2. Set the mode switches for "Power Denial Mode" F1 = 0, RC = 0 or 1. B1 = -24V or -80V.

#### Discussion:

This test will measure the tip and ring voltages, referenced to ground, to verify the SLIC is in the Power Denial state. The Power Denial state is invoked when the F1 pin goes low (RC is a don't care).

#### Verification:

Compare measured values with those in Table 6.

TABLE 6.

V <sub>BAT</sub>	R <sub>L</sub>	TIP TO GND	RING TO GND
(V)	(Ω)	(V)	(V)
-24 or -80	∞	≈ -5.0	

#### **TEST #4 - SLIC GAIN VERIFICATION**

This test will verify that HC5517 SLIC is operating properly and that the SLIC is exhibiting unity gain. Unity gain will only exist if the SLIC is properly terminated with a  $600\Omega$  load.

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- Set the mode switches for "Active Mode" F1 = 1, RC = 0, B1 = -24V.
- 3. Terminate HC5517 SLIC with a  $600\Omega$  load.
- 4. Connect a sine wave generator to the V-REC input.
- 5. Set the generator for  $0.775V_{RMS}$  and 1kHz.
- 6. Connect an AC voltmeter across tip and ring.

#### Discussion:

When terminated with 600 $\Omega$ , the SLIC will exhibit unity gain from the V-REC input pin to across tip and ring. The unity gain results from the matched impedance that the 600 $\Omega$  termination represents to the internally synthesized 600 $\Omega$  of the SLIC. When an open circuit exists, a mismatch occurs and the gain of the SLIC doubles.

#### Verification:

- 1. Tip to ring AC voltage of  $0.775V_{\mbox{RMS}}$  when terminated.
- 2. Tip to ring AC voltage of 1.55V<sub>RMS</sub> when not terminated.

#### TEST #5 - TRANSHYBRID BALANCE VERIFICATION

This test will verify the transhybrid balance circuitry for both the voice path and the pulse metering (TELETAX) path. A low distortion AC signal source and a volt meter are the only additional hardware required to complete this test.

#### VOICE PATH:

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- 2. Set the mode switches for "Active Mode" F1 = 1, RC = 0, B1 = -24V.
- 3. Terminate HC5517 SLIC with a  $600\Omega$  load.
- Set the AC source to 1V<sub>RMS</sub>, 1kHz and apply to the V-REC input.
- 5. Connect an AC voltmeter between the V-XMIT and GND.

#### Discussion:

Transhybrid balance is a measure of how well the input signal is canceled (that being received by the SLIC) from the transmit signal (that being transmitted from the SLIC). Without this function, voice communication would be difficult because of the echo.

#### Verification:

- 1. Measure the AC voltage at V-XMIT output.
- 2. Calculate the Transhybrid balance using Equation 1.

Transhybrid = 
$$20 \times log \frac{V - XMIT}{1V_{RMS}}$$
 (EQ 1.)

3. The value should be around -40dB.

#### **PULSE METERING Option**

NOTE: Resistors  $R_6$  and  $R_7$  must be installed for this option. See Table 8 for  $R_6$  and  $R_7$  values to allow up to a 1V  $_{RMS}$  Pulse Metering Signal.

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- 2. Set the mode switches for "Active Mode" F1 = 1, RC = 0, B1 = -24V.
- 3. Terminate HC5517 SLIC with a 600Ω load.
- Set the AC source to 1V<sub>RMS</sub>, 12kHz or 16kHz and apply to the V-TELETAX input BNC.
- 5. Connect an AC voltmeter between the V-XMIT and GND.

#### Discussion:

The pulse metering signal is a 12kHz or 16kHz signal that is injected on to the tip and ring lines. This signal is monitored by a counter (non-U.S. markets) inside the pay phone, which tallies up the cost of the call. Because it travels on the tip and ring lines simultaneously with the speech, the amplitude of this signal must be accounted for in the tip and ring overhead voltage. To account for this, resistors  $R_6$  and  $R_7$  can be added to allow the pulse metering signal.

#### Verification:

- 1. Measure the AC voltage at V-XMIT output.
- 2. Calculate the Transhybrid balance using Equation 1.
- 3. The value should be around -25dB.

#### **TEST #6 - THROUGH SLIC RINGING VERIFICATION**

This test will verify the through SLIC ringing function of the HC5517EVAL by ringing the phone(s) and monitoring the Ring Trip Detect ( $\overline{RTD}$ ) and the  $\overline{SHD}$  LEDs. A telephone (or equivalent resistance of  $8k\Omega$  in parallel with a  $10\mu F$  capacitor per phone) and a 20Hz AC signal source are the only additional hardware required to complete the test.

#### Setup:

- 1. Connect the power supplies to the HC5517EVAL.
- 2. Set the mode switches for "Ringing Mode" F1 = 1, RC = 1, B1 = -80V.
- Connect up to 3 telephones (or equivalent resistance) across tip and ring.
- 4. Connect a 20Hz 1.2V<sub>RMS</sub> AC source to V<sub>RING</sub>.
- 5. Connect an AC voltmeter across tip and ring.

#### Discussion:

The gain of the  $V_{RING}$  input is internally set to provide a total voltage gain of 40 across tip and ring. Tip and ring are internally set to be 4V from GND and 4V from  $V_{BAT}$  respectively (plus any offset for teletax signals). This results in a maximum tip to ring of (80V-8V) 72V. With a gain of 40 through the  $V_{RING}$  input the maximum input signal without clipping is therefore 1.2 $V_{RMS}$  (1.2x1.414x40 = 67.8 $V_{PEAK}$  or 47.95 $V_{RMS}$ ).

The Ring Trip is detected at  $\overline{\text{RTD}}$  when going from on-hook to off-hook with the ringing signal applied. The low off-hook impedance causes a high AC current that exceeds both the  $\overline{\text{SHD}}$  threshold (12mA) and the externally set  $\overline{\text{RTD}}$  threshold (30mA).

#### Verification:

- 1. Apply power to the SLIC.
- Verify that both the tip and ring voltages are approximately V<sub>BAT</sub>/2. This allows the maximum voltage swing of the AC signal for ringing the phone(s).
- Apply the AC source to the input labeled V<sub>RING</sub>. The phone(s) will start to ring.
- Verify that while ringing the phone(s) the RTD light is out and the SHD light is flashing at 20Hz.
- Verify that the tip-to-ring AC voltage is approximately 48V<sub>RMS</sub>.
- 6. Verify that while ringing the phone(s) and going off-hook both the SHD and RTD LEDs illuminate.

# Functional Circuit Component Descriptions

The HC5517EVAL design incorporates all of the external components necessary for ringing the phone through the SLIC. A brief description of each component is provided below. The components will be grouped by function to provide further insight into the operation of the HC5517EVAL board.

#### TWO-WIRE SIDE, TIP AND RING

R <sub>11-14</sub>	Feed resistors that limit the current into the tip and ring inputs and are used for loop current detection.
D <sub>1-4</sub> C <sub>9</sub>	Provides surge protection for tip and ring by directing large voltage transients to either GND or $V_{\text{BAT}}$ .

The Two-Wire Side components are typical telephony values. Design equations are not used for these components.

#### **BATTERY SWITCH CIRCUIT**

R <sub>21</sub> , R <sub>22</sub> D <sub>7-10</sub>	The BATTERY switch circuit selects one of two supply voltages by either a logic input from and
T <sub>1</sub> , T <sub>3</sub> SPDT switch	external source or an on board SPDT toggle switch.

#### TRANSHYBRID CIRCUIT

R <sub>1-5</sub> U1	Transhybrid balance circuit cancels the input
U1	signal (that being received by the SLIC) from the
	transmit signal (that being transmitted from the SLIC).

#### MTU CIRCUIT

R <sub>19</sub> , R <sub>24</sub> D <sub>11</sub>	The MTU circuits clamps the voltage across tip and ring within the range of -42V and -56V.
C <sub>16</sub> T <sub>2</sub> SPDT Switch (RC)	

#### RTD FILTER

R <sub>15-17</sub>	Filters out the AC to avoid false ring trip detection
D <sub>5</sub>	when ringing the phone.
C <sub>10</sub>	

#### RING CENTERING CIRCUIT

R <sub>18,</sub> R <sub>19</sub> D <sub>6,</sub> D <sub>13</sub> C <sub>11</sub>	The Ring Centering circuit offsets the tip and ring voltages to $V_{BAT}/2$ when the SLIC is configured for ringing (F1 = 1, RC = 1).
--	---

#### **AC DECOUPLING CAPACITORS**

C <sub>5-8</sub>	AC decoupling capacitors
------------------	--------------------------

#### **PULSE METERING**

R <sub>6</sub> , R <sub>7</sub> Optional, not supplied with board  The pulse metering circuit provides and offset voltage on tip and ring to accommodate a pulse metering signal.
---

#### **CURRENT LIMIT**

R <sub>10</sub> , R <sub>28</sub>	Sets the loop current limit.					
	ILIMIT = $0.6 \cdot \frac{R_{10} + R_{28}}{200 \cdot R_{28}}$					
	R <sub>28</sub> is a potentiometer					

#### **GAIN RESISTORS**

R <sub>8,</sub> R <sub>9</sub>	Sets	the	gain	of	the	internal	ор	amp	for
-, -	imped	dance	matc	hing	and	transhyb	rid b	alance	. ,

#### SUPPLY DECOUPLING CAPACITORS

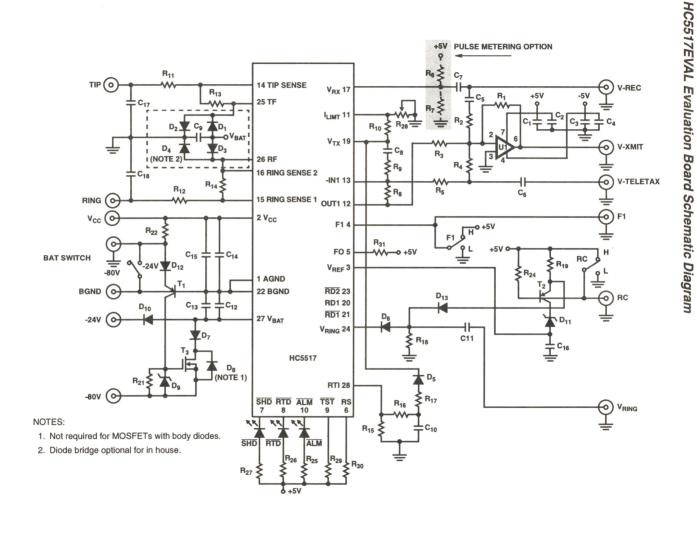
C <sub>1-4</sub> C <sub>12-15</sub>	Supply decoupling capacitors.
-12-13	

#### SHD, RTD, ALM LEDS

	Current limiting resistors for the $\overline{\rm SHD},  \overline{\rm RTD}$ and $\overline{\rm ALM}$ LEDs
--	--

#### **PULL UP RESISTORS**

#### SPDT TOGGLE SWITCH



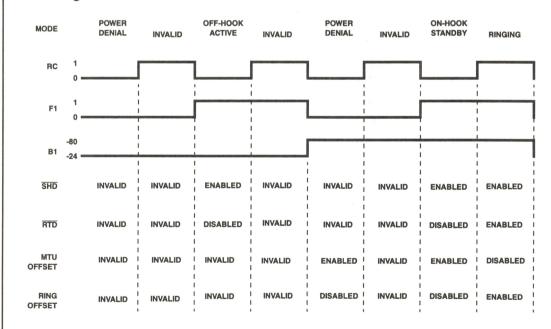
# HC5517 SLIC Operating Modes for Application Schematic

TABLE 7. LOGIC STATES

BATTERY				DETEC (VA		APPLICATIO (VA	
SWITCH B1	F1	RC	MODE	SHD	RTD	MTU VOLTAGE	TIP TO RING CENTERING
-24V	0	0	Power Denial				
-24V	0	1	Invalid				
-24V	1	0	Off-Hook Active	1			
-24V	1	1	Invalid	-177			
-80V	0	0	Power Denial			1	
-80V	0	1	Invalid				
-80V	1	0	On-Hook Standby	1		1	
-80V	1	1	Ringing	(Note)	1		<b>/</b>

NOTE: During Ringing, the SHD output will be active for both on-hook and off-hook conditions. The AC current, for the on-hook condition, exceeds the SHD threshold of 12mA. Valid off-hook detection during ringing is provided by the RTD output only.

# Mode Diagram



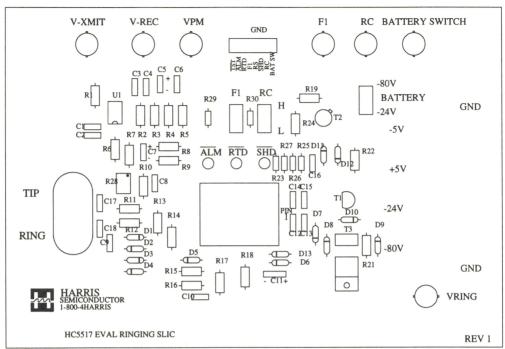
# HC5517EVAL Evaluation Board Parts List

## TABLE 8. EVALUATION BOARD PARTS LIST

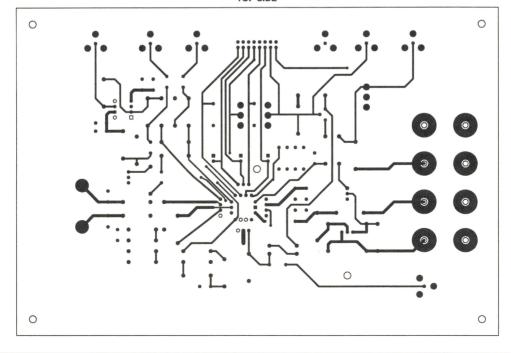
COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
SLIC	HC5517	N/A	N/A	C <sub>2,</sub> C <sub>4,</sub> C <sub>15</sub>	0.1μF	20%	50V
R <sub>1</sub> , R <sub>2</sub>	24.9kΩ	1%	1/4W	C <sub>5,</sub> C <sub>7</sub>	10μF	20%	20V
R <sub>3</sub>	8.25kΩ	1%	1/4W	C <sub>6,</sub> C <sub>8</sub>	0.47μF	20%	20V
R <sub>4</sub>	12.1kΩ	1%	1/4W	C <sub>9</sub> , C <sub>12</sub>	0.01μF	20%	100V
R <sub>5,</sub> R <sub>8,</sub> R <sub>9</sub>	40kΩ	1%	1/4W	C <sub>10</sub>	1.0μF	20%	50V
R <sub>6</sub> (not provided)	23.2kΩ	1%	1/4W	C <sub>11</sub>	100μF	20%	5V
R <sub>7</sub> (not provided)	10kΩ	1%	1/4W	C <sub>13</sub>	0.1μF	20%	100V
R <sub>10</sub>	100kΩ	5%	1/4W	C <sub>16</sub>	0.5μF	20%	50V
R <sub>11-14</sub>	50Ω	1%	1/4W	C <sub>17,</sub> C <sub>18</sub>	3300pF	20%	100V
R <sub>15</sub>	47kΩ	1%	1/4W	D <sub>1-4</sub> , D <sub>7</sub> , D <sub>8</sub> , D <sub>10</sub>	1N4007		100V, 1A
R <sub>16</sub>	1.5ΜΩ	1%	1/4W	D <sub>5</sub> , D <sub>6</sub> , D <sub>12</sub> , D <sub>13</sub>	1N914		100V, 1A
R <sub>17</sub>	56.2kΩ	1%	1/4W	D <sub>9</sub>	1N4744		15V, 1W
R <sub>18</sub>	1.1kΩ	1%	1/4W	D <sub>11</sub>	1N5255		28V, 1/2W
R <sub>19</sub>	825Ω	1%	1/4W	T <sub>1</sub>	NTE 383		100V, 1A
R <sub>20</sub> , R <sub>22</sub> , R <sub>29</sub> , R <sub>30</sub> , R <sub>31</sub>	10kΩ	5%	1/4W	T <sub>2</sub>	2N2907		60V, 150mA
R <sub>24</sub>	47kΩ	5%	1/4W	Т <sub>3</sub>	RFP2N10 or equivalent		100V, 2A
R <sub>25-27</sub>	560Ω	5%	1/4W	F1, RC, Battery	SPDT Toggle S	Switches, center of	off.
R <sub>28</sub>	20kΩ Poten	tiometer	1/4W	U1	CA741C Op An	np	
R <sub>21</sub>	47kΩ	5%	1/4W	Textool Socket	228-5523		
C <sub>1,</sub> C <sub>3,</sub> C <sub>14</sub>	0.01μF	20%	50V				

# HC5517EVAL Evaluation Board Layout

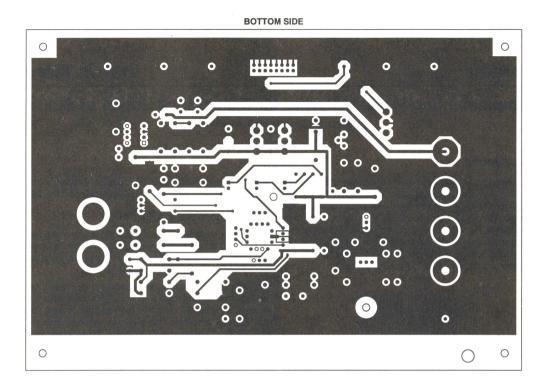
SILK SCREEN



TOP SIDE



# HC5517EVAL Evaluation Board Layout



**No. AN9608** July 1996

# Harris Telecom

# Implementing Pulse Metering for the HC5509 Series of SLICs

Authors: Ed Berrios and Don LaFontaine

#### Introduction

Pulse metering or Teletax is used outside the United States for billing purposes at pay phones. A 12kHz or 16kHz burst (see Figure 1) is injected into the 4-wire side of the SLIC and transmitted across the tip and ring lines from the central office to the pay phone. The burst updates a counter that indicates the cost of the call to the user. The repetition rate of the burst is dependent upon the billing rates for the specific time of the day and the distance of the call.

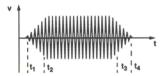


FIGURE 1. PULSE METERING SIGNAL ENVELOPE

The waveform in Figure 1 represents the pulse metering signal burst. The rise and fall times of the waveform are specified to minimize emissions of the burst. Table 1 lists the electrical specifications of the waveform.

**TABLE 1. PULSE METERING ELECTRICAL PARAMETERS** 

PARAMETER	VALUE	NOTE	LIMITS
Frequency	12kHz or 16kHz	Selectable	±50Hz
Level	1V <sub>RMS</sub>	200Ω load	±10%
2 <sup>nd</sup> , 3 <sup>rd</sup> Harmonics	<200mV	200Ω load	-
2-Wire Impedance	200Ω	12kHz or 16kHz	±40Ω
Rise (t <sub>r</sub> ) and fall (t <sub>f</sub> ) times	10ms or 20ms	$t_r = t_2 - t_1$ $t_f = t_4 - t_3$	±10%

This Application Note discusses the technique for injecting a pulse metering signal into the 4-wire side of the SLIC for transmission on the 2-wire side. The complete implementation includes a circuit for injecting the AC pulse metering signal, a circuit for offsetting the tip and ring DC voltages and a circuit for the transhybrid balance of the pulse metering return signal. The tip and ring DC voltages must be offset by the peak value of the pulse metering signal to allow simultaneous transmission of voice and pulse metering. A brief discussion of impedance matching will lead into the detailed pulse metering discussion. For a detailed discussion, refer to

AN9607, "Impedance Matching Design Evaluation for the HC5509 Series of SLIC", AnswerFAX Document No. 99607.

## SLIC Impedance Matching

Impedance matching is used to set the 4-wire to 2-wire gain of the SLIC for a specified termination impedance across tip and ring. The termination may vary from purely resistive (typ  $600\Omega$ ) to complex (resistive plus capacitive).

The impedance matching is synthesized by feeding back a voltage that is proportional to the 2-wire loop current. This voltage is then scaled and injected into the summing node of the tip feed amplifier. The feedback compensates for the voltage drop across the tip and ring sense resistors (R<sub>S</sub>), which results in the impedance of the SLIC matching the load (R<sub>L</sub>).

Figure 2 shows the network used to derive the impedance matching equations. The loop equation from tip to ring is written as follows:

$$V_C + 2R_S \Delta I_L - \Delta V_{IN} + R_L \Delta I_L + 2R_S \Delta I_L - V_D = 0$$
 (EQ. 1)

where

$$V_{C} = -V_{D} = -2R_{S}\Delta I_{L} \left(1 - \frac{Z_{O}}{R_{F}}\right)$$
 (EQ. 2)

Solving for  $\Delta V_{IN}/\Delta I_I$  results in Equation 3.

$$\frac{\Delta V_{IN}}{\Delta I_L} = 4R_S \left(\frac{Z_O}{R_F}\right) + R_L \tag{EQ. 3}$$

By setting R<sub>F</sub> equal to 4R<sub>S</sub> then:

$$R_{L} = Z_{O} (EQ. 4)$$

Therefore, to match the impedance of the SLIC, with  $R_S$  equal to  $50\Omega$  to a  $600\Omega$  load:

$$R_F = 4R_S = 4(50\Omega) = 200\Omega$$
 (EQ. 5)

and

$$R_{L} = Z_{O} = 600\Omega \tag{EQ. 6}$$

To prevent loading of the  $V_{TX}$  output, the value of  $R_F$  and  $Z_O$  are typically scaled up by a factor of 100:

$$KR_F = 20k\Omega$$
  $KZ_O = 60k\Omega$  (EQ. 7)

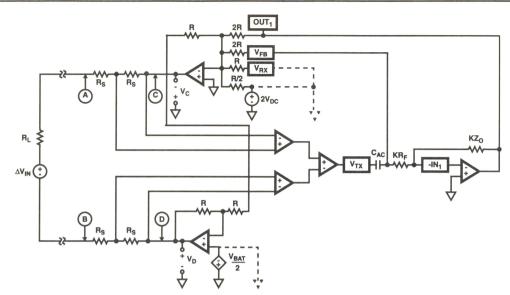


FIGURE 2. FEEDBACK NETWORK FOR IMPEDANCE MATCHING

# Injecting The Pulse Metering Signal

Two circuits must be designed for injection of the pulse metering signal. One circuit is used to sum the pulse metering signal and the incoming voice signal on the 4-wire side and the other is used to offset both tip and ring by the peak amplitude of the pulse metering signal.

#### **Summing Amplifier Design**

The pulse metering signal is injected in the  $-IN_1$  pin of the SLIC. This pin is the inverting input of the internal amplifier (A1) that is used to implement impedance matching.

The components required for pulse metering are  $C_{PM}$  and  $R_{PM}$ , are shown in Figure 3. The pulse metering signal is AC coupled to prevent a DC offset on the input of the internal amplifier. The value of  $C_{PM}$  should be  $10\mu F$ . The value of  $R_{PM}$  is calculated from Equations 9 and 10.

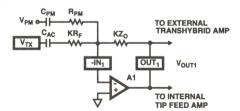


FIGURE 3. PULSE METERING SUMMING AMPLIFIER DESIGN

$$V_{OUT1} = -V_{TX} \circ \frac{KZ_O}{K_{RF}} - V_{PM} \circ \frac{KZ_O}{R_{PM}}$$
 (EQ. 8)

The first term of Equation 8 is the gain of the feedback voltage from the 2-wire side and the second term is the gain of the injected pulse metering signal. The effects of  $C_{AC}$  and  $C_{PM}$  are negligible and therefore omitted from the analysis.

The injected pulse metering output term of Figure 3 is shown below in Equation 9 and rearranged to solve for R<sub>PM</sub> in Equation 10.

$$V_{OUT1}(injected) = V_{PM} \circ \frac{KZ_O}{R_{PM}} = 2$$
 (EQ. 9)

$$R_{PM} = \frac{KZ_0}{2} \tag{EQ. 10}$$

The ratio of  $KZ_O$  to  $R_{PM}$  is set to 2 to compensate for the gain of 0.5 at the tip feed amplifier. This results in unity gain of the pulse metering signal from 4-wire side to 2-wire side. The value of  $KZ_O$  is considered to be a constant since it is selected based on impedance matching requirements.

When complex impedance matching is implemented, match the  $R_{PM}$  circuit to the  $KZ_{O}$  circuit, keeping in mind the required gain of 2.

#### Additional Tip and Ring Offset Voltage

A DC offset is required to level shift tip and ring from ground and  $V_{BAT}$  respectively. By design, the tip amplifier is offset 4V below ground and the ring amplifier is offset 4V above  $V_{BAT}$ . The 4V offset was designed so that the peak voice signal could pass through the SLIC without distortion. Therefore, to maintain distortion free transmission of pulse metering and voice, an additional offset equal to the peak of the pulse metering signal is required.

The tip and ring voltages are offset by a voltage divider network on the  $V_{RX}$  pin. The  $V_{RX}$  pin is a unity gain input designed as the 4-wire side voice input for the SLIC. Figure 4 details the circuit used to generate the additional offset voltage.

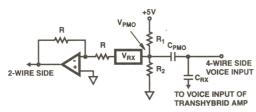


FIGURE 4. PULSE METERING OFFSET GENERATION

The amplifier shown is the tip amplifier. Other signals are connected to the summing node of the amplifier but only those components used for the offset generation are shown. The offset generated at the output of the tip amplifier is summed at the ring amplifier inverting input to provide a positive offset from the battery voltage. The connection to the ring amplifier was omitted from Figure 4 for clarity, refer to Figure 2 for details. The typical component values for Figure 4 are listed in Table 2.

TABLE 2. TYPICAL COMPONENT VALUES FOR FIGURE 4

REF DES	VALUE	REF DES	VALUE
C <sub>RX</sub>	10μF	R	108kΩ
C <sub>PMO</sub> 10μF		R <sub>1</sub>	23.2kΩ
		R <sub>2</sub>	10kΩ

The term V<sub>PMO</sub> is defined to be the offset required for the pulse metering signal. The value of the offset voltage is calculated as the peak value of the pulse metering signal. Equation 11 assumes the amplitude of the pulse metering signal is expressed as an rms voltage.

$$V_{PMO} = \sqrt{2} \cdot V_{PM} \tag{EQ. 11}$$

The value of R<sub>1</sub> can be calculated from the following equation:

$$R_{1} = \left(\frac{R_{2}R}{R_{2} + R}\right) \left(\frac{5 - V_{PMO}}{V_{PMO}}\right)$$
 (EQ. 12)

The component labeled R is the internal summing resistor of the tip amplifier and has a typical value of  $108 k\Omega$ . The value of  $R_2$  should be selected in the range of  $4.99 k\Omega$  and  $10 k\Omega$ . Staying within these limits will minimize the parallel loading effects of the internal resistor R on  $R_2$  as well as minimize the constant power dissipation introduced by the divider.

Solving equation 11 for  $1V_{RMS}$  results in a 1.414V requirement for  $V_{PMO}.$  Setting  $R_2$  of Equation 12 to  $10k\Omega$  and substituting the values for  $V_{PMO}$  and R yields 23.2k $\Omega$  for  $R_1.$  The value of  $R_1$  can be rounded to the nearest standard value without significantly changing the offset voltage.

#### **Voice Path Considerations**

The presence of the offset circuitry in the voice path alters the input impedance seen by the voice signal. The input impedance for the standard application is equal to the value of R ( $108k\Omega$ ) in Figure 4. The additional offset circuitry lowers the impedance to approximately  $5k\Omega$  which maintains a relatively high impedance for the voice driver.

The configuration used also results in a high pass RC network as shown in Figure 5.

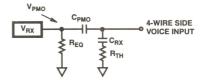


FIGURE 5. HIGH PASS NETWORK FORMED AT VRX NODE

The impact of the resultant high pass network is negligible in the voice band, 200Hz to 3400Hz. The value of the input impedance varies slightly over the voice band,  $5.3k\Omega$  at 200Hz versus  $5.2k\Omega$  at 3400Hz. Replacing both capacitors with a short circuit ( $f = \infty$ ), the steady state value obtained is  $5.19k\Omega$ . The relatively constant input impedance implies the high pass corner frequency is well below the band of interest.

#### **Loop Length Considerations**

The additional offset required for pulse metering reduces the maximum loop resistance driven by the SLIC. For a loop current ( $I_L$ ) of 25mA and battery voltage of -48V, the maximum loop resistance is equal to:

$$R_{L_{\mbox{\scriptsize MAX}}} = \frac{V_{\mbox{\scriptsize TR}}}{I_{\mbox{\scriptsize I}}} = \frac{(-4 + 48)}{0.025} = 1.6 \mbox{k}\Omega \eqno(EQ.~13)$$

For a pulse metering level (V<sub>PM</sub>) of 1V<sub>RMS</sub> and the same conditions as above the maximum loop resistance is:

$$R_{L_{MAX}} = \frac{V_{TR} - 2V_{PMO}}{I_{L}} = \frac{(-4 + 48 - 2(1.414))}{0.025} = 1.48k\Omega$$
 (EQ. 14)

The loop resistance terms in Equations 13 and 14 include the  $200\Omega$  contribution of the SLIC's sense resistors. Therefore, actual loop resistance is  $200\Omega$  less than the calculated values in the above example.

# Cancellation of the Pulse Metering Signal

There are many techniques available for cancelling the return pulse metering signal. The techniques range from filtering of the return signal to transhybrid cancellation. The selected approach varies from application to application and is dependent on the impedance characteristics of the line. The discussion to follow will address the transhybrid technique of cancellation shown in Figure 6.

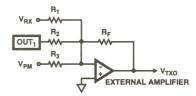


FIGURE 6. CANCELLATION OF THE PULSE METERING SIGNAL

The transhybrid cancellation technique that is used for the voice signal is also implemented for pulse metering. The technique is to drive the transhybrid amplifier with the signal that is injected on the 4-wire side, then adjust its level to match the amplitude of the feedback signal, and cancel the signals at the summing node of an amplifier.

NOTE: The external operational amplifier is used in the application as a "stand in" for the operational amplifier that is traditionally located in the CODEC, where transhybrid cancellation is performed.

Referring to Figure 2,  $V_{TX}$  is the feedback signal used to drive the internal amplifier (A1) that drives the  $OUT_1$  pin of the SLIC. The voltage measured at  $V_{TX}$  is related to the loop impedance as follows:

$$V_{TX} = \frac{-200}{P_1} \bullet V_{PM} \bullet G_{PM}$$
 (EQ. 15)

For a  $600\Omega$  termination and a pulse metering gain  $(G_{PM})$  of 1, the feedback voltage  $(V_{TX})$  is equal to one third the pulse metering signal on the 4-wire side. Note, depending upon the line impedance characteristics and the degree of impedance matching, the pulse metering gain may differ from the voice gain. The pulse metering gain  $(G_{PM})$  must be accounted for in the transhybrid balance circuit.

The following equation is used to calculate the output voltage of the internal amplifier (A1) at OUT<sub>1</sub>:

$$OUT_{1} = -\left(\frac{K_{ZO}}{KR_{F}}\right) \circ V_{TX} + \left(-\frac{K_{ZO}}{R_{PM}}\right) \circ V_{PM}$$
 (EQ. 16)

The first term of the equation is the gain of the feedback signal through the internal amplifier. The second term is the gain of the injected pulse metering signal discussed in the Summing Amplifier Design section of this Application Note. The polarity of the signal at OUT<sub>1</sub> is opposite of V<sub>PM</sub> allowing the circuit of Figure 6 to perform the final stage of transhybrid cancellation.

The following equations do not require much discussion. They are based on inverting amplifier design theory. The voice path V<sub>RX</sub> signal has been omitted for clarity. All reference designators refer to components of Figures 3 and 6.

$$V_{TXO} = -KZ_O * \left( -\frac{V_{TX}}{KR_F} - \frac{V_{PM}}{R_{PM}} \right) * \frac{R_F}{R_2} - \left( V_{PM} * \frac{R_F}{R_3} \right)$$
 (EQ. 17)

The first term refers to the signal at  $OUT_1$  and the second term refers to the 4-wire side pulse metering signal used to complete the transhybrid cancellation. Since ideal transhybrid cancellation implies  $V_{TXO}$  equals zero when a signal is injected on the 4-wire side,  $V_{TXO}$  is set to zero and the resulting equation is shown below.

$$0 = KZ_O \bullet \left(\frac{V_{TX}}{KR_F} + \frac{V_{PM}}{R_{PM}}\right) \bullet \frac{R_F}{R_2} - \left(V_{PM} \bullet \frac{R_F}{R_3}\right)$$
 (EQ. 18)

Rearranging terms of Equation 18 and solving for  $R_3$  results in Equation 19. This is the only value to be calculated for the transhybrid cancellation. All other values either exist in the application circuit or have been calculated in previous sections of this Application Note.

$$R_{3} = \left(\frac{KZ_{O}}{R_{2}} \circ \left(\frac{-200 \circ G_{PM}}{R_{L} \circ KR_{F}} + \frac{1}{R_{PM}}\right)\right)^{-1}$$
 (EQ. 19)

The value of  $R_3$  (Figure 6) is  $8.25k\Omega$  given the following set of values:

$$KZ_{O}=60k\Omega$$
,  $KR_{F}=20k\Omega$ ,  $R_{L}=600\Omega$ ,  $R_{2}=8.25k\Omega$ ,  $R_{PM}=30k\Omega$ ,  $G_{PM}=1$ 

Substituting the same values into Equations 15 and 16, it can be shown that the signal at  $OUT_1$  is equal to  $-V_{PM}$ . This result, along with Equation 18 where  $R_2$  equals to  $R_3$ , indicates the signal levels into the transhybrid amplifier are equal in magnitude but opposite in phase, thereby achieving transhybrid balance at  $V_{TXC}$ .

#### No. AN9628.1 June 1997

# Harris Telecom

# AC Voltage Gain for the HC5509 Series of SLICs

Authors: Don LaFontaine Ed Berrios

### Introduction

The HC5509 Series of SLICs use feedback to synthesize the impedance at the 2-wire tip and ring terminals. This feed back network determines the AC voltage gains for the SLIC.

This application note will discuss the basic AC operation of SLIC. The DC operation and the requirements for impedance matching are discussed in application note AN9607 "Impedance Matching Design Equations for the HC5509 Series of SLICs" and is recommended reading as accompaniment to this application note.

The analysis will use the HC5509B as the basis for the discussion. The same analysis is applicable to the HC5509A1R3060, HC5524 and the HC5517.

## AC Voltage Gain Design Equations

The 4-wire to 2-wire voltage gain (VRX to VR) is set by the feedback loop shown in Figure 1. The First Feedback Loop senses the loop current through resistors R<sub>13</sub> and R<sub>14</sub>, sums their voltage drop and gains it up by 2 to produce an output voltage at the V<sub>TX</sub> pin equal to +4R<sub>S</sub>∆IL. This voltage is then fed back into the tip current summing node via the VFB pin. The current into VFB is equal to:

$$I_{VFB} = \frac{4R_S \Delta I_L}{2R}$$
 (EQ. 1)

The V<sub>TX</sub> voltage is also fed into the -IN input of the SLIC's internal op-amp (Feedback). This signal is gained up by KZ<sub>0</sub>/ KRF then fed into the tip current summing node via the OUT1 pin. (Note: the V<sub>RX</sub> pin and the internal +2V reference are grounded for the AC analysis.) The current into the OUT1 pin is equal to:

$$I_{OUT1} = -\frac{4R_S\Delta I_L}{2R} \left( \frac{Z_0}{R_F} \right)$$
 (EQ. 2)

Equation 3 is the node equation for the tip amplifier summing node. The current in the tip feedback resistor (IR) is given in

$$-I_{R} + \frac{4R_{S}\Delta I_{L}}{2R} - \frac{4R_{S}\Delta I_{L}}{2R} \left(\frac{Z_{0}}{R_{F}}\right) + \frac{V_{RX}}{R} = 0 \tag{EQ. 3}$$

$$I_{R} = \frac{4R_{S}\Delta I_{L}}{2R} - \frac{4R_{S}\Delta I_{L}}{2R} \left(\frac{Z_{0}}{R_{F}}\right) + \frac{V_{RX}}{R}$$

The voltage V<sub>C</sub> is then equal to:

$$V_{C} = (I_{R})(R) \tag{EQ. 5}$$

$$V_{C} = 2R_{S}\Delta I_{L} \left(1 - \frac{Z_{0}}{R_{F}}\right) + V_{RX}$$
 (EQ. 6)

and the AC voltage at VD is:

$$V_{D} = -2R_{S}\Delta I_{L}\left(1 - \frac{Z_{0}}{R_{F}}\right) + V_{RX}$$
 (EQ. 7)

NOTE: V<sub>BAT</sub>/2 is grounded for AC analysis.

The values for Z<sub>0</sub> and R<sub>F</sub> are selected to match the impedance requirements on tip and ring, for more information reference AN9607. The following loop current calculations will assume the proper  $Z_0$  and  $R_F$  values for matching a  $600\Omega$ load (reference Table 1).

TABLE 1. FEEDBACK RESISTORS FOR MATCHING A 600Ω

PART	R <sub>F</sub>	Z <sub>0</sub>
HC5509B	20kΩ	60kΩ
HC5509A1R3060	20kΩ	30kΩ
HC5524	20kΩ	50kΩ
HC5517	40kΩ	40kΩ

The loop current (AI, Figure 1) with respect to the feedback network, is calculated in equations 8 through 11. Where  $Z_0 =$  $60k\Omega$ ,  $R_F = 20k\Omega$ ,  $R_L = 600\Omega$ ,  $R_{11} = R_{12} = R_{13} = R_{14} = 50\Omega$ .

$$\Delta I_L = \frac{V_C - V_D}{R_L + R_{11} + R_{12} + R_{13} + R_{14}} \tag{EQ. 8} \label{eq:deltaI}$$

$$\Delta I_{L} = \frac{2 \times \left(2 R_{S} \Delta I_{L} \left(1 - \frac{Z_{0}}{R_{F}}\right) + V_{RX}\right)}{R_{L} + R_{11} + R_{12} + R_{13} + R_{14}} \tag{EQ. 9}$$

(EQ. 3) 
$$\Delta I_L = \frac{2V_{RX} - 400\Delta I_L}{800}$$
 (EQ. 10)

(EQ. 4) 
$$\Delta I_L = \frac{V_{RX}}{600}$$
 (EQ. 11)

Equation 11 is the loop current with respect to the feedback network. From this, the 4-wire to 2-wire and the 2-wire to 4-wire AC voltage gains can be calculated. Equation 12 shows the 4-wire to 2-wire AC voltage gain is equal to one. Equation 13 shows the 2-wire to 4-wire AC voltage gain is also equal to one.

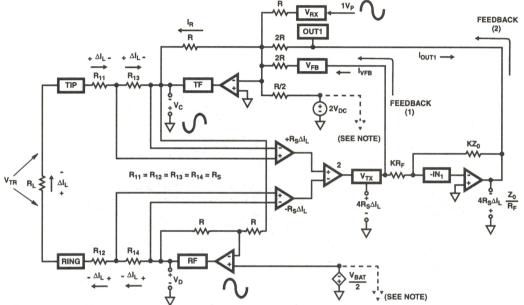
$$A_{4w-2w} = \frac{V_{TR}}{V_{RX}} = \frac{\Delta I_L(R_L)}{V_{RX}} = \frac{\frac{V_{RX}}{600}(600)}{V_{RX}} = 1$$
 (EQ. 12)

$$A_{2w-4w} = \frac{V_{OUT1}}{V_{TR}} = \frac{4R_S \Delta I_L \left(\frac{Z_0}{R_F}\right)}{\Delta I_L (R_L)} = \frac{200 \frac{V_{RX}}{600}(3)}{\frac{V_{RX}}{600}(600)} = 1 \text{ (EQ. 13)}$$

Table 2 lists the AC voltage gains for the HC5509 family of SLICs:

TABLE 2. AC VOLTAGE GAINS

PART	AC GAIN 4-WIRE TO 2-WIRE	AC GAIN 2-WIRE TO 4-WIRE
HC5509B	1	1
HC5509A1R3060	1	0.5
HC5524	1	0.833
HC5517	1	1/3



NOTE: Grounded for AC Analysis

FIGURE 1. AC VOLTAGE GAIN AND IMPEDANCE MATCHING



No. AN9632 December 1996

# Harris Telecom

# Operation of the HC5523, HC5515 Evaluation Board

Authors: Don LaFontaine, Ed Berrios

#### **Features**

- · Includes the Ringing Relay
- Toggle Switch Programming for Logic States
- Convenient Monitoring of DET Via LED or Banana Jack Output
- Logic Terminal Port for Easy Evaluation in Existing Systems
- Includes On-Board Op Amp for Evaluation of Transhybrid Balance
- · Pulse Metering Capability

## **Applications**

 Solid State Line Interface for Digital and Analog Telephone Line Cards

## Functional Description

The HC5523/15EVAL Subscriber Line Interface Circuit (SLIC) evaluation board has provisions for full evaluation of the voice and DC feeding characteristics of the HC5523 and the HC5515, including the ringing function.

SLIC functional control is provided using the toggle switches E0, E1, C1 and C2. The logic truth tables for the HC5523 and the HC5515 are shown in Table 2 and Table 3 respectively. DET is available at both a banana jack for monitoring with test instrumentation, as well as an LED for visual verification.

# Applying Power to the HC5523/15EVAL

#### **Power Supply Connections**

The HC5523/15EVAL requires three external power supplies for operation. The supply voltages are labeled on the HC5523/15EVAL as V $_{\rm CC}$ +5V, V $_{\rm EE}$ -5V and V $_{\rm BAT}$ . The typical supply currents, when the SLIC is in the Active mode and terminated with a  $600\Omega$  load, are given in Table 1.

**TABLE 1. POWER SUPPLY INFORMATION** 

SUPPLY	TYP (V)	TYP (mA)
V <sub>CC</sub> +5V	+5	11
V <sub>EE</sub> -5V	-5	1
V <sub>BAT</sub> , R <sub>SG</sub> is Open Circuit	-28	27
V <sub>BAT</sub> , R <sub>SG</sub> is 4.0kΩ	-48	30

#### **Ground Connections**

The HC5523/15EVAL has two separate grounds designated as AGND and BGND. AGND is the analog ground reference for the SLIC. BGND is the battery ground reference, and is to be connected to zero potential. All loop current and longitudinal current flow from this ground. For proper SLIC operation, AGND and BGND must be connected to a common ground, with a potential difference not exceeding ±100mV.

#### HC5523/15EVAL Board SLIC Controls

The design of the HC5523/15EVAL board incorporates five SPDT switches. Four of the switches control the functional state of the SLIC and the fifth controls the DET output.

#### **Mode Control Switches**

The four switches labeled E0, E1, C1 and C2 are used to set the operational mode of the HC5523. Three switches labeled E0, C1 and C2 are used to set the operational mode of the HC5515. Each switch is a Single Pole Double Throw (SPDT) switch with a center open position.

The two inputs labeled E0 and E1 are enable pins. The two pins labeled C1 and C2 are used to select 1 of 4 operating states of the SLIC. Refer to the HC5523 or the HC5515 data sheet for a full description of the functionality of each pin.

If off-board mode control of the SLIC is desired, the four switches can be set to center open position and driven by logic at the logic terminal port. The logic terminal port is located just below the toggle switches at the bottom of the board. A common ground must exist between the HC5523/15EVAL evaluation board and the off board logic. A differential ground voltage may result in erroneous logic states at the SLIC inputs.

#### **DET** Select Switch

A switch is provided on the evaluation board to direct the DET signal to one of two outputs. With the switch positioned to the right, DET will illuminate the LED, when positioned to the left, DET may be monitored at the banana jack using an oscilloscope.

## Verifying the HC5523/15EVAL Operation

The operation of the HC5523/15EVAL and the sample part can be verified by performing six tests:

- 1. Power Supply Current Verification.
- 2. Active Mode Verification.
- 3. Standby Mode Verification.
- 4. SLIC Gain Verification.
- 5. Ring Trip Detector Verification.
- 6. Transhybrid Balance Verification.

The first four tests require a  $600\Omega$  load, an AC volt meter and an oscilloscope. The last test requires a telephone and a battery backed AC source. All of the tests require three external supplies, one each for  $V_{CC}$ ,  $V_{FF}$ , and  $V_{BAT}$ .

Verify that the sample HC5523 or the HC5515 included with the evaluation board is oriented in its socket correctly. Correct orientation is with pin 1 pointing towards the bottom of the board.

Application Tip: When terminating tip and ring on the HC5523/15EVAL, it is handy to assemble terminators using a Pomona MDP dual banana plug connector as the terminating resistor receptacle. Refer to Figure 1 for details.

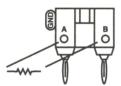


FIGURE 1. TERMINATION ADAPTER

Using the termination shown in Figure 1 provides an unobtrusive technique for terminating tip and ring while still providing access to both signals using the banana jack feature of the MDP connector. Posts are also available that fit into holes A and B, providing a solderable connection for the terminating resistor.

#### **Test No. 1 - Power Supply Current Verification**

A quick check of evaluation board and the sample is to measure the currents of each supply voltage. The readings should be similar to the values listed in Table 1. The measurements can be made using a series ammeter on each supply, or power supplies with current displays.

#### Setup:

- 1. Connect the power supplies to the HC5523/15EVAL.
- 2. Set V<sub>BAT</sub> to -48V.
- 3. Connect AGND and BGND to common ground point.
- 4. Connect V-REC pin to common ground point.
- 5. Terminate the HC5523 or the HC5515 with  $600\Omega$  load across Tip and Ring.
- 6. Set the mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.

#### Discussion:

Once setup is complete, apply power to the HC5523/15EVAL and verify the supply currents listed in Table 1. Note that special power supply sequencing is not required for either the HC5523 or the HC5515.

#### Test No. 2 - Active Mode Verification

This test verifies loop current operation and loop current detection in the Active mode via the onboard LED.

#### Setup:

- 1. Connect the power supplies to the HC5523/15EVAL.
- 2. Set V<sub>BAT</sub> to -48V.
- 3. Connect AGND and BGND to common ground point.
- 4. Connect V-REC pin to common ground point.
- 5. Terminate the HC5523 or the HC5515 with  $600\Omega$  load across Tip and Ring.
- 6. Set the mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.
- 7. Position the DET select switch to the right.

#### Discussion:

When power is applied to the SLIC a loop current will flow from tip to ring through the  $600\Omega$  load. This loop current triggers an internal detector that pulls the output of  $\overline{\text{DET}}$  low, illuminating the LED through the +5V supply. Once the LED illuminates, remove the  $600\Omega$  termination and verify that the LED turns off.

#### Verification:

- 1. LED is on when tip and ring are terminated with  $600\Omega$ .
- 2. LED is off when tip and ring are open circuit.

#### Test No. 3 - Standby Mode Verification

This test verifies loop current operation and loop current detection in the Standby state via the banana jack interface.

#### Setup:

- 1. Connect the power supplies to the HC5523/15EVAL.
- 2. Set V<sub>BAT</sub> to -48V.
- 3. Connect AGND and BGND to common ground point.
- 4. Connect V-REC pin to common ground point.
- 5. Terminate the HC5523 or the HC5515 with  $600\Omega$  load across Tip and Ring.
- 6. Set the mode switches to E0 = 0, E1 = 1, C1 = 1, C2 = 1.

- 7. Position the DET select switch to the left.
- 8. Connect an oscilloscope or DC voltmeter to the DET jack.
- 9. Monitor the V<sub>BAT</sub> supply current.

#### Discussion:

When power is applied to the SLIC, loop current will flow from tip to ring through the  $600\Omega$  load. This loop current triggers an internal detector that pulls the output of  $\overline{D\text{ET}}$  near zero volts. Disconnecting the  $600\Omega$  termination will cause  $\overline{D\text{ET}}$  to be pulled to the  $V_{CC}$  rail. In Standby mode, the  $V_{BAT}$  current should be approximately 16.4mA with the  $600\Omega$  termination and 0.8mA without the  $600\Omega$  termination.

#### Verification:

- 1.  $\overline{\text{DET}}$  is near 0V when terminated with 600 $\Omega$ .
- 2.  $\overline{\text{DET}}$  is near the V<sub>CC</sub> rail when not terminated with 600 $\Omega$ .
- 3. V<sub>RAT</sub> current is near 16.4mA when terminated.
- 4. V<sub>BAT</sub> current is near 0.8mA when not terminated.

#### Test No. 4 - SLIC Gain Verification

This test will verify that SLIC is operating properly and that the SLIC is exhibiting unity gain. Unity gain will only exist if the SLIC is properly terminated with  $600\Omega$ .

#### Setup:

- 1. Connect the power supplies to the HC5523/15EVAL.
- 2. Set V<sub>BAT</sub> to- 48V.
- 3. Connect AGND and BGND to common ground point.
- 4. Terminate the HC5523 or the HC5515 with  $600\Omega$  load across Tip and Ring.
- 5. Set the mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.
- 6. Connect a sine wave generator to the V-REC input.
- 7. Set the generator for 0.775V<sub>BMS</sub> and 1kHz.
- 8. Connect an AC voltmeter across tip and ring.

#### Discussion:

When terminated with  $600\Omega$ , the SLIC will exhibit unity gain from the V-REC input pin to across tip and ring. The unity gain results from the matched impedance that the  $600\Omega$  termination represents to the internally synthesized  $600\Omega$  of the SLIC. When an open circuit exists, a mismatch occurs and the gain of the SLIC will double.

#### Verification:

- 1. Tip to ring AC voltage of 0.775V<sub>RMS</sub> when terminated.
- 2. Tip to ring AC voltage of  $1.55V_{RMS}$  when not terminated.

#### **Test No. 5 - Ring Trip Detector Verification**

This test will verify the ringing function of the SLIC. A telephone and an AC signal source are the only additional hardware required to complete the test.

#### Setup:

- 1. Connect the power supplies to the HC5523/15EVAL.
- 2. Set V<sub>RAT</sub> to -28V.
- 3. Connect AGND and BGND to common ground point.
- 4. Connect V-REC pin to common ground point.
- 5. Set the mode switches to E0 = 0, E1 = 1, C1 = 1, C2 = 0.
- 6. Connect the telephone across tip and ring.
- Connect battery backed AC (20 Hz oscillator) to RING-ING (V<sub>RAT</sub> + 90V<sub>RMS</sub>) banana jack.
- 8. Position DET select switch to the right (for LED).

#### Discussion:

The  $600\Omega$  termination is not necessary for this test since the phone provides this nominal impedance when off-hook. Setting the mode switches as shown above will cause the RIN-GRLY pin of the SLIC to energize the relay that is on the evaluation board. The  $D_T$  and  $D_R$  comparator inputs will sense the flow of DC loop current, causing the Ring Trip comparator to sense when the phone is either on-hook or off-hook. Refer to the HC5523 or the HC5515 data sheet for a full description of the functionality of the Ring Trip Detector.

#### Verification:

- 1. Phone starts ringing when power applied to test setup.
- 2. While ringing and on-hook, DET LED is not illuminated.
- 3. While ringing, going off-hook will illuminate the LED.

CAUTION: Short time durations of off-hook should be maintained to protect R<sub>RT</sub>. In systems, the ring relay is software controlled to turn off milliseconds after off-hook is detected, hence limiting power dissipated in R<sub>RT</sub>.

- 4. When phone is returned to on-hook, LED will turn off.
- 5. Configure SLIC in Active mode to stop phone from ringing. Set mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.

#### Test No. 6 - Transhybrid Balance Verification

This test will verify the transhybrid balance circuitry for both the voice path and the pulse metering (TELETAX) path. A low distortion AC signal and a voltmeter are the only additional hardware required to complete this test.

#### **Voice Path**

#### Setup:

- 1. Connect the power supplies to the HC5523/15EVAL.
- 2. Set V<sub>BAT</sub> to -48V.
- 3. Connect AGND and BGND to common ground point.
- 4. Terminate the HC5523 or the HC5515 with  $600\Omega$  load across Tip and Ring.
- 5. Set the mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.
- Set the AC source to 1V<sub>RMS</sub>, 1kHz and apply to the V-REC input.
- 7. Connect an AC voltmeter between the V-XMIT and GND.

#### Discussion:

Transhybrid balance is a measure of how well the input signal is canceled (that being received by the SLIC) from the transmit signal (that being transmitted from the SLIC). Without this function, voice communication would be difficult because of the echo.

#### Verification:

- 1. Measure the AC voltage at V-XMIT output.
- 2. Calculate the Transhybrid balance using Equation 1.

Transhybrid(dB) = 
$$20 \times log \frac{V - XMIT}{1V_{RMS}}$$
 (EQ. 1)

3. The value should be approximately -40dB.

#### **Pulse Metering Option**

#### Setup:

- 1. Connect the power supplies to the HC5523/15EVAL.
- 2. Set V<sub>BAT</sub> to -48V.
- 3. Connect AGND and BGND to common ground point.
- 4. Terminate the HC5523 or the HC5515 with  $600\Omega$  load across Tip and Ring.
- 5. Set the mode switches to E0 = 0, E1 = 1, C1 = 0, C2 = 1.
- Set the AC source to 1V<sub>RMS</sub>, 12kHz or 16kHz and apply to the V-PM input.
- 7. Connect an AC voltmeter between the V-XMIT and GND.

#### Discussion:

The pulse metering signal is a 12kHz or 16kHz signal that is injected on to the tip and ring lines. This signal is monitored by a counter (non-U.S. markets) inside the pay phone, which tallies up the cost of the call.

#### Verification:

- 1. Measure the AC voltage at V-XMIT output.
- 2. Calculate the Transhybrid balance using Equation 1.
- 3. The value should be approximately -25dB.

## Passive Components

The HC5523/15EVAL design incorporates all of the external components necessary for using the HC5523 or the HC5515 in normal applications. A brief description of each component is provided below. The components will be grouped by function to provide further insight to the operation of the HC5523/15EVAL board.

#### TWO WIRE SIDE, TIP AND RING

Relay	Allows injection of ringing signal.
PTC	Provides thermal protection for relay to ground path during extended periods of use. The PTC is not provided with HC5523/15EVAL board.
R <sub>F1</sub> , R <sub>F2</sub>	Feed resistors that limit the current into the tip and ring inputs of the SLIC.
D <sub>1</sub> D <sub>4</sub>	Provide transient protection on the tip and ring inputs.
C <sub>TC</sub> , C <sub>RC</sub>	Provide immunity against high frequency noise on tip and ring respectively.

The Two Wire Side components are typical telephone values. Design equations are not used for these components.

#### RING TRIP DETECTOR

R <sub>1</sub> , R <sub>2</sub>	Generate a bias voltage from $V_{\mbox{\footnotesize BAT}}$ to drive the RD pin.
R <sub>3</sub> , R <sub>4,</sub> R <sub>RT</sub>	Combine to sense off-hook condition and drive the RT pin.
C <sub>RT</sub>	Provides attenuation of the ring signal for stability of DT pin.

The component values for the Ring Trip Detector circuit do not require design equations. For information concerning the functionality of this supervisory function refer to the "Supervisory Function" section of the HC5523 or the HC5515 Data Sheet.

#### LOOP CURRENT DETECTOR

R <sub>D</sub>	Sets the loop current detect threshold for the SLIC's internal comparator function.
----------------	---

The value of  $R_D$  programs the loop current detect threshold for the SLIC. Since the internal comparator has hysteresis, there are two equations that apply to the value of  $R_D$ . One equation is for on-hook to off-hook threshold, and the other is for off-hook to on-hook threshold. The equations for each condition are as follows:

On-Hook to Off-Hook Threshold

$$R_{D} = \frac{465}{I_{ON-HOOK to OFF-HOOK}}$$
 (EQ. 2)

Off-Hook to On-Hook Threshold

$$R_{D} = \frac{375}{I_{OFF-HOOK to ON-HOOK}}$$
 (EQ. 3)

For details concerning the design equations refer to the "Supervisory Function" section of the HC5523 or the HC5515 Data Sheet. As delivered, the HC5523/15EVAL is configured for a loop current detect level of 11.9mA for onhook to off-hook, and 9.6mA for off-hook to on-hook.

#### SATURATION GUARD RESISTOR

R <sub>SG</sub>	Sets the saturation guard for the SLIC.

When operating in systems with a -28V battery,  $R_{SG}$  needs to be an open circuit. When operating in systems with a -48V battery,  $R_{SG}$  needs to be 4.0k $\Omega$  as per the following equation:

$$R_{SG} = \frac{5 \cdot 10^5}{|V_{BAT}| - V_{MAR} - 16.66V} - 17300$$
 (EQ. 4)

For details concerning the design equations refer to the "Constant Loop Current (DC) Path" section of the HC5523 or the HC5515 Data Sheet. As delivered, the HC5523/15EVAL is configured for a saturation guard of 4V on both the tip side and ring side, resulting in a V<sub>MARGIN</sub> of 8V for V<sub>BAT</sub> of -48V.

#### FOUR WIRE SIDE, SLIC IMPEDANCE MATCHING

R <sub>T</sub>	Sets the synthesized impedance across the tip and ring terminals.
R <sub>RX</sub>	Performs a voltage to current conversion of the receive signal. Selected to maintain unity gain from 4-wire to 2-wire side when SLIC is terminated with $600\Omega$ .

The values of  $R_T$  and  $R_{RX}$  have been selected for a  $600\Omega$  system. These values can be modified for different impedances. Also, complex impedance matching is possible using these components. For information on impedance matching of the SLIC, refer to the "(AC) 2-Wire Impedance" section of the HC5523 or the HC5515 Data Sheet.

#### CONSTANT FEED CURRENT PROGRAMMING

R <sub>DC1</sub> , R <sub>DC2</sub>	Sets the constant feed current that flows from tip to ring when a DC path is present during off-hook conditions. Resistance is split to allow capacitor for filtering ( $C_{DC}$ ).
C <sub>DC</sub>	Filter capacitor to attenuate high frequency noise that is fed back from tip and ring.

The constant feed current is programmed using the sum of  $R_{DC1}$  and  $R_{DC2}$ . The design equation used to set the loop current is shown below.

$$I_{L} = \frac{2.5V}{R_{DC1} + R_{DC2}} \times 1000$$
 (EQ. 5)

For details concerning the design equations for loop current as well as the selection of C<sub>DC</sub> refer to the "Constant Loop Current (DC) Path" section of the HC5523 or the HC5515 Data Sheet. As delivered, the constant feed current is set at 30mA

#### TRANSHYBRID BALANCE

U2	Op-amp used for transhybrid balance:
R <sub>TX</sub> , R <sub>B,</sub> FB, RPM	Used as part of transhybrid balance circuitry that is located off board.

Transhybrid balance is accomplished by using an external op amp (U2, usually part of the CODEC) and by the inversion of the signal from the 4-wire receive port (RSN) to the 4-wire transmit port ( $V_{TX}$ ). The input signal will be subtracted from the output signal if  $I_1$  equals  $I_2$  (Figure 2). Node analysis yields the following equation:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 (EQ. 6)$$

The value of Z<sub>B</sub> is then

$$Z_{B} = -R_{TX} \cdot \frac{V_{RX}}{V_{TX}}$$
 (EQ. 7)

Where V<sub>RX</sub>/V<sub>TX</sub> equals 1/ A<sub>4-4</sub>

Therefore,

$$Z_{B} = R_{TX} \cdot \frac{Z_{RX}}{Z_{T}} \cdot \frac{Z_{T}}{1000} + 2R_{F} + Z_{L}$$
 (EQ. 8)

Example:

Given:  $R_{TX}$  =  $20k\Omega,~Z_{RX}$  =  $280k\Omega,~Z_{T}$  =  $562k\Omega$  and  $Z_{L}$  =  $600\Omega$  and  $R_{F}$  =  $20\Omega$  .

The value of  $Z_B = 18.7k\Omega$  1%.

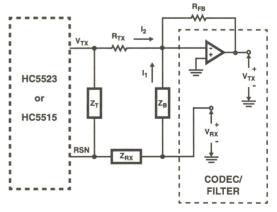


FIGURE 2. TRANSHYBRID CIRCUIT

# Logic Truth Table

The logic truth tables for the HC5523 and the HC5515 are options available selecting the supervisory signal that drives shown in Table 2 and Table 3 respectively. The SLIC has four the DET pin. The supervisory signals are Ground Key Detect operating states. The states are Open Circuit, Active, Ringing and Standby. Each state, except Open Circuit, has

(HC5523 only), Loop Current Detect and Ring Trip Detect.

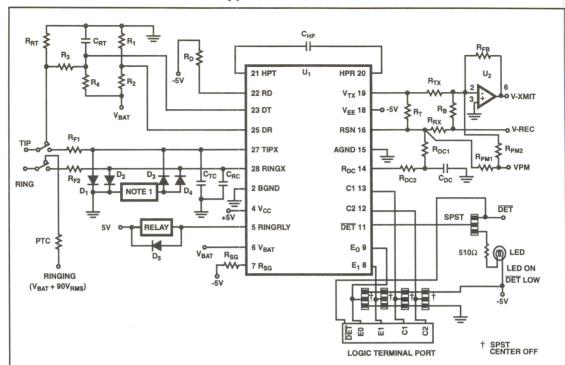
# HC5523/15 SLIC Operating States

TABLE 2. HC5523 LOGIC TRUTH TABLE

E0	E1	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	DET OUTPUT	
0	0	0	0	Open Circuit	No Active Detector	Logic Level High	
0	0	0	1	Active Ground Key Detector Gro		Ground Key Status	
0	0	1	0	Ringing No Active Detector L		Logic Level High	
0	0	1	1	Standby Ground Key Detector		Ground Key Status	
0	1	0	0	Open Circuit	No Active Detector	Logic Level High	
0	1	0	1	Active	Loop Current Detector	Loop Current Status	
0	1	1	0	Ringing	Ring Trip Detector	Ring Trip Status	
0	1	1	1	Standby	Loop Current Detector	Loop Current Status	
1	0	0	0	Open Circuit	No Active Detector	,	
1	0	0	1	Active	Ground Key Detector		
1	0	1	0	Ringing	No Active Detector		
1	0	1	1	Standby	Ground Key Detector	71	
				Logic Level High			
1	1	0	0	Open Circuit	No Active Detector		
1	1 1 0 1		Active	Loop Current Detector			
1	1	1	0	Ringing Ring Trip Detector			
1	1	1	1	Standby	Loop Current Detector	,	

#### **TABLE 3. HC5515 LOGIC TRUTH TABLE**

E0	C1	C2	SLIC OPERATING STATE ACTIVE DETECTOR		DET OUTPUT	
0	0	0	Open Circuit	No Active Detector	Logic Level High	
0	0	1 .	Active	Loop Current Detector	Loop Current Status	
0	1	0	Ringing	Ring Trip Detector	Ring Trip Status	
0	1	1	Standby Loop Current Detector		Loop Current Status	
1	0	0	Open Circuit	No Active Detector	1	
1	1 0 1		Active	Loop Current Detector	Logic Level High	
1	1 1 0		Ringing	Ring Trip Detector		
1	1	1	Standby	Loop Current Detector	1	



#### NOTE:

 The anodes of D<sub>3</sub> and D<sub>4</sub> may be connected directly to the V<sub>BAT</sub> supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D<sub>3</sub> and D<sub>4</sub> be shorted to ground through a transzorb or surgector.

FIGURE 3. DEMO BOARD SCHEMETIC

# HC5523/15EVAL Evaluation Board Parts List

TABLE 4. EVALUATION BOARD PARTS LIST

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	HC5523 or I	HC5515		R <sub>PM2</sub>	18.7kΩ	1%	1/4W
U2	CA741C OpAmp			R <sub>RT</sub>	150Ω	5%	2W
R <sub>F1</sub> , R <sub>F2</sub>	20Ω	1% match	1/2:W	R <sub>SG</sub> , V <sub>BAT</sub> = -48V	4.0kΩ	1%	1/4W
R <sub>1</sub> , R <sub>3</sub>	200kΩ	5%	1/4W	R <sub>DC1,</sub> R <sub>DC2</sub>	41.2kΩF	5%	1/4W
R <sub>2</sub>	910kΩ	5%	1/4W	C <sub>DC</sub>	1.5μF	20%	63V, (npo)
R <sub>4</sub>	1.2ΜΩ	5%	1/4W	C <sub>HP</sub>	10nF	20%	100V, (npo)
R <sub>B</sub>	18.7kΩ	1%	1/4W	C <sub>RT</sub>	0.39μF	20%	100V, (npo)
R <sub>D</sub>	39kΩ	5%	1/4W	C <sub>TC,</sub> C <sub>RC</sub>	2200pF	20%	100V, (npo)
R <sub>FB</sub>	20.0kΩ	1%	1/4W	D <sub>1</sub> . D <sub>4</sub>	1N4007 or E	Equivalent	100V, 3A
R <sub>RX</sub>	280kΩ	1%	1/4W	D <sub>5</sub>	1N914	N/A	N/A
R <sub>T</sub>	562kΩ	1%	1/4W	PTC	Shorted	N/A	N/A
R <sub>TX</sub>	20kΩ 1% 1/4		1/4W	K <sub>R</sub>	2C Contacts	s, 12V Coil	N/A
R <sub>LED</sub>	510Ω	10%	1/4W	Textool Socket	228-5523		
R <sub>PM1</sub>	280kΩ	1%	1/4W				

# HC5523/15EVAL Evaluation Board Layout

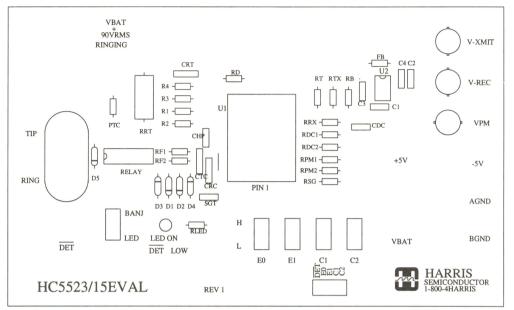
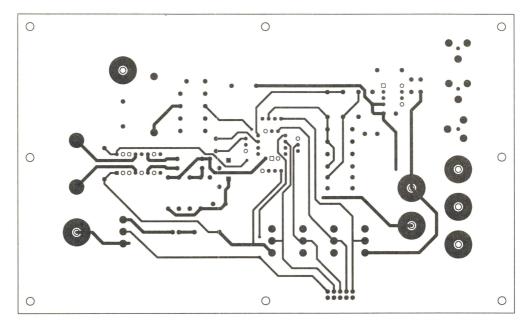


FIGURE 4. SILK SCREEN

# HC5523/15EVAL Evaluation Board Layout (Continued)



NOTE: Board dimensions not actual size.

FIGURE 5. TOP SIDE

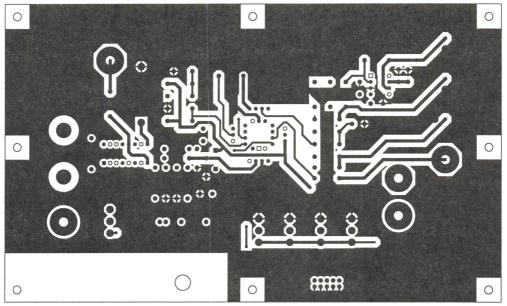


FIGURE 6. BOTTOM SIDE

COMMUNICATIONS

# MAPROTE

No. AN9636.2 June 1997

# Harris Telecom

# Implementing an Analog Port for ISDN Using the HC5517

Authors: Dave Feller, Don LaFontaine

#### Introduction

With the need for faster and faster data communications for the home and office, more and more people are turning to the ISDN (Integrated Services Digital Network) line as a solution. The standard data modem that operates over a twisted pair telephone line has been traditionally limited to 28,800 B/s. Compression algorithms and special modulation techniques have pushed the data rate to the extremes. The limited bandwidth of the twisted pair and standard central office SLICs and CODEC's puts an upper limit on the possible data rates. The industry has just about reached that limit. There are quite a few options available to increase the data rates to the outside world including ADSL/VDSL modems, bringing a T1 connection straight to the computer (1.544 Mb/s - typical for video teleconferencing setups), and even fiber optic cabling. However, most of these options are very expensive or are not yet available in all areas of the country. ISDN provides an affordable, available, supported solution to the need for higher data rates.

This application note includes a brief discussion of ISDN and ISDN signaling, the use of the HC5517 as an interface between the analog subscriber side and the digital ISDN line, and provides a detailed description of the hardware interface. A good understanding of the hardware is necessary to understand ISDN protocol so that software can be written to properly control the SLIC and translate analog queues into ISDN signal commands. The discussion of the hardware will include the SLIC, the power supply, all appropriate signaling circuitry, glue circuitry to a standard analog interface, and battery backup recommendations.

# Implementing ISDN in the Home or Office

ISDN is an entirely digital system, it is not backwards compatible with any of the analog equipment on the market today (telephones, fax machines, modems, answering machines, etc.). To allow backwards compatibility, a method is needed to allow an analog device to be plugged into the ISDN line. That need has pushed the creation of the HC5517 ringing SLIC. The concept is actually simple: move the standard SLIC (Subscriber Line Interface Circuit) and CODEC that normally controls a telephone from the central office to the home.

Having the SLIC/CODEC local presents a new set of challenges for the designer. The standard telephone commands and signaling techniques must now be taken care of locally, and perhaps more importantly the ring signal must be generated locally. The HC5517 SLIC allows the ring signal to be routed and driven through the SLIC instead of using relays and high power high voltage generators to ring the phone. The functions of an At The Home SLIC (ATH SLIC) will be discussed shortly, but suffice it to say that the HC5517 will make the ringing function easier and cheaper than conventional methods.

#### ISDN Basics

#### **Data Rates and Services**

It is important to note that an ISDN line in any form is a true digital interface to the service provider, and all the data rates discussed below are true digital rates and not analog modulated digital information.

ISDN service comes in two forms: Basic Rate Interface (BRI), and Primary Rate Interface (PRI). BRI is the typical ISDN line purchased by individuals and most small businesses. It consists of a total possible data rate of 128KB/s with a 16KB/s data channel added for signaling and control. The 128K total throughput can be broken down into two distinct digital channels of 64KB/s each called Bearer (B) channels. The 16KB signaling and control channel is referred to as the D channel. Therefore, the BRI is commonly referred to as 2B + D indicating two 64K channels for data and one 16KB data channel for signaling. Each B channel is independent and two separate calls can be made at the same time by making use of both B channels, or they can be synchronously combined in software with the proper protocol to provide a total of 128K to a single destination. The PRI is simply a large grouping of B channels that can be purchased at great expense for very high speed communications. This interface is usually only purchased by larger corporations or service providers but is included here for completeness. The total bandwidth of the PRI is based on the predominant carrier trunk in the area, so in the US the total bandwidth is 1.544MB/s (T1) and in Europe it is 2.048MB/s (E1). The 1.544MB/s is broken down into 24 individual 64KB lines one of which is reserved for signaling much like the 2B + D line. Therefore the PRI in the USA is commonly referred to as a 23B + D connection.

The basic 64KB/s data rate is derived from the present analog system. The typical bandwidth of standard analog tele-

phone connection is very nearly 3,500Hz or 4,000Hz if rounded up to the nearest thousand. Nyquist tells us that we must over sample by two to get an accurate reproduction of the digitized waveform; that brings us to 8K. If we take 8 bits of data for each sample that indicates that the primary bandwidth needed for a standard analog connection is 64KB/s. It is therefore logical that the standards should use this rate since the equipment already in place must be utilized. So each B channel assigned is treated like any other digitized analog connection once it reaches the switch (more or less).

#### Interface Breakdown

With a 2B + D entering the home, the next major goal is to connect an analog device to it via some interface box. The interface solution can vary depending on what kind of device is being plugged in as well as where it is located (see Figure 1). The two wire connection that the service provider installs is generally referred to as the U interface. It is transformer coupled and generally converted to a four wire S interface that can be distributed within a reasonable distance within an office. The U interface is a standard RJ11 jack and the S interface is usually an RJ45 iack like a standard Ethernet connection. Unlike an analog telephone, only one device can be plugged into a U interface at a time. This is the primary reason for converting to an S interface; up to 8 devices can be plugged into an S interface and each can have its own unique address. An obvious conflict arises if three different S interface devices each request a B channel and the U interface is a standard 2B + D connection; one of them simply has to wait. The S interface is extremely useful if the number of users is small and the individual usage times are short, or if there are a number of different devices that are to be plugged in. The device that converts from U to S is called a Network Termination (NT-1) and can either be a stand alone device or it can be built into a LAN card. The final interface is generally a high speed serial port like RS232. A device can be purchased to convert from U or S to RS232 and is referred to as a Terminal Adapter (TA). TAs can also be purchased as stand alone or integrated units. These are primarily useful if all IRQs or ISA/PCI slots are used up, or if the desired device needs to be backwards compatible with standard Hayes modem commands and normal communications software.

## The NT-1

This primary conversion point is an ideal spot for an analog port for a standard telephone connection. This provides a main port access to standard communications systems for system check and ease of initial setup. If any part of the system is working it is likely to be the U interface since it is the direct line to the service provider. An analog port here with a simple battery backup is also necessary for emergency communications in the event of a power failure. The closer to the U interface the more likely a connection can be established. The HC5517 ringing SLIC described below makes the analog port interface a simple task.

#### The ISDN Modem Card (NT-1 included)

Since the U interface is the primary connection to the home, most ISDN modems available on the commercial market will most likely include an NT-1 on board so that there is no accessible S interface. This is primarily because the vast

majority of users will only need one connection per site. A card that plugs directly into the U interface and provides conversion to ISA or PCI is the most likely place to have an analog port or two. An analog port provides the user with the ability to utilize standard telephones as well as fax machines, answering machines, modems, and even caller ID services.

#### The S-BUS ISDN Modem Card

The S interface LAN card while functionally similar to the standard ISDN modem card does not include an on board NT-1. The typical S interface card plugs into an external NT-1 via an RJ45 connector and is typically located within a few hundred feet of that NT-1. These modems are primarily used in small businesses and multiple computer sites that all require periodic ISDN access. The inclusion of analog ports in these cards is identical to that of the standard ISDN modem.

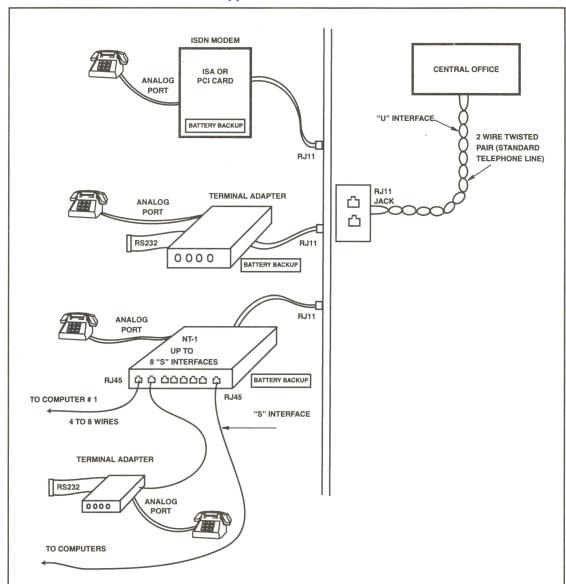
#### **Basic Signaling**

For purposes of this discussion, it will be assumed from here on that we are talking about an analog port that is to be installed into a standard ISDN modern that plugs directly into a PCI or ISA slot. A separate IC vendor will provide the necessary devices to get from a U interface to a four wire analog interface.

If we make the basic assumption that the hardware is in place, then we can focus on analog port control software. The software driving the modern that runs on the host PC must convert the ISDN commands into the proper signals needed by the HC5517 SLIC. The basic interface signals include audio in, audio out, ring generation, switch hook detection, ring trip detection and power supply control. With the exception of the audio signals, these can be any set of I/O pins controllable and readable by the host processor. These hardware connections are shown in detail in the hardware section, but first the steps needed for connection will be discussed.

#### Call Setup Protocol

The process of making a call on ISDN is roughly similar to the progression of a standard telephone call. For the purposes of this discussion, an ISDN call will refer to the process of establishing a link to another computer over an ISDN line and is not necessarily analog port to analog port. The actual service desired (voice, 3.1KB analog, or pure data) that is to be transmitted on the B channel can either be established during call setup or after call connection as a function of normal B channel communications. This setup of the channel is referred to as out-of-band if done during setup and in-band if done after the B channel is connected. Out-ofband is most common for telephony connections via the analog port, and In-band setup is most common for data and 3.1kHz analog (analog modem use). Since a telephone connection normally takes place during call setup, that is the most logical situation to discuss. The following connection process would also take place in the same basic order for the in-band condition.



#### NOTES:

- 1. Only one device can be plugged into the "U" interface at a time!
- Local battery backup is necessary only if ISDN is the only communication line into a home or residence since it is not provided by the telephone company. A power outage would make communication on ISDN impossible without local battery backup.

#### FIGURE 1. INTERFACE BREAKDOWN

For the sake of brevity, the call setup process will be discussed on the level seen by the host software. It is not necessary at this point to get into the actual bit stream commands at the two wire level. To properly envision the process we will consider that only three distinct computers are involved: the originator, the network (the computer controlling the network switch), and the Receiving computer (see Figure 2).

The basic steps are Setup, Call Proceeding, Alerting, Connect, and Connect Acknowledge. These five steps, if identified correctly in software, can be used as the breaking points for proper SLIC control. It should be noted that the D channel of the U interface is normally active and communicating with the central office. A connection usually refers to the connection of the B channels only.

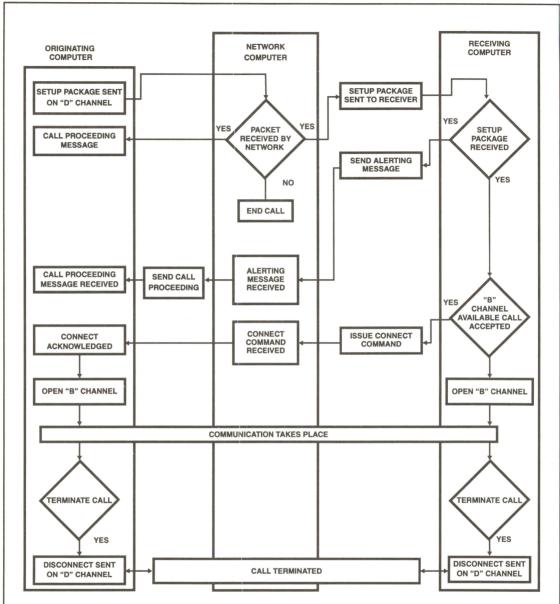


FIGURE 2. CALL SETUP PROTOCOL AN CALL RELEASE

#### Setup

The "setup" step is analogous to dialing an analog telephone. During this process a number of packets are sent over the D channel specifying the originating telephone number, the destination phone number, the quality of line required, the type of transmission to follow including the compounding method if telephony is selected ( $\mu$  law or A law).

This packet is received by the network and passed on to the receiving station. Just after the network passes this packet on (sometimes with slight modification), the network returns a "call proceeding" message back to the originator. There is no direct equivalent in the analog world with the possible exception that a series of clicks or varying static can be heard after completing a DTMF sequence and before ring back begins. The next step is totally dependent on the receiving station. It has to acknowledge the receipt of the

setup packet and return an "alerting" message to the network. The network passes this "altering" message on to the originating station as a "call proceeding" message. This "call proceeding" message is equivalent to ring back in an analog system. At the receiving end, the NT-1 passes the "setup" message on to the end user that may be connected directly, via an S interface, or via a terminal adapter. If a B channel is available and if the intended receiving station accepts the call, it issues a "connect" command to the network. The network passes this command back to the originating station as a "connect acknowledge" message and opens a B channel for both the receiving station and the originating station. The originator processes the "connect" message received and begins to communicate on the B channel with the type of service requested by the original "setup" message. At this point synchronization on the B channels takes place and communication begins.

#### **Call Release**

The process of call release (hang-up) is quite straightforward. It can be initiated by either end of the call in progress at any time since the D channel does not have to wait for any particular pause in the B channel(s) in use. A disconnect signal is sent to the network on the D channel, passed on to the opposite station, and both sides then disconnect their respective B channels as does the network. It should be noted that timers similar to those in an analog interface are used by the network to make sure that no phase of setup or call release hangs up and a line holds open.

#### Services Provided and Handshaking

Simply stated, a service is a method of communication over a B line. This can take the form of a pure data connection using one of the more common protocols such as Point to point Protocol, Multilink Point to Point Protocol or the service can be specified as a telephone voice connection or as a 3.1kHz analog connection for analog modem use. Of course, there are a number of other services such as teleconferencing over a B line, but the three just mentioned are the most common. The two that are of particular interest here are the two analog services. They may seem arbitrary, but specifying one or the other actually optimizes the total bandwidth and the bit error rate of the line in use. Some of the original specs governing ISDN separated these into two categories defining mostly the quality of the line assigned. A voice connection can stand to lose a little data here and there, where a modem connection cannot.

#### Interface Functions

In every telephone system there has to be some way to transform the analog voice signals to a digitally coded bit stream. In a standard telecommunications application, that part is called a CODEC. It provides the Analog to Digital (A/D) and Digital to Analog (D/A) function between the four wire transmit/receive interface to the two wire analog world. It also performs a function called companding that reduces the overall bandwidth of the signal. A part is needed in the ISDN world that provides a similar function as well as telephone control, ring signaling, status detection, and power control. One family of parts that provides these functions is the ARCOFI® by Siemens. Although initially designed to power a separate microphone and loudspeaker for implementing a

crude speaker phone, the ARCOFI makes a good starting platform for the analog interface by providing the following functions:

- a) Analog to Digital Interface.
- b) Digital to Analog Interface.
- c) Switch Hook Detection Interface.
- d) Ring Trip Detection Interface.
- e) Power Supply Control.
- f) Ring Signaling Including Ring Cadence Generation.
- Two Wire Power Denial for rEfusing Access to the ISDN Line Through the Analog Port.
- h) Companding (μ-Law or A-law Selectable).

#### **SLIC Functions**

The HC5517 SLIC provides the two wire to four wire interface, as well as most of the standard Borscht functions needed to completely control the telephone. The basic goal is to make the RJ11 analog port on the ISDN modem card as close as possible to a standard telephone line. The HC5517 accomplishes this by providing the following functions:

#### **Loop Current Generation**

The loop current provides a medium for incoming and outgoing calls to take place, as well as providing power to any DTMF generation circuitry in the phone. Programming of the maximum loop current is performed by resistors  $\rm R_{10}$  and  $\rm R_{28}$  (see Figure 3). Since an ISDN modem application is typically very short loop, the total two wire voltage as well as the loop current are both limited to prevent overheating of the SLIC and wasted power in the modem.

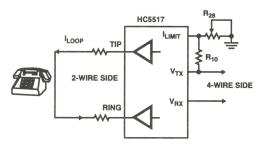


FIGURE 3. LOOP CURRENT GENERATION

#### **Switch Hook Detection**

The SHD pin on the HC5517 goes low whenever the telephone goes off hook. This provides an indication of the status of the telephone set as well as providing a signal to the ISDN interface to begin an ISDN connection upon call initiation

#### **Ring Trip Detection**

The RTD pin on the HC5517 goes low whenever the telephone goes off hook during a ring period. This provides signaling to the ISDN interface to stop ringing and answer the incoming call on the ISDN line by sending a CONNECT command to the network.

#### **Ring Generation**

This function of the HC5517 is the primary advantage of using this type of SLIC over a standard Central Office SLIC. The standard topology to ring a telephone is shown in Figure 4.

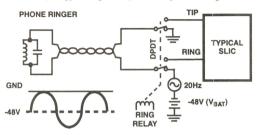


FIGURE 4. BATTERY BACKED RINGING

Typically the SLIC is removed from the two wire side by a DPDT relay which then inserts a high current 20Hz AC signal biased on top of  $V_{BAT}$  which is typically -48 $V_{DC}$ . The resulting waveform is also shown in Figure 4. This is called battery backed ringing since the 20Hz AC signal is backed or biased up by the battery voltage. Obviously this method requires a separate high power AC signal generator precisely tuned to 20Hz; that can get expensive and bulky. This is the type of ringing approved by TR57 and required for all central office applications. However, since the ISDN modem is not connected to the standard analog telephone system, and is therefore not directly governed by that part of the TR57 spec, some liberties can be taken to allow a much simpler design that is much more cost effective.

The HC5517 topology to ring a telephone is shown in Figure 5. Instead of removing the SLIC from the two wire lines as in the standard central office topology, the SLIC is left connected and the ring signal is supplied by the large amplifiers feeding the tip and ring lines internal to the SLIC. If the control line (RC) goes high, the SLIC is put into ring mode. In this mode the tip and ring terminals both slew to  $V_{\rm BAT}/2$  (40V if the  $V_{\rm BAT}$  power supply is at 80V). Any signal on the  $V_{\rm RING}$  pin is multiplied by a gain of 40 and appears across the tip and ring amplifiers. The rest of the hardware involved in this process will be described in the "Glue Circuitry" section.

The circuit in Figure 5 provides balanced non battery backed ringing at power levels adequate to ring 3 REN. A REN (Ringing Equivalency Number) is defined in the FCC specs as a standard impedance by which telephone systems can be measured and tested. A single REN is generally equivalent to an old desktop telephone with mechanical bell ringers. Therefore, the HC5517 would be capable of ringing up to three of these old phones. The vast majority of newer phones use piezo or other electronic ringers that make use of only a fraction of a REN. In that type of situation many phones could be rung simultaneously. The ring signal is also not battery backed; this brings the peak voltages down to a much lower level that is simpler and cheaper to generate and creates less of a safety issue inside the computer (see Figure 5). Telephones and other equipment only respond to the AC RMS signal, so the lack of a DC bias is not a requirement for ring. The primary requirement to ring all telephones reliably is for

the ringing voltage to be at least 40V<sub>RMS</sub> at 20Hz. Some other papers indicate that all phones will ring with a peak of 56V<sub>RMS</sub> and a crest factor of only 1.2, however that is not the case. A full 1.41 crest factor is needed to ring many newer phones such as those produced by Northern Telecom.

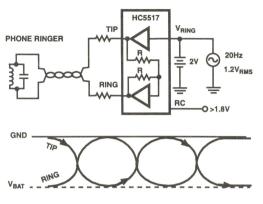


FIGURE 5. BALANCED RINGING

It should be noted that 20Hz is critical since most phones are tuned to respond to a very narrow frequency band around 20Hz. The HC5517 will easily generate the ring signal at this frequency with any desired wave shape. There are three main options for wave shape in the present industry: square wave, trapezoidal wave, and sine wave. TR57 requires a sine wave to reduce channel to channel interference and provide the highest possible energy to the telephone. A square wave is composed of the primary and an infinite number of harmonics that cause interference in adjacent channels and become merely unused energy as the telephone ringer filters out everything but the primary 20Hz. A trapezoidal wave is a compromise of the two. It also wastes some energy in the harmonics and creates a noisy ring signal. Therefore, the sine wave is preferred whenever possible. The HC5517 SLIC will drive any of the above ring signals and provides the most options for ringing of any SLIC on the market.

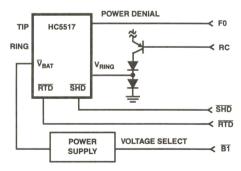


FIGURE 6. SLIC CONTROL AND INTERFACE

#### SLIC Control and Interface

For the most robust control of the analog port, 5 digital I/O lines are needed for communication with the ISDN interface (see Figure 6). These 5 lines can come directly from a device like the Siemens ARCOFI, any controller connected to the S or U interfaces, or directly from the host processor by way of the Peripheral Component Interconnect (PCI) or Industry Standard Architecture (ISA) bus. The 5 signals needed are Switch Hook Detect (SHD). Ring Trip Detect (RTD), Ring Cadence (RC), F1 (power denial pin), and Battery Switch (B1). SHD and RTD are described above in the SLIC functions section. RC is the Ring Cadence input to the SLIC circuitry that gates the sine generator connection to the V<sub>RING</sub> pin and switches the transistor to create the proper DC bias on the V<sub>RING</sub> pin for optimum balanced ringing. RC is normally provided by timing generators that produce a variety of pattern as shown in Table 1. F1 is an input to the SLIC that will put the system in a low power mode. This limits loop current to the two wire side which disables voice and Dual Tone Multi Frequency (DTMF) signals from an external handset. It can be used to password protect the analog port for cost savings since the use of a standard telephone line (if available) is generally cheaper. Finally the B1 is used to switch from the ringing voltage of -80V to the active voltage of -27V.

**TABLE 1. DISTINCTIVE ALERTING PATTERNS** 

	INTERVAL DURATION IN SECONDS									
PAT- TERN			RING- ING	SILENT	RING- ING	SILENT				
Α	0.4	0.2	0.4	0.2	0.8	4.0				
В	0.2	0.1	0.2	0.1	0.6	4.0				
С	0.8	0.4	0.8	0.4	-	-				
D	0.4	0.2	0.6	4.0	-	-				
E	1.2	4.0	-	-	-	-				
F	1 ±0.2	3 ±0.3	-	-	-	-				
G	0.3	0.2	1.0	0.2	0.3	4.0				

TABLE 2. LOGIC STATES FOR APPLICATIONS REQUIRING FAX AND ANSWERING MACHINE OPERATION

STATE	RC	F1	B1	BATTERY (V)
Standby (On-hook)	0	1	0	-80
Ringing (On-hook)	1 (Pulsed)	1	0	-80
Active (Off-hook)	0	1	1	-27
Power Denial	×	0	х	х

#### **Power Needs**

For standby and ringing modes, the SLIC requires  $-80V_{DC}$  and for the off hook active mode the SLIC can be operated at  $-27V_{DC}$  for power conservation (see Table 2). The -80V provides the high energy needed to ring a telephone during the ring period and provides a high enough voltage to create a  $-80V_{DC}$ 

48V potential across the two wire interface during standby operation. In the standby state the application circuit limits the tip to ring voltage to within the Maintenance Termination Unit (MTU) voltage of -42.25 to -56V. The MTU voltage is generated by using the breakover voltage of the external zener diode (D11) to set the internal reference voltage. The MTU potential across the tip and ring wires is not necessary for normal telephone operation, but some fax machines, answering machines, and test equipment look for an MTU voltage to signal on hook active lines. If a system does not need to support fax or answering machines, the -27V supply can be used during all modes except for ringing, see Table 3.

TABLE 3. LOGIC STATES FOR APPLICATIONS NOT REQUIR-ING FAX AND ANSWERING MACHINE OPERATION

STATE	RC	F1	B1	BATTERY (V)
Standby (On-hook)	0	1	1	-27
Ringing (On-hook)	1 (Pulsed)	1	0	-80
Active (Off-hook)	0	1	1	-27
Power Denial	х	0	х	х

Supply currents are minimal since an ISDN modem is truly a short loop application. During the on hook mode, the 80V source only needs to supply a maximum of a few milliamps to the SLIC and its supporting circuitry. During the active mode, the current around the two wire loop is set by external resistors usually somewhere in the range of 25 to 40mA. Therefore the total supply current will be the loop current plus about 5mA for SLIC internal use. During the ring mode the largest amount of power is needed. If we assume that a single REN is roughly equivalent to  $8000\Omega$  resistive (a rough approximation strictly for power consumption calculations) then it can be shown that for each REN connected to a 40V<sub>RMS</sub>/56.6V<sub>PEAK</sub> two wire interface about 7mA of current will be drawn. The maximum power will be drawn at the highest load of 3 REN supported by the HC5517. This creates about 21mA around the two wire loop. The SLIC itself draws about 10mA of internal current during the ring mode so the total is about 31mA at 80V for a fully loaded ringing SLIC.

#### Hardware

#### The Two Wire Side

The two wire interface is the user interface of the analog port. It consists of a pair of wires that closely emulates a standard telephone jack. The polarity of these wires for normal operation is irrelevant. This interface is shown to the left of the SLIC in Figure 11 and the supporting components include the diode bridge (D1-D4) and the four feed/sense resistors (R11-R14). The diode bridge provides a small amount of surge protection for the circuit. Any voltage higher than V<sub>BAT</sub> or lower than ground is chopped off and prevented from reaching the SLIC.

#### The "Glue Circuitry"

A number of intermediate functions can be controlled by external discrete components around the SLIC such as loop current, two wire impedance, transhybrid balance, DC ring

bias, short circuit protection, MTU voltage, and ring trip detection. The application note for the HC5517 evaluation board includes parts for pulse metering, but since ISDN does not perform that function those components will not be discussed here.

The loop current can be set by adjusting resistors R10 and R28. The ratio of R10 to the set resistance on R28 determines the current limit for the two wire loop. The current limit is determined by the following equation:

$$I_{Limit} = 0.6 \frac{(R_{10} + R_{28})}{200 \times R_{28}}$$
 (EQ. 1)

Resistors R8 and R9 should be set to provide a gain of one for the internal transmit op amp. This sets the two wire impedance, as well as the transhybrid balance circuit input. More information on impedance setting can be obtained in Application Note AN9607. A good choice would be 40K resistors as shown in the schematic. C8 provides AC coupling to block the bias generated by the loop current limit pot R28.

Transhybrid balance refers to the electrical canceling of the input signal in the SLIC output. This is necessary because of the full duplex nature of the two wire interface. Both received signals (from the ISDN interface) and transmitted signals (from the handset microphone) are simultaneously present on the two wire interface. Both then appear on the transmit line on the output of the SLIC. If not canceled, the signal originally received from the network would be retransmitted to the network causing an intolerable echo on the line, making communication almost impossible. The simple solution is to remove the original input signal from the signal transmitted to the network. Simply (In + Out)-In = Out. This is accomplished by creating a resistive network around an op amp that sums the currents into a node. The original input signal goes into the node as +In, the summed signal comes out of the SLIC as (-In) + (-Out) and the result is (+In) + (-In) + (-Out) =-Out. The result is inverted by the external op amp and simply becomes +Out. Transhybrid balance therefore, measures the ability of this circuit to cancel the input signal. A number of elements factor in to the value of transhybrid balance, but the better the impedance matching, the better the transhybrid balance and the less echo present. The only other thing to note is the gain of three in the external op amp circuit. This is necessary because of the HC5517's internal gain of one third. Reference Application Note AN9628 "AC Voltage Gain for the 5509 Series of SIIC's".

As previously mentioned, when the RC input goes high the external application circuitry puts the tip and ring voltages at  $V_{BAT}/2$  to provide the most headroom for differential ringing. The circuit used to generate the centering voltage is shown in Figure 7.

The circuitry within the dotted lines is internal to the HC5517. The value of the resistor designated as R is  $108 \mathrm{k}\Omega$  and the resistor R/20 is  $5.4 \mathrm{k}\Omega$ . The tip amplifier gain of  $20 \mathrm{V/V}$  amplifies the  $+1.8 \mathrm{V_{DC}}$  at VC to  $+36 \mathrm{V_{DC}}$  and adds it to the internal  $4 \mathrm{V_{DC}}$  offset, generating  $-40 \mathrm{V_{DC}}$  at the tip amplifier output. The  $-40 \mathrm{V}$  dc offset also sums into the ring amplifier, adding to the battery voltage, achieving  $-40 \mathrm{V}$  at the ring amplifier output.

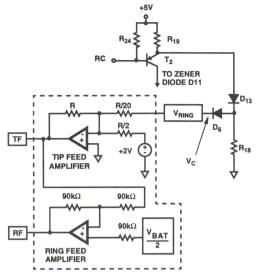


FIGURE 7. BALANCED RINGING

The 1.8V is applied to the  $V_{RING}$  pin when the pnp transistor is turned off by the high on RC. This causes the resistors R18 and R19 to create a simple divider from  $5V_{DC}$  along with a couple of forward diode drops. Putting the  $V_{RING}$  input between the diodes has the effect of isolating the  $V_{RING}$  pin from the resistor to ground seen in R18. That resistor would affect the longitudinal balance, 2-wire return loss and Idle Channel noise.

A simple sine wave generator is needed to provide the proper voltage to the  $V_{RING}$  pin. The proper voltage is one that utilizes the entire headroom so as to provide the greatest ring energy to the telephone, while not being so large as to clip against the rails. The maximum tip to ring voltage is equal to  $V_{BAT}$  minus the output transistor overhead of 6V (3V for tip and 3V for ring). The maximum tip to ring voltage with an 80V supply is 80 -6 = 74V. Therefore, the maximum input voltage to prevent clipping is approximately  $1.3V_{RMS}$ . (1.3\*1.414\*40 =  $74V_{PEAK}$  or  $52.33V_{RMS}$ ). Recall that  $40V_{RMS}$  is the minimum voltage required to ring all telephones so there is considerable headroom in this design. Any input voltage from  $1V_{RMS}$  to  $1.3V_{RMS}$  will normally be acceptable.

When the transistor (T2) is on (RC low) and  $V_{BAT}/2$  is greater than the zener diode (D11) breakdown voltage, D11 clamps the maximum voltage on the  $V_{REF}$  pin and thereby the ring feed amplifier voltage. The maximum DC output voltage of the ring feed amplifier ( $V_{RDC}$ ) is given in Equation 2.

$$V_{BDC} = 2(-V_Z + (V_{BE} - V_{CE})) + 4$$
 (EQ. 2)

The  $V_{RDC}$ , with a 28V zener, is -52.6V (2(-28+0.3) +4). The MTU voltage is the ring voltage minus the tip voltage and is equal to -48.6V.

Short circuit protection is simply provided by the capacitor C16, Figure 11. When the metallic loop current exceeds the set reference level, the SLIC's transconductance amplifier

sources current. This current charges up C16 in the positive direction, causing the ring feed voltage to approach the tip feed voltage, effectively reducing the battery feed across the loop which will limit the DC loop current. The value of the capacitor determines the speed of this reduction.

The Ring Trip Detect circuit uses R15-R17, D5, and C10 to detect the negative high voltage peak when a handset is lifted off hook during a ring interval. Under normal conditions during a ring mode, a high voltage differential sine wave is applied across a relatively high impedance (up to  $8K\Omega$  for 1 REN). This creates a relatively low current and is sensed by the SLIC and output on the V<sub>TX</sub> pin. When the handset is lifted off hook, the metallic contacts provide a much lower impedance to the same applied ring voltage creating a significantly higher AC loop current. This difference in AC current is used for ring trip detection, by putting a trip point between the high and low level output voltages. All that has to be done is rectify that AC voltage, divide down the output voltages, and set a trip point in-between them. The trip point should be high enough to quarantee that noise does not cause an artificial ring trip detection yet low enough to guarantee that even with modest loop lengths and a variety of phones that removing the receiver from the hook crosses the trip point. The resistor divider simply sets this trip point to match the internal 0.24V reference. The capacitor provides a bit of a filter to damp out fast transients that might cause a false ring trip detect. The RTI pin on the SLIC is essentially an input to an internal comparator that trips at 0.24V. To activate the RTD pin, at least 0.24V must appear on the RTI pin. The resistors can be changed to create different trip points for different operating voltages and conditions.

Test bar and RS pins should be pulled high by a 10K resistor.

#### **Sine Wave Generator**

There are literally hundreds of circuits that would provide a cost effective sine wave oscillator for use in the ring circuit, but one of the easiest to understand and implement is a simple Wein bridge oscillator. This straightforward circuit can be found in a majority of college texts and is simple to derive. The basic assumption is that a circuit will oscillate according to the Barkhausen criterion. That is, a circuit will oscillate where the overall loop gain is one and the phase shift is zero. (see Figure 9) The loop equations for the frequency response of the circuit are:

$$V_{\text{in}+j\omega} = \frac{\frac{R}{1+j(RC)}}{\frac{R}{1+j(RC)} + R + \frac{1}{jC}}$$
 (EQ. 3)

Since we add  $\rm R_6$  and  $\rm R_5$  around the negative feedback path, the total loop equation reduces to:

$$T_{(j\omega)} = \left(1 + \frac{R_6}{R_5}\right) \times \left[\frac{1}{3 + J\omega \left(RC - \frac{1}{RC}\right)}\right]$$
 (EQ. 4)

Therefore, the frequency at which the circuit will oscillate is where the phase is zero or:

$$\omega = \frac{1}{BC}$$
 (EQ. 5)

And the gain to sustain oscillation needs to be a total of 1 around the loop so:

$$\left(1 + \frac{R_6}{R_5}\right)\left(\frac{1}{3}\right) = 1$$
 (EQ. 6)

or 
$$R_6/R_5 = 2$$

The amplitude of the oscillation can be controlled with a nonlinear limiter around the entire loop. In this case the oscillation needs to be set at  $1.3 V_{RMS}$  and the frequency needs to be kept as close to 20Hz as possible; in fact TR57 says it needs to be within 3Hz. The values shown on the schematic should do just that. The CA124 op amp can also be used in place of the CA324 if more precision is necessary. The resistor values should have a tolerance of 1% and the capacitors should be 5% ceramics.

#### **ARCOFI** Interface

Whether the ARCOFI is used or one of the many other brands of interface chips, the basic interface idea is the same. These types of chips generally include a microphone input, a speaker output (amplified), a CODEC, a number of programmable timers, multiple programmable gain stages. and analog filters. The internal CODEC needs to be programmed to the appropriate companding type for the area, and the gain stages should be set to transmit and receive a maximum of 2.5V<sub>PEAK</sub> without clipping. The microphone input is used in a balanced configuration to receive the outgoing transmission from the transhybrid balance circuit. The input is centered about 2.5V by using the internal VREF of the ARCOFI tied to the non inverting input of the external op amp. There is also a diode clamp that limits the output of the amp to between +5V and ground. This is necessary to protect the input of the ARCOFI and may or may not be needed, depending on the interface chip used. The HOP pin is used for the receive signal from the network to the SLIC. It is generally meant for a handset output, but the specs for its impedance and voltage capabilities more closely match the SLIC than any other output. The simplest implementation of the digital I/O interface uses the four programmable pins on the ARCOFI for control and monitoring of the SLIC.

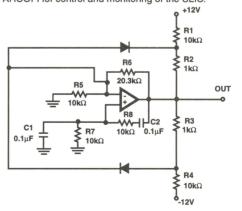


FIGURE 8. TYPICAL WEINBRIDGE OSCILLATOR

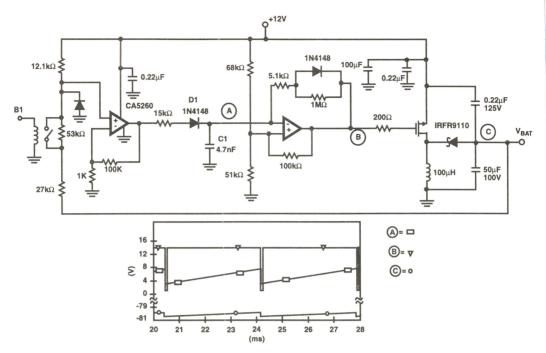


FIGURE 9. SIMPLE BOOST CONVERTER

#### Simple Boost Converter

The power needs for this type of circuit are new to computer cards. There will be no -80VDC supply available on the PCI or ISA bus so it needs to be generated locally. The first issue is safety - does the supply need to be isolated? Probably not, since the primary supply from which it draws its power is undoubtedly already isolated. Does it need overcurrent protection? Again, probably not since the SLIC itself provides short circuit protection. However, since requirements vary from system to system, two different power supplies will be shown that would adequately support the analog interface. The simple boost converter is shown in the schematic and has the advantages of being the smallest and cheapest. The object will be to derive -27 and -80VDC from the +12V supply with a reasonably high efficiency and with a minimum parts count.

The circuit basically consists of a dual op amp, a FET, an inductor, a rectifying diode, and some output capacitance (see Figure 9). The first amp on the left acts merely as an error amplifier. The resistors on its input form a voltage divider. The error amp tries to maintain a virtual ground on that pin so zero appears on that pin when the output voltage is correct. A 48K resistor would give -48V, an 80K resistor gives -80V, and a 27K resistor gives -27V. Obviously it will be quite simple to change the output voltage by simply switching in different resistances to the bottom of the divider. The only precaution is that the switch needs to withstand a full 80V of potential. A simple relay is the most straightforward method of switching. Note that a SPST relay can be used if it is put across the 53K

resistor. When open the total resistance is 53 + 27 = 80KW and when closed the total resistance is 27+(contact resistance) = ~27KW. This is cheaper than using a SPDT relay with a 27K and an 80K resistor attached. The gain around the error amp is about 100 to set the sensitivity and accuracy of the supply.

In any other application the next section to the right would be termed a peak detector, but upon further investigation the diode and cap interact with the following op amp to form a simple multivibrator. The basic circuit can be found in most college textbooks, but the basic function is fairly straightforward. The resistors on the non inverting input of the second amp form a resistor divider that sets the trip points of the "comparator". The trip points are skewed by the positive feedback to create some hysteresis. The basic triangle wave that the amp compares the trip points to is generated by the resistors in the negative feedback loop acting on C1. If the output is high, diode D1 is reverse biased and the total resistance between the 12V output and the cap C1 is a little more than 1MW. The cap will charge to the high trip point and cause the output of the amp to go low. This forward biases D1 and causes the total resistance between C1 and ground to be about 5.1K. This discharges the capacitor rather quickly. This alternating charge and discharge sets up the basic triangle wave that translates to a square wave at the output of the amp, that in turn drives the gate of a P channel FET. A low output corresponds to the 5.1K time constant and sets the on time of the FET. If the voltage detected by the error amplifier is too low, the off time is simply reduced by pre-charging C1 with the error amplifier. Waveforms for the circuit are also shown in Figure 9.

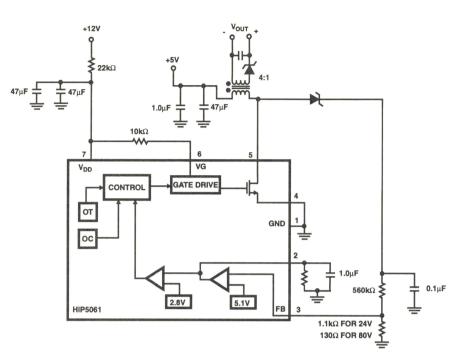


FIGURE 10. ALTERNATE ISOLATED CONVERTER

The rest of the circuit follows the well understood equations of an inverting boost converter. When the FET is on, the rectifying diode is reverse biased. The current in the inductor ramps up linearly at a rate di/dt = Vin/L. After the on time (governed by the time constant of 5.1K and 4.7nF) a total energy has been stored in the inductor of:

$$E = \frac{1}{2}(LI_{P}^{2})$$
 (EQ. 7)

where the peak current is given by:

$$I_{p} = \frac{V_{in}t_{on}}{I_{on}}$$
 (EQ. 8)

When the FET turns off, the inductor tries to maintain constant current so the voltage across it changes polarity and the peak current begins to flow through the rectifying diode and the output capacitor. This charges the cap up to a negative voltage. If all of the energy stored in the inductor is transferred to the output capacitor before the next turn on period, then the circuit is said to operate in discontinuous mode. This in fact is necessary for stability of the control loop. The total power delivered to the load is

$$P = \frac{1}{2} \frac{L(l_p^2)}{T}$$
 (EQ. 9)

$$V_o = V_{in} \left[ T_{on} \times \sqrt{\frac{R_o}{2T \times L}} \right]$$
 (EQ. 10)

T = total period

and of course  $P = V^2/R$  so the output voltage can be found from Equation 10:

Note that in this particular case the on time is held constant and the period is varied unlike a standard pulse width modulator where the opposite is true.

The output capacitor must be capable of sustaining the output current during an entire cycle of the FET without allowing excessive droop. Since the cap must support the entire output current for a majority of the time, a fairly large value is required.

#### **Alternate Isolated Boost Converter**

Since system requirements periodically dictate more stringently designed power supplies, an alternate power solution is also available. If isolation, overcurrent protection, or overtemperature protection are needed, a simple boost regulator with an output transformer can be used. The simplest and most cost effective solution that provides all these features can be found in the HIP5061 family of controllers. The HIP5061 (see Figure 10) contains all the necessary components on a monolithic die to perform all the necessary functions involved in controlling a boost regulator (oscillator, PWM, OT, OC, precision reference, and integrated FET). The only limitation of using the HIP5061 to implement the telecom supply is that the HIP5061 has a maximum voltage rating of 60V. The output transformer needs to be a step up so that the primary can run at a lower voltage that is within

the range the HIP5061 can handle. A 4:1 transformer provides a reasonable primary voltage.

In order to keep the cost down, primary side control will be used (otherwise another isolation boundary must be crossed by either another transformer or an optocoupler). The same basic method of setting the output voltage applies to this circuit except that the internal reference is 5.1V. So a 1.1K resistor on the bottom gives 24V and a  $130\Omega$  resistor gives 80V.

A small rectifier and output cap on the secondary side is all that is needed to provide sustained DC voltage. All protection functions are taken care of internal to the HIP5061 so only those parts shown are necessary. This implementation is slightly more expensive than the simple boost converter but if the extra features are needed it provides a simple topology.

#### **Battery Backup**

The local telephone operator provides a large battery bank at each central office to give emergency power to telephones during the event of a power loss Even if electric power to the home is lost, the telephone line keeps working (although cordless and powered phones will obviously die). This is necessary since 911 and emergency services often need to be accessed during power outages. The ISDN line, however. has no battery backup provided by the telephone company to power the ISDN modem. That power has to come from the computer slot. It might not be necessary to provide battery backup for ISDN unless it is the only communication line into the home. Most homes will have ISDN and a standard analog telephone to provide emergency access. If ISDN is the only line, there are two methods for battery backup. If the NT-1 is an independent unit and it has an analog port with an HC5517 SLIC installed, only the NT-1 needs battery backup. The rest of the devices on the S interface can go down, and the analog port on the NT-1 can still dial out. If the NT-1 is part of another card like a modem card, the entire computer with that card needs battery backup. These devices are very reasonably priced and will also prevent data loss in the event of a power failure. An uninterruptable power supply can be constructed fairly simply using Application Note 9611 "A DC-AC Isolated Inverter Using the HIP4082" with a few minor modifications. A gel cell battery provides a reliable long life energy source that can be continuously trickle charged.

#### **Options**

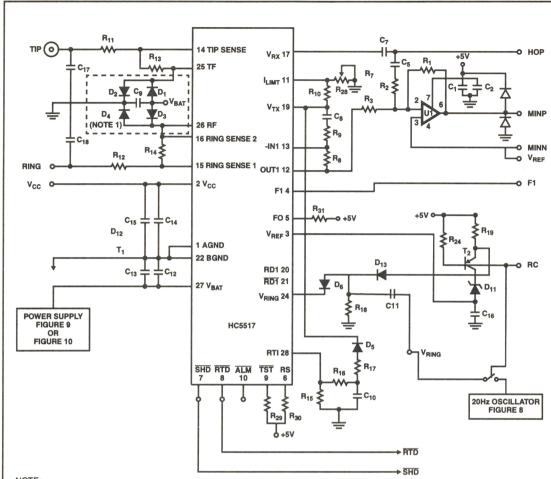
To simplify the design a number of things can be done.

For instance, it is not necessary to distinguish between switch hook detect and ring trip detect. These signals could be or'd together to create a detect output to the ISDN interface. All that needs to be known is whether the phone is off hook or on hook.

Depending on what voltage choices have been made, that off hook condition could be used to also control the power supply (for instance if we choose to have 80V supplied to the SLIC in both ringing and standby modes and 27V supplied only during active or off hook periods).

The F1 (Power denial pin) could be controlled by an unused state of RC and B1 such as RC high and B1 indicating 27V. There would never be an instance when a ring is commanded with only 27V applied to the SLIC. This could signal a power denial state with simple logic and shut the SLIC down.

Using shortcuts like these could allow control of the SLIC with one digital input for switch hook detection and two outputs for RC and F1 (or RC and PS). This is only necessary if the number of I/O lines are limited since the most versatility can be obtained by having all five control lines active.



NOTE:

1. Diode bridge optional for in-house use.

FIGURE 11. APPLICATION CIRCUIT

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
SLIC	HC5517	n/a	N/A	C <sub>2,</sub> C <sub>15</sub>	0.1μF	20%	50V
R <sub>1</sub> , R <sub>2</sub>	24.9kΩ	1%	1/4 Watt	C <sub>5,</sub> C <sub>7</sub>	10μF	20%	20V
R <sub>3</sub>	8.25kΩ	1%	1/4 Watt	C <sub>8</sub>	0.47μF	20%	20V
R <sub>8,</sub> R <sub>9</sub>	40kΩ	1%	1/4 Watt	C <sub>9,</sub> C <sub>12</sub>	0.01μF	20%	100V
R <sub>10</sub>	100kΩ	5%	1/4 Watt	C <sub>10</sub>	1.0μF	20%	50 V
R <sub>11-14</sub>	50Ω	1%	1/4 Watt	C <sub>11</sub>	100μF	20%	5V
R <sub>R15</sub>	47kΩ	1%	1/4 Watt	C <sub>13</sub>	0.1μF	20%	100V
R <sub>16</sub>	1.5ΜΩ	1%	1/4 Watt	C <sub>16</sub>	0.5μF	20%	50V
R <sub>17</sub>	56.2kΩ	1%	1/4 Watt	C <sub>17,</sub> C <sub>18</sub>	3300pF	20%	100V
R <sub>18</sub>	1.1kΩ	1%	1/4 Watt	D <sub>1-4</sub>	1N4007	-	100V, 1A
R <sub>19</sub>	825Ω	1%	1/4 Watt	D <sub>5,</sub> D <sub>6,</sub> D <sub>13</sub>	1N914	-	100V, 1A
R <sub>29,</sub> R <sub>30,</sub> R <sub>31</sub>	10kΩ	5%	1/4 Watt	D <sub>11</sub>	1N5255	-	28V, 1/2W
R <sub>24</sub>	47kΩ	5%	1/4 Watt	T <sub>2</sub>	2N2907	-	60V,150mA
R <sub>25-27</sub>	560Ω	5%	1/4 Watt	F1, RC, Battery	SPDT	Toggle switches, center off.	
R <sub>28</sub>	20kΩ P	otentiometer	1/4 Watt	U1	CA741C Op Amp		
C <sub>1,</sub> C <sub>14</sub>	0.01μF	20%	50V	Textool Socket	228-5523		

# MAPPOTE

No. AN9640.1 December 1996

# Harris Communications

Broadcasting Satellite Service

Carrier-To-Interference Ratio

Basic Trading Area

German C System

# **Glossary of Communication Terms**

Authors: Mark Amarandos and Don LaFontaine

BSS +

**BTA** 

C/I

C-NETz

# Introduction

The following glossary of communication terms is provided as a quick reference to aid understanding of technical communication literature. The list is a collection of terms that the authors encountered in their work and is in no way a complete list. The Glossary of terms is preceded by a list of Acronyms, some of which are included in the Glossary.

# **Acronyms**

AAL	ATM Adaption Layer
ACS	Advanced Cellular System
ACI +	Adjacent Channel Interference
ADSL	Asymmetrical Digital Subscriber Line
	Automatic Gain Control
AGC +	
ALT	Alternate Local Transport Company
AM †	Amplitude Modulation
AMI	Alternate Mark Inversion
AMPS	Advanced Mobile Phone Service
AMTA	American Mobile Telecommunications
	Association
ANSI	American National Standard Institute
AP (CO)	Applications Processor
APC	American Personal Communications
ARPANET	Advanced Research Project Agency
	Network
ART †	Amplitude Radio Transmission
ARQ	Automatic Repeat Request
ASCII	American Standard Code For Information
	Interchange
ASIC	Application Specific Integrated Circuit
ASP	Average Selling Price
ATG †	Air-To-Ground
ATM †	Asynchronous Transfer Mode
AWG	American Wire Gauge
AWGN †	Additive White Gaussian Noise
B-ISDN +	Broadband ISDN
BBS +	Bulletin Board System
BCC	Block Check Character
BELLCORE	Bell Communications Research
BER	Bit Error Rate
BFSK	Binary Frequency-Shift Keying
BPDU †	Burst Protocol Data Unit
BPF †	Band Pass Filter
BISYNC	Binary Synchronous Communications
BOC †	Bell Operating Company
BPS †	Bits Per Second
BPSK	Binary Phase-Shift Keying
DDI	Deels Detectations

Basic Rate Interface

C/I	Carrier- i o-interierence Hatto
CAD †	Computer Aided Design
CAGR	Compound Annual Growth Rate
CAI	Common Air Interface
CAM †	Computer Aided Manufacturing
CAP	Competitive Access Provider
CAP (HDSL)	Carrier-less AM/PM
CBEMA †	Computer And Business Equipment
	Manufacturers Association
CC	Cluster Controller
CC (#)	Country Code
CCA †	Clear Channel Assessment
CCIR †	Consultative Committee On International
	Radio
CCITT	Consultative Committee On International
	Telephone And Telegraph
CCS	Common Channel Signaling
CDMA	Code Division Multiple Access
CDPD	Cellular Digital Packet Data
CELP	Code-Excited Linear Predictive Coding
CEPT	Conference Of European Postal And
	Telecom Administration
CGSA	Cellular Geographic Service Area
CIC	Cascaded Integrator Comb
CMIP	Common Management Information Protocol
CMOS	Complementary Metal Oxide Semiconductor
CO	Central Office
CO switch †	Central Office Switch
COAX	Coaxial Cable
CODEC †	Coder/Decoder
CPE	Customer Premises Equipment
CPFSK †	Constant Phase Frequency Shift Keying
CPS	Characters Per Second
CRC	Cyclic Redundancy Check
CS †	Carrier Sense
CSA	Canadian Standards Association
CSDN	Circuit Switched Digital Network
CSMA/CA	Carrier Sense Multiple Access/Collision
	Avoidance

Carrier Sense Multiple Access With

Cordless Telephone - First Generation

Cordless Telephone - Third Generation

Cordless Telephone - Second Generation

Collision Detection

Channel Service Unit

Cordless Telephone

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BRI

CSMA/CD

CSU

CT

CT1

CT2

CT3

CTIA	Callular Talacammunications Industry	EDDI	Fiber Data Distributed Interface
CTIA	Cellular Telecommunications Industry	FDDI	Fiber Data Distributed Interface
CVPC	Association	FDM	Frequency Division Multiplexing
CVBS †	Composite Video Blanking Synchronization	FDMA	Frequency Division Multiple Access
DAB	Digital Audio Broadcasting	FDX	Full Duplex
DACS	Digital Access And Cross-Connect System	FEC	Forward Error Correction
DAN	Desk Area Network	FEP	Front End Processor
DARPA	Defense Advanced Research Projects	FER †	Frame Error Rate
	Agency	FFS FH	For Further Study Frequency Hopping
dB	Decibel	FHSS	
dBm	Decibel Referencing 1 Milliwatt		Frequency Hopping Spread Spectrum First-In, First-Out Memory
DBPSK †	Differential Binary Phase Shift Key	FIFO memory FM	Frequency Modulation
DBS	Direct Broadcast From Satellite	FPLMTS	Future Public Land Mobile Telecommuni-
DCE	Data Circuit Terminating Equipment	FPLWIS	cations System
DCS †	Digital Cellular Systems	FSK †	Frequency-Shift Keying
DCT 900	Ericsson's Digital Cordless Telephone At	FT1	Fractional T1
	900MHz	FTTC †	Fiber To The Curb
DCT †	Digital Cordless Telephone	-	
DDC †	Digital Down Converter	GAP	Ground-To-Air Paging
DDD	Direct Distance Dial Network	Gb/s	Gigabits Per Second
DDS	Digital Dataphone Service	GCI	General Communication Interface
DECT	Digital European Cordless Telephone	GFSK	Gaussian Frequency-Shift Keying
DEMUX	Demultiplexing	GP †	Processing Gain
DIP †	Dual-In-Line Package	GSM	Global System For Mobile Communications
DNL †	Differential Non Linearity	GSO	Geostationary Satellite Orbit
DOC	Dept. Of Communications	HDLC	High-Level Data Link Control
DPI	Dots Per Inch	HDSL	High Bit-Rate Digital Subscriber Line
DPSK †	Differential Phase Shift Keying	HDX †	Half-Duplex
DPN	Digital Packet Network	HPF †	High Pass Filter
DQPSK †	Differential Quadrature Phase Shift Key	HSSI †	High Speed Serial Interface
DQT †	Digital Quadrature Tuner	HW †	Hardware
DS	Direct Sequence	Hz	Cycles Per Second
DSSS †	Direct Sequence Spread Spectrum	IEC	Interchange Carrier
DS0	Digital Signal, Level 0	IEEE	Institute Of Electrical And Electronics
DS1	Digital Signal, Level 1		Engineers
DS2	Digital Signal, Level 2	IF †	Intermediate Frequency
DS3	Digital Signal, Level 3	IIP3 †	Input Third Order Intercept Point
DSI †	Digital Speech Interpolation	IMASS	Intelligent Multiple Access Spectrum Sharing
DSL DSP	Digital Subscriber Line	IMD †	Inter-Modulation Distortion
	Digital Signal Processor	IMTS	Improved Mobile Telephone Service
DSU	Digital Service Unit	IN	Intelligent Network
DSX †	Digital Signal Cross-Counter	INL †	Integral Non-Linearity
DTE DTMF	Data Terminal Equipment	INMARSAT	The International Maritime Satellite
-	Dual Tone Multi-Frequency		Organization
E-mail	Electronic Mail	INTELSAT	International Telecommunications
E-TDMA	Enhanced TDMA		Satellite Organization
E.164	Numbering Plan For The ISDN ERA	IP3 †	Third Order Intercept Point
EAMPS	Expanded Amps	IRAC	Interagency Radio Advisory Committee
EBCDIC	Extended Binary Coded Decimal	IS-54	EIA/TIA Interim Standard-54
FOMA	Interchange Code	ISDN	Integrated Services Digital Network
ECMA †	European Computer Manufacturers	ISI	Intersymbol Interference
F004	Association	ISM BAND	Industrial Scientific and Medical band
ECSA †	Exchange Carrier Standards Association	ISO	International Organization For
ED †	Energy Detection		Standardization
EDSL	Extended Digital Subscriber Line	ITU	International Telecommunications Union
EIA †	Electronic Industries Association Effective Number Of Bits	Jм ÷	Jamming Margin
ENOB †		JPEG †	Joint Photographic Experts Group
ET	Enhanced Specialized Mobile Radio Exchange Termination	J-TACS	Japanese TACS
ETACS †	Extended TACS	Kbps	Kilobits Per Second
ETSI †	European Telecommunications Standards	kHz	Thousands Of Cycles Per Second
EISIT	Institute	km	Kilometer
Euro ISDN	Eurofile Transfer Standard For ISDN	ksps †	Kilo Samples Per Second
FITL		LAN	Local Area Network
	Fiber In The Loop	LAPB	Link Access Procedure Balanced
FAX	Facsimile	LAPB	Link Access Procedure Balanced Link Access Procedure D
FCC	Federal Communications Commission	LAPM	Link Access Procedure D  Link Access Procedure For Modems
FCS	Frame Check Sequence	-AF IN	LIIN ACCESS I TOCEUME FOI MOUEINS

LATA	Local Access Transport Area	NTT	The Japanese Nippon Telephone And
		MIII	
LCM	Line Concentrating Module	•	Telegraph Cellular System
LEC	Local Exchange Carrier	OA&M †	Operations, Administration And Maintenance
LEO	Low-Earth Orbit	OAM&P	Operations, Administration, Management
LME †	Layer Management Entity		And Provisioning
LNA †	Low Noise Amplifier	OC-n	Optical Carrier At Level N
LNB +	Low Noise Block	OOK †	Optical Carrier At Level N
LO †	Local Oscillator	ONA †	
LPC	Linear Predictive Coding		Open Network Architecture
LPF †	Low Pass Filter	OP1db †	Output 1dB Compression Point
LSB	Least Significant Bit	OQPSK †	Offset Quadrature Phase Shift Keying
		OSI	Open System Interconnection Reference
LT	Line Termination		Model
M13	Multiplexer DS1 To DS3	PAD	Packet Assembler/Disassembler
MAC	Media Access Control	PAL †	Phase Alternate Line
MAU	Media Access Unit And Multi-Station	PBX	
	Access Unit		Private Branch Exchange
Mbps.	Megabits Per Second	PC	Personal Computer
		PCM	Pulse Code Modulation
Mbits	Megabits	PCMCIA	Personal Computer Memory Card
MDS	Minimum Discernible Signal		International Association
MEO	Mid-Earth Orbit	PCN	Personal Communications Network
MF	Multi-Frequency	PCS	Personal Communications Service
MFJ	Modified Final Judgment		(System)
MFLOPS	Millions Of Floating Point Instructions Per	PDA †	Personal Digital Assistant
	Second	PDMA	
MIB +	Management Information Base		Phase Division Multiple Access
MIPS	Millions Of Instructions Per Second	PDN	Public Data Network
MIRS	Motorola Integrated Radio Systems	PDS	Premises Distribution System
		PDU †	Protocol Data Unit
MNP	Micron Network Protocol	PGA †	Pin Grid Array (Package)
MPDU †	MAC Protocol Data Unit	PHS	Personal Handyphone System
MPEG †	Motion Picture Experts Group	PHY †	Physical Layer (Radio)
MPT	Ministry Of Posts And Telecommunications	PHY DATA.REQ	†MAC Requests To Sent Data To PHY
MQFP †	Metric Quad Flat Pack (Packages)	PHY_SAP +	Physical Layer Service Access Point
MSA	Metropolitan Statistical Area	PL	Private Line
MSB	Most Significant Bit	PLCP †	Physical Layer Convergence Protocol
MSC	Mobile Services Switching Center		
msec	Milisecond	PLL	Phase Locked Loop
MSPS +	Mega Samples Per Second	PLME †	PHY Layer Management Entity
		PLMR	Private Land Mobile Radio
MSS	Mobile Satellite Service	PMD †	Physical Medium Dependent
MSK †	Minimum Shift Keying	PMD_ANTSEL †	MD Antenna Select
MTA	Major Trading Area	PMD_FREQ †	PMD Channel Frequency
MTSO	Mobile Telephone Switching Office	PMD_RATE †	PMD Data Rate
MTX	Mobile Telephone Exchange	PMD_SAP +	Physical Medium Dependent Service
MUX	Multiplexer		Access Point
N-ISDN	Narrowband ISDN	PMR	Public Mobile Radio
N-TACS	Narrowband TACS	PN	
			Pseudo-random Noise
NAMPS	Narrowband Advanced Mobile Phone	PN CODE †	Pseudo-random Noise Code
	Service	POP	Point Of Presence
NANP	North American Numbering Plan	POS †	Point Of Sale
NCO †	Numerically Controlled Oscillator	POTS †	Plain Old Telephone Service
NCOM †	Numerically Controlled Oscillator Modulator	PPDU †	PHY Protocol Data Unit
NFS	Network File System	PPM †	Pulse Position Modulation
NIC	Network Interface Card/Controller	PRA	Primary Rate Access
NMT +	Nordic Mobile Telephone	PRI	Primary Rate Interface
NMT450	Nordic Mobile Telephone at 450MHz	PSK †	Phase-Shift Keying
NMT900	Nordic Mobile Telephone at 900MHz	PSTN	Public Switched Telephone Network
NNI	Network Node Interface And Network-To-	PTN	Personal Telephone Number
14141	Network Interface	PTT	Postal Telephone and Telegraph
NDA			
NPA	Numbering Plan Area	Q †	Quadrature
NPRM	Notice Of Proposed Rulemaking (By FCC)	QAM	Quadrature Amplitude Modulation
NT	Network Termination	QFSK †	Quadrature Frequency Shift Keying
NT2 †	Network Termination 2	RAM	Random Access Memory
NTACS	Nippon TACS	RBOC	
NTIA	National Telecommunications And Infor-		Regional Bell Operating Company
	mation Administration	RCC	Radio Common Carrier
NTSC	National Television Standards Committee	RDSS	Radio Determination Satellite Service
		RELP	Residual-Excited Linear Predictive Coding
		RF †	Radio Frequency

RISC Reduced Instruction Set Computing
The Italian Cellular System

RRC † Root Raised Cosine RSA Rural Service Area

RSSI † Receive Signal Strength Indicator RTMS † Radio Telephone Mobile System

RTU Right-To-Use

SAMTS † South American Mobile Telephone Service

SAP † Service Access Point

SAPI Service Access Point Identifier
SAR Segmentation And Reassembly
SAW + Surface Acoustic Wave

SDH Synchronous Digital Hierarchy
SDL Specification Description Language
SDLC Synchronous Data Link Control
SDN Software Defined Network

SDN Software Defined Network
SECAM † Sequential Color And Memory
SFD Start Frame Delimiter
Spurious Free Dynamic Range

SIM Subscriber Identification Module
SLC Subscriber Loop Carrier
SLIC Subscriber Line Interface Circuit
SMDS Switched Multi-Megabit Data Service

SMR Specialized Mobile Radio
SNA Systems Network Architecture
SNR Signal To Noise Ratio

SNR Signal To Noise Ratio
SOIC † Small Outline Integrated Circuit
SONET Synchronous Optical Network
SQ + Signal Quality (PN code correlation

strenath)

SS Spread Spectrum

SSOP + Shrink Small Outline Package STP (SS7) Signal Transfer Point

STP (WIRE) Shielded Twisted Pair STS-n Synchronous Transport Signal At Level n

SW † Software
T CARRIER T-MUX Software
T1 Carrier
T1 Multiplexer

T1 (ANSI) Telephony Committee
T1C T1 Carrier C

T1X1 † T1 Committee Of The Exchange Carriers

Standards Association Technical Advisory Terminal Adapter

TA (ISDN)
Terminal Adapter
Total Access Cellular System
TAM †
Total Available Market

TCM Time Compression Multiplexing
TCP/IP Transmission Control Protocol/Internet

Protocol

TDM Time Division Multiplex
TDMA Time Division Multiple Access
TE Terminal Equipment
TE1 Terminal Equipment Type 1
TE2 Terminal Equipment Type 2

TIA Telecommunications Industry Association

TQFP † Thin Quad Flat Pack
TR Technical Requirement

TTC † Telecommunications Technology Committee

TXE + Transmit Enable

UDI Unrestricted Digital Information
UMTS Universal Mobile Telecommunications

Service User Network Interface

UPS Uninteruptable Power Supply
UPT Universal Personal Telecommunications

UTP + Unshielded Twisted Pair

VCO † User-To-User Information
User-To-User Information
Voltage Controlled Oscillator

VDSL Very-High-Bit-Rate Digital Subscriber Line

VIRTUAL POP Virtual Point Of Presence
VOD + Video On Demand
VPN Virtual Private Network

VSCS † Voice Switching And Control System
VSELP Vector-Sum Excited Linear Predictive

Coding

WARC World Administrative Radio Conference

WDM Wavelength Division Multiplexing
WLAN + Wireless Local Area Network

WLL Wireless Local Loop

WPBX † Wireless Private Branch Exchange

# Glossary

# **1BASE-5 ETHERNET**

A version of Ethernet that operates a 1 megabit per second over twisted-pair wire. Also know as StarLAN. 1BASE-5 Ethernet has been superseded by 10BASE-T.

# 2 BINARY, 1 QUATERNARY (2B1Q)

A pulse amplitude modulation scheme used to send highspeed digital signals over ordinary telephone wires in ISDN and HDSL services. The scheme uses four voltage levels, and each level represents a dibit (group of two bits).

# 2B+D

The Basic Rate Interface ISDN service that provides two 64 kilobit per second circuit switched B (bearer) data channels and one 16 kilobit per second D (data) channel for signaling and low speed packetized data.

#### 30B+D

The European ISDN Primary Rate Interface that provides 30 circuit switched 64 kilobit per second B (bearer) channels and one 64 kilobit per second D (data) channel for signaling and packet switched data.

# 4 BINARY 3 TERNARY (4B3T)

A line code in which 4 binary bits are converted into three ternary symbols for transmission across the ISDN U interface.

#### 4ESS

AT&T toll/tandem digital switch. The first digital switch (1976) introduced in the North American market. Makes up the bulk of the AT&T long distance network.

# 5ESS

AT&T medium to large-size digital end office (class 5) switch introduced in 1981.

UNI

TA (BC)

# 10BASE-2 ETHERNET

A version of Ethernet that uses thin coaxial cable and operates at 10 megabits per second with a maximum cable length of 185 meters also called Cheapernet or Thinwire Ethernet.

#### 10BASE-5 ETHERNET

A version of Ethernet that operates at 10 megabits per second and uses thick coaxial cable with a maximum network length of 500 meters.

# **10BASE-T ETHERNET**

A version of Ethernet that operates over twisted-pair wire at a speed of 10 megabits per second. 10BASE-T networks must use an Ethernet hub and a star topology.

#### μ-LAW

A North American standard for the nonlinear digitization of voice.

#### A-LAW

A European standard for the nonlinear digitization of voice signals.

# AAL (ATM Adaption Layer)

ATM formats that specify constant or variable bit rate and connection oriented or connection-less mode

# **ACCESS PROTOCOL**

A defined set of procedures that is adopted at an interface at a specified reference point between a user and a network to enable the user to employ services of that network.

# ACS (ADVANCED CELLULAR SYSTEM)

A Swedish cellular system, operating at 400MHz or 800MHz, introduced in 1983 in Sweden, and later into Hong Kong.

# **ADDRESS**

A designator that defines the identification of a terminal, peripheral device, or any other node on a network.

# ADSL (ASYMMETRICAL DIGITAL SUBSCRIBER LINE)

A technology to provide high speed, one way digital information to subscribers at up to 6 megabits per second over existing local loops. There would also be a low speed reverse channel from the subscriber to the service provider.

# **ALGORITHM**

A prescribed set of well defined rules or processes for finding the solution to a problem.

# **ALT (ALTERNATE LOCAL TRANSPORT COMPANY)**

Local exchange competitor such as Metropolitan Fiber Systems (MFS) or Teleport. Currently targeted to large customers operating in metropolitan areas.

# **ALTERNATE MARK INVERSION**

A line code that uses 0 volts to represent 1s and alternate positive and negative voltage levels to represent 0s.

# **ALTERNATE ROUTE**

A secondary communication path between two terminals that is used when the primary route is unavailable.

# **AMPLIFIER**

**Application Note 9640** 

An electronic circuit that detects weak analog signals and makes them stronger (amplifies them). An amplifier amplifies noise as well as the desired signal.

# AMPS (ADVANCED MOBILE PHONE SERVICE)

The predominant cellular system in North and South America and elsewhere (in more than 35 countries) at 800MHz. Analog Cellular FDMA System with 30kHz channels.

# AMTA (AMERICAN MOBILE TELECOMMUNICATIONS ASSOCIATION)

The industry trade organization representing Specialized Mobile Radio (SMR) operators.

#### **ANALOG SIGNAL**

Continuously varying with an amplitude which is an analog of the original information, and thus may have virtually an infinite numbers of states. Contrasted with a digital signal which has only a very limited number of discrete states.

# **ANALOG TRANSMISSION**

Repeats where necessary by mere amplification without recovering information. Thus noise is cumulative in an analog transmission system.

# ANSI (AMERICAN NATIONAL STANDARDS INSTITUTE)

A voluntary U.S. industry association to develop standards without undue influence from any one company.

#### **ANSWER BACK**

A signal from a receiving terminal in response to transmitting terminal's request. The answer back indicates that the receiving terminal is ready to receive data or has successfully received them.

#### **ANSWER MODEM**

The modem that does not originate communication in a full duplex communication system.

# AP(CO) (APPLICATIONS PROCESSOR)

Non-real-time adjunct computer for the AT&T 5ESS. Provides advanced features such as Electronic Directory, Facilities Management, and Message Desk.

# APC (AMERICAN PERSONAL COMMUNICATIONS)

A corporation developing "Telepoint" and PCS capabilities in the U.S.

# APPLICATION LAYER

OSI Reference model top layer - the end user layer.

# **ARCHITECTURE**

An overall plan that represents the goal towards which its implementors strive. Architecture is used to describe data communications system, integrated circuit layouts, operating systems and other complex hardware and/or software structures. See communications architecture.

# ARPANET (ADVANCED RESEARCH PROJECT AGENCY NETWORK)

U.S. Department of Defense network to link university and government research centers. Service began in 1969 based on connectionless "Datagram." Has evolved as an Ad Hoc "Standard."

# ARQ (AUTOMATIC REPEAT REQUEST)

A general term for error control protocols featuring hardware detection and retransmission of defective data. This term is used primarily by US Robotics.

# ASCII (AMERICAN STANDARD CODE FOR INFORMA-TION INTERCHANGE)

A 7-bit code that is widely used in data communications, especially for the communication text.

# ASIC (APPLICATION SPECIFIC INTEGRATED CIRCUIT)

Integrated Circuits (ICs) customized to perform a specific task - as opposed to general purpose microprocessors or DSPs.

#### ASP

Abbreviation for Average Selling Price.

# **ASRO**

Motorola's new digital Public Land Mobile Radio (PLMR) for evolution from analog FM. Band independent, FDMA using VSELP and splitting current 25kHz channels into two 12.5kHz channels.

This is one of four candidates for national standardization by APCO (Associated Public-Safety Communications Officers) which oversees public safety frequencies.

# **ASYNCHRONOUS COMMUNICATIONS**

A form of communication that uses a start bit at the beginning of each data word and a stop bit a the end of each data word.

# **ASYNCHRONOUS TRANSMISSION**

Data is sent character by character. The receiver and transmitter are synchronized for each individual character via a start and stop pulse. Asynchronous transmission is normally found on dial up circuits, usually at speeds between 300 and 28,800 bps.

# AT COMMAND SET

A defacto set of standard commands used to control the operation of intelligent modems. Also called the Hayes Command Set.

# **ATM FORUM**

An organization made up of hundreds of companies whose purpose is to promote cooperation among its members in developing ATM standards and the ATM market.

# ATM PIPE SWITCH

An ATM technology developed and marketed by L.M. Ericsson.

#### **ATTENUATION**

Signal loss in a communications circuit or equipment.

#### **AUDIO FREQUENCIES**

Frequencies that can be heard by the human ear, typically 30Hz to 20kHz.

# **AUTO ANSWER**

The modem feature which enables detection of a ring and answering without assistance from a program.

# AWG (American Wire Gauge)

A wire size standard.

# **B-CHANNEL**

A 64kb/s (DS0) ISDN user-to-network channel. Used in both the Basic Interface and the Primary Rate Interface. Carries a voice, data or image call, but not the signaling for the call. Normally circuit-switched by the network, but can be packet-switched, or even semi-permanently connected. When circuit switched, may carry multiplexed information streams, but only to the same destination.

#### **BACKBONE NETWORK**

A network that links several smaller networks.

# **BALANCING NETWORK**

Another name for hybrid, a circuit that connects a twowire line to a four wire line and maximizes power transfer while minimizing echo.

# **BANDWIDTH**

- 1) In analog signals, the difference between a signals lowest frequency component and its highest signal component as measured in Hertz (Hz).
- 2) The speed of a digital communications circuit in bits per second.

# **BASEBAND SIGNAL**

A signal that is not modulated onto a carrier. In a cellular telephone, all of the analog and digital signals except the radio frequency portion of the telephone.

# **BASE STATION**

A radio transceiver that is located near the center of each cell in a cellular telephone network and which communicates with all of the active cellular telephones in the cell and provides them with a connection to the switched telephone network.

# **BAUD**

Number of times (per second) the signal can change.

# **BCC** (Block Check Character)

An extra data word added to the end of data transmission to aid in error detection. Also called binary check character.

# BEARER CAPABILITY

Information carrying capability requested by the user and provided by the network. For example, bearer capability of voice with possible echo-suppression and loss-insertion is different than bearer capability of digital information where the bits are carried transparently.

#### BEARER SERVICES

Basic communications services including, but not limited to, voice circuits, 64 kilobit per second switched data circuits, T1 lines in North America and E1 lines in Europe.

#### **BELL 103**

A 300b/s full duplex FSK modern standard. The international version is V.21.

#### **BELL 202**

A half-duplex FSK modem standard that operates at 1200 b/s over dial up telephone lines and 1800b/s over leased conditioned lines.

#### **BELL 212A**

A full duplex 4PSK modem standard that operates at 1200b/s and 600 baud. The international version is V.22.

#### **BELLCORE** (BELL COMMUNICATIONS RESEARCH)

Research and Development organization owned by the seven Regional Bell Operating Companies.

# **BER (BIT ERROR RATE)**

A measure of transmission quality. Generally shown as a negative exponent. Example:

 $10^{-7}$  means 1 out of  $10^{7}$  bits are in error or 1 out of 10,000,000 bits are in error or .0000001 error/bit.

# **BFSK** (BINARY FREQUENCY-SHIFT KEYING)

A modulation technique in which a digital signal shifts the frequency of an analog carrier between two distinct frequencies. BFSK is usually limited to low data communications speeds.

# **BISYNC (BINARY SYNCHRONOUS COMMUNICATIONS)**

An old (pre-SNA) IBM character-oriented, half-duplex protocol.

# BIT

Binary character consisting of one of two possible values, 0 or 1.

# **BIT ORIENTED PROTOCOL**

A set of rules for communicating data that divides each block of data into bit fields. Each bit field serves a purpose in the protocol.

#### **BIT STREAM**

A continuous series of bits transmitted over a communications link.

#### **BLUE BOOKS**

CCITT recommendations published in 1988.

# BPSK (BINARY PHASE-SHIFT KEYING)

A modulation scheme that uses two phases to represent data. One phase represents a mark, and the other phase represents a space.

# **BRI** (BASIC RATE INTERFACE)

An ISDN User-to-Network Interface consisting of three full-duplex channels; two 64Kb/s B Channels and one 16 Kb/s D Channel (2B&D). the 2B+D U interface requires two twisted pairs of wire.

#### BRIDGE

A device that operates at OSM Model levels 1 and 2 to connect two or more LANs of the same type.

# BROADBAND

A communications channel that has a bandwidth greater than 64 kilobits per second and that can provide higher speed data communications than a standard telephone circuit. Also called wide band.

# **BROADCAST**

A service with one transmitter and many receivers, where all receivers connected to the network receive the message, often by use of a broadcast address. (Compare to Multicast, where a subset of the receivers are addressed.

#### BROUTER

A device that performs the functions of both a bridge and a router (X.25 network product).

# **BTA (BASIC TRADING AREA)**

To identify areas of economic integration, Rand McNally (1-800-284-6565) in their \$395 Commercial Atlas and Marketing Guide," has divided the country into 487 Basic Trading Areas (BTAs). A BTA consists of a number of counties; counties are never split between BTAs. For example, the Chicago BTA consists of 14 counties including Kenosha County in Wisconsin and 4 counties in Indiana. Each BTA belongs to a Major Trading Area (MTA). For instance, the Chicago BTA along with 17 other BTAs make up the Chicago MTA.

# **BUILT-IN MODEM**

A modem integrated into the motherboard of a terminal or computer.

#### **BURST**

Several events occurring within a short period of time.

#### **BURST ERROR**

A series of consecutive errors in data transmissions.

# **BURSTY**

A characteristic of data communications network. It refers to the fact that the bandwidth needed for data communications tends to vary greatly from one moment to the next as data is sent in bursts.

# **BUS NETWORK**

A network topology that uses a single communications link to connect three or more terminals. Also called a multi-drop network.

# **BYTE**

A group of eight bits that is processed as a single logical unit.

# C-450

An analog cellular telephone standard used in Germany and Portugal.

# C-NETz (GERMAN C SYSTEM)

The German C system is a digital cellular system at 450MHz, introduced prior to 1989, having 237 channels.

# C/I (CARRIER-TO-INTERFERENCE RATIO)

The ratio of the desired signal strength to the combined interference from all other mobiles or portables (usually dominated by the co-channel interferers; i.e., those using the SAME frequency in other cells.)

# **CAGR** (Compound Annual Growth Rate)

Abbreviation for compound annual growth rate. The average yearly growth in a market over a period of several years.

# CAI (Common Air Interface)

A standard radio and protocol definition which ensures interoperability of mobile and portable radios from one vendor with bas stations to another vendor.

# **CALL-SETUP TIME**

The time required to establish a connection between two terminals over a communications network.

# CAP (COMPETITIVE ACCESS PROVIDER)

Local exchange competitor such as Metropolitan Fiber Systems (MFS) or Digiport. Currently targeted to large customers operating in metropolitan areas.

# CAP (HDSL) (Carrierless AM/PM)

A method of transmitting information using two signal phases (Phase Modulation [PM]) and multiple amplitude levels (AM) to represent groups of 2 or more bits.

# CARRIER

A continuous frequency capable of being either modulated or impressed with another information carrying signal. Carriers are generated and maintained by modems via the transmission lines of the telephones companies.

#### **CARRIER SYSTEM**

A method of obtaining several communications channels over a single communications link by multiplexing the channels together at the transmitting end and demultiplexing them at the receiving end.

# **CC** (CLUSTER CONTROLLER)

BM models 3174/3274, etc. Control Unit serving multiple IBM 3178/3278 and other terminals. The name is derived from the fact that terminals are "clustered" around this. The connection from the 3278 terminal to the 3274 controller is known as COAX Type A, which operates at 2.3 Mb/s.

Cluster controllers are either local or remote. Local cluster controllers are located with 225 feet of the IBM host computer and are connected via the IBM channel protocol operating at 16MB/s (2 megabytes per second). Remote cluster controllers are connected via a 9.6 or 56k/bs dedicated connection using the old bisync or the newer SNA protocol. On the average, eight cluster controllers share a single (multidrop) communications line.

# CC(#) (COUNTRY CODE)

Part of a (telephone) number. The I.463 country code for North America is 1.

# CCITT (CONSULTATIVE COMMITTEE ON INTERNA-TIONAL TELEPHONE AND TELEGRAPH)

International committee under the auspices of the International Telecommunications Union and in turn, the U.N. The CCITT develops "Recommendation" associated with all aspects of international telecommunications and public data network implementations. Organized by topics into Study Groups which publish on a four year cycle in colored books (e.g. Red, Blue). Books are subdivided into fascicles for publications. Fascicles contain recommendations which are referenced as LETTER.NUMBER (e.g., X.25, V.35, Q.931).

Participants come from National Administrations, Public Network Providers and Equipment Vendors. All U.S. participation is coordinated through the State Department.

# **CCS** (COMMON CHANNEL SIGNALING)

A method of using a single signal channel to carry signaling information relating to a number of information channels. The signaling information is sent in packet form. See Signaling System 7 (SS7). Contrast with in-band signaling.

# CDMA (CODE DIVISION MULTIPLE ACCESS)

A "spread spectrum" method of allowing multiple users to share the radio frequency spectrum by assigning each active user an individual "code".

# CDPD (CELLULAR DIGITAL PACKET DATA)

A piggyback system for sending and receiving digital data on the existing AMPS system. For use with laptop computers.

# CELL

An ATM packet that is 53 bytes in length with a 5 byte header and a 48 byte payload.

#### **CELP** (CODE-EXCITED LINEAR PREDICTIVE CODING)

A general class of enhancements to Linear Predictive Coders using a combination of a limited number of excitations from a "code book."

# **CENTRAL OFFICE SWITCH**

A system located in a telephone company office that completes dialed up telephone connections.

# **CENTREX**

Service created by software in telephone company local office which simulates multiple virtual PBXs.

# CEPT (CONFERENCE OF EUROPEAN POSTAL AND TELECOMM, ADMINISTRATION)

A European telecommunications standard committee.

# CEPT1 (E1)

2.048Mb/s European rate. This is the rate used by European CEPT carrier to transmit 30 64Kb/s digital channels for voice or data calls, plus a 64Kb/s channel for signaling (Time Slot 16) and a 64Kb/s channel for framing and maintenance (Time Slot 0).

# CEPT3 (E3)

34.368Mb/s European rate. Consists of 16 CEPT1s plus overhead.

# CEPT4

139.264Mb/s European rate.

# CGSA (CELLULAR GEOGRAPHIC SERVICE AREA)

The region in which a single service provider is licensed to operate. Includes all the cells covered by that license. If a single service provider provides service in multiple disjoint or adjoining areas, each probably has a separate license; is a different RSA or MSA; and therefore each is a different CGSA.

# CHAIN

A series of store and forward nodes through which a packet must pass when it is sent from one terminal to another.

# CHANNEL

Communication path. Note the ISDN channels are normally full duplex.

### **CHARACTER-ORIENTED PROTOCOL**

A set of rules for communicating data that relies upon special characters, such as SOH, STX and ETX, to control the flow of information. BISYNC is a character-oriented protocol.

# CHECKSUM

A block check character that is formed by taking the arithmetical sum of the binary data transmitted.

# **CHIP SET**

A set of integrated circuits that supply all or most of the circuitry needed to build an item of electronic equipment. Most modems and computers are built from chip sets.

#### **CIRCUIT SWITCHING**

Dedicates an entire circuit (normally DS0 in a digital system) to each call. Inefficient for bursty data.

# CITY-WIDE CENTREX

A combination of multiple centrex switches and SS7, which gives the customers the same features across a LATA that Centrex gives on a single switch.

# CLIENT-SEVER NETWORK

A network that uses a central computer, the server, to store data that is accessed from other computers on the network, called clients.

# CMIP (COMMON MANAGEMENT INFORMATION PROTO-COL)

An OSI protocol for the exchange of network management information that provides the means to request actions and report events but does not specify what those actions and events are.

# CMOS (COMPLEMENTARY METAL OXIDE SEMICON-DUCTOR)

A semiconductor field effect transistor (FET) technology which utilizes both N-Channel and P-Channel devices.

# CO (CENTRAL OFFICE)

The local telephone company switch that terminates subscribers lines for switching and connection to the public network. Known as a class 5 office. The most popular local exchange switches today are the 5ESS, DMS-100, 1AESS.

# COAX (COAXIAL CABLE)

A tubular wire transmission medium that consists of a central conductor surrounded by a dielectric insulator that is in turn surrounded by a tubular conductor. The outer conductor is usually at ground potential and also serves as an electrical shield.

# CODE

A system of using symbols to represent other information. ASCII and EBCDIC are two binary codes used in data communications.

# CODEC (CODER/DECODER)

A device that converts (codes) an analog signal to a digital PCM format and converts (decodes) an incoming digital PCM signal to analog.

# COLLISION

A contention situation in the CMSA/CD protocol when two nodes attempt to transmit simultaneously.

# **COMBINATIONAL NETWORK**

A network that uses more than one topology. A combinational network often results when several previously independent networks are linked.

# **COMMON CARRIER**

A company that provides communications services to any member of the public that desires them.

# **COMMUNICATIONS ARCHITECTURE**

A combination of hardware and software that implements some communications function. See architecture.

# **COMMUNICATIONS CONTROLLER**

An IBM satellite processor that manages communications lines from terminals and remote cluster controllers for a large host computer and statistically multiplexes the data into a single channel for transmission to the host com-

puter. Examples are IBM 3725, COMTEN 3690, etc. Also known as a Front End Processor (FEP). Not to be confused with a Cluster Controller.

#### COMMUNICATIONS PORT

A connection on a terminal through which data is input and/or output.

# **COMPRESSION RATIO**

The ratio of the number of bits required to represent the original information to the number of bits required to represent the compressed signal.

#### CONCENTRATOR

A hub-like device used on some FDDI networks to connect several single-attached nodes to the network.

#### CONDITIONED LINE

A telephone circuit that has had its frequency response and/or delay characteristics optimized.

# CONDITIONING

Applying electronic filtering to a communication link to improve its ability to support higher communication speeds. Also see equalization.

# **CONNECTION IDENTIFIER**

A part of the header information in an ATM cell that associates the cell with a given virtual channel. The connection identifier is used by network nodes for multiplexing, demultiplexing and switching.

# **CONNECTION-LESS PROTOCOL**

A packet-switched protocol that permits a terminal to send data thorough the network without first establishing a virtual connection to the receiving terminal.

# CONNECTION-ORIENTED PROTOCOL

A packet-switching technology, such as ATM, that can establish a virtual circuit between transmitting and receiving terminals so that it appears that the terminals are connected by a switched circuit with a fixed bandwidth. Connection-oriented protocols, unlike other packet-switching technologies, can be used to send information that requires a constant delay and bandwidth such as voice and video.

#### CONTENTION

A method of line control in which terminals compete with each other for permission to transmit over a common channel. If the channel is free, the terminal transmits. If the channel is in use by another terminal, the terminal attempting to transmit waits until the channel is free.

# **CORPORATE UTILITY NETWORKS**

Private Networks which carry all or nearly all of a company's voice data and voice traffic. They take advantage of the price benefits of buying bandwidth in quantity. The bandwidth is then usually divided up among the applications using T1 time division (TDM) circuit multiplexers. Some have used statistical multiplexers (X.25, or more efficient vendor proprietary protocols) for allocating the bandwidth. These private networks can be designed for

higher reliability and greater security than public networks.

# CPE (CUSTOMER PREMISES EQUIPMENT)

In the U.S., end-users equipment that may not be owned by the local exchange; Carrier equipment that resides on the end user's side of the network interface boundary established by Computer Inquiry II.

# **CPS** (CHARACTERS PER SECOND)

A transfer rate estimated from the bit rate and length of each character. If each character is 8 bits long and includes a start and stop bit for asynchronous transmission, each character needs 10 bits to be sent. At 2400 baud it is transmitted at approximately 240 CPS.

# CRC (CYCLIC REDUNDANCY CHECK)

A type of block check character that is very effective in detecting communications errors. CRC characters are usually 12, 16, 24 or 32 bits long.

# CROSSTALK

The unwanted transfer of energy from one communications circuit to another.

# CSMA/CD (CARRIER SENSE MULTIPLE ACCESS WITH COLLISION DETECTION)

A protocol that Ethernet and some other LANs use to allow nodes to contend for the right to transmit over the network.

#### CSU (CHANNEL SERVICE UNIT)

A customer-owned, physical-layer device that connects CPE, such as a router, to a DSU. The CSU uses V.35 or similar protocol to communicate with the CPE. Because of regulatory changes, there is no need for physical separation of CSU and DSU any longer. Most so-called "DSUs" now marketed are really combination CSU/DSUs.

# CT (CORDLESS TELEPHONE)

A generic term for systems evolved from the simple residential cordless telephone.

#### CT<sub>0</sub>

Another name for the British MTP1233 analog cordless telephone standard. The standard uses eight channel pairs with a base station transmit frequency near 1.7MHz and a handset transmit frequency near 47.5MHz.

# CT1 (CORDLESS TELEPHONE - FIRST GENERATION)

First generation CT with analog speech and FDMA.

# CT1+

A new version of the European CT1 analog cordless telephone standard that allocates 80 channel pairs in the 885 to 887MHz and 930 to 932MHz bands.

# CT2 (CORDLESS TELEPHONE - SECOND GENERATION)

Second generation CT with digital speech and FDMA.

# CT2+

An improved version of the CT2 cordless telephone standard that permits both incoming and outgoing calls.

# CT3 (CORDLESS TELEPHONE - THIRD GENERATION)

A generic name for third generation CT, or it can refer to Ericsson's implementation of its DCT 900 cordless telephones.

# CTIA (CELLULAR TELECOMMUNICATIONS INDUSTRY ASSOCIATION)

The cellular industry association, formed in May, 1984, to promote cellular technology, address common concerns, provide a forum for exchange of non-proprietary information, and provide a strong, effective voice in Washington. Represents more then 90% of the cellular carriers.

#### **D CHANNEL**

An ISDN statistically-multiplexed user-to-network channel. It carries signaling messages to control the B channels and/or X.25 packet-switched user data. It operates at 16kb/s in the Basic interface and 64kb/s in the Primary Rate Interface.

# DAB (DIGITAL AUDIO BROADCASTING)

A proposed service for satellite broadcasting of CD-quality audio. The FCC is proposing spectrum allocation in both

1429-1525MHz and 2300-2390MHz bands

to WARC.

DACS (DIGITAL ACCESS & CROSS-CONNECT SYSTEM)
Part of AT&T Service NET-2000.

# DAN (DESK AREA NETWORK)

The variety, power and complexity of the devices located on the desk top has increased to the point where the management and communications of this area deserves special consideration.

# DARPA (DEFENSE ADVANCED RESEARCH PROJECTS AGENCY)

A US Department of Defense Agency that funds high-risk research projects and that funded the development of UNIX 4.2, and the TCP/IP communications protocol.

# **DATA BASE**

An integrated collection of information that supports multiple applications and often multiple users.

# **DATA COMMUNICATIONS EQUIPMENT**

A device that modulates digital signals onto an analog carrier for communications over an analog communications link, or which demodulates received analog signals to recover the digital information. A modem.

# **DATA COMPRESSION**

A method of reducing the number of bits that are needed to represent information. Data compression allows higher communication speeds and allows more information to be stored on a disk.

#### **DATALINK LAYER**

Layer 2 of the OSI model. It defines error control, framing, synchronization, link initialization and disconnection, addressing and frame sequence control.

#### DATA MANAGEMENT

Software that manages the storage, retrieval, security, and integrity of information.

#### DATA RATE ADAPTATION

A feature of the data service unit (DSU) in the switched 56 service that allows the service to be used with terminals that operate at speed other than 56 kilobit per second. Data rate adaptation is the conversion between whichever clocking scheme and speed the terminal uses and the 56 kilobit per second synchronous clocking of the switched 56 line.

# **DATA SET**

Telephone company jargon for a modem.

#### DATAGRAM

A Layer 3 packet. Typically in a connectionless service, in which case its header will contain source address and destination address.

# dB (DECIBEL)

A unit for measuring the relative strength of signal power. The number of decibels equals ten times the logarithm (to the base 10) of the ratio of the measured signal power to a reference power. One-tenth of a Bell.

dBm (DECIBEL REFERENCING 1 MILLIWATT)
Signal power relative to 1mW expressed in dB.

# **DBS** (DIRECT BROADCAST FROM SATELLITE)

A service for Broadcast of TV (and HDTV) signals from

# DCE (DATA CIRCUIT TERMINATING EQUIPMENT)

Carrier's equipment that is the DTE's Interface to the Network

# DCT 900 (ERICSSON'S DIGITAL CORDLESS TELE-PHONE AT 900MHz)

Ericsson's CT3 implementation of digital cordless telephones and base stations intended for use with PBXs.

# **DDD** (DIRECT DISTANCE DIAL NETWORK)

A telephone network to directly dial long distance telephone calls.

# **DDS** (DIGITAL DATAPHONE SERVICE)

Originally an AT&T nationwide non-switched special service network for synchronous data at speeds up to 56kb/s.

#### **DECnet**

Digital Equipment Corporation's family of network products.

# **DECT (DIGITAL EUROPEAN CORDLESS TELEPHONE)**

A digital cordless telephone standard that incorporates some of the features of a cellular telephone system.

DECT telephones use picocells and calls can be handed off from one cell to the next.

# **DEMUX (DEMULTIPLEXING)**

The process of separating a multiplexed signal into its separate intelligence signals.

#### **DETERMINISTIC MULTIPLEXING**

Each channel takes a constant, determined space. Digital systems use time division multiplexing (TDM) while analog systems use frequency division multiplexing.

# **DIGITAL INFORMATION**

A stream of binary (0's and 1's) bits. Voice, documents, and even television can be sampled, quantized and converted to a digital bit stream.

#### **DIGITAL SIGNAL**

Has a very limited number of discrete states. (Usually no more than 4.) Contrasted with an analog signal which varies continuously and thus may have virtually an infinite number of states.

# DIGITAL SYSTEMS INTERFACE

A chip-to-chip interface for ISDN modules supported by National Semiconductor and SGS-Thomson.

# **DIGITAL TRANSMISSION**

Repeats where necessary by deriving then regenerating the original digital data. Much of the noise is removed by a digital system.

#### **DMS-10**

NT small to medium-size digital end office (class 5) switch.

# **DMS-100**

NT large digital end office (class 5) switch.

# **DMS-200**

NT large digital toll, access tandem, and/or operator switch.

#### **DMS-250**

NT large digital toll and operator switch for Interexchange Carriers. Makes up the bulk of the Sprint and half of the MCI long distance networks.

# DOC (DEPT. OF COMMUNICATIONS)

The Canadian equivalent of FCC. Responsible for allocating spectrum in Canada.

# **DOWNLOAD**

The process of transferring a file from a remote computer (called the host) to the user's computer.

# dpi (DOTS PER INCH)

# **DPN** (DIGITAL PACKET NETWORK)

NT packet-switched product line evolved from the successful SL10 packet switch.

#### DROP

A connection between a terminal and a multi-drop (bus) network.

# DS (DIRECT SEQUENCE)

The most common "spread spectrum" technique used in CDMA which spreads the signal bandwidth by directly modulating the signal with a pseudo noise sequence.

# DS0 (DIGITAL SIGNAL, LEVEL 0)

64kb/s rate. This is the basic building block in both the North American and European digital hierarchies. A DS0 channel can carry any one of the following:

An uncompressed voice call

A compressed high quality voice call

2 or more compressed voice calls

Data at speeds up to 56 or 64kb/s.

# DS1 (DIGITAL SIGNAL, LEVEL 1)

1.544Mb/s North American rate. This is the rate used by T1 carrier.

# DS2 (DIGITAL SIGNAL, LEVEL 2)

6.312Mb/s North American rate. This is the rate used by T2 carrier for 96 calls. It is expensive to install since it requires special cable, therefore, it is quite rare.

# DS3 (DIGITAL SIGNAL, LEVEL 3)

44.736Mb/s North American rate. Consists of 28 DS1S plus overhead.

# **DSL** (DIGITAL SUBSCRIBER LINE)

ISDN Basic Interface (2B+D) provided over a normal customer line (or loop).

# DSP (DIGITAL SIGNAL PROCESSOR)

A digital integrated circuit (IC) designed as a general purpose filter and signal processor.

# **DSU** (DIGITAL SERVICE UNIT)

A customer-owned, physical-layer device that terminates an access line, such as a T1, from the network. The customer's "mirror image" of a central office repeater. Traditionally, DSUs were network equipment used in conjunction with customer-owned CSUs (Channel Service Units) to determinate access lines. Because of regulatory changes, there is no need for physical separation of CSU and DSU any longer. Most so-called "DSUs" now marketed are really combination CSU/DSUs.

# **DTE (DATA TERMINAL EQUIPMENT)**

User terminal equipment.

# **DTMF** (DUAL TONE MULTI-FREQUENCY)

We can say Touchtone now that AT&T no longer enforces the trademark.

# **DU100 MODEM POOL ELEMENT**

A device marketed by Motorola that allows users of the switched 56 service to communicate with analog modems at speeds of up to 9,600 b/s.

# **DUAL ATTACH NODE**

An FDDI terminal that connects to both the primary and secondary nodes. A dual-attach node has two input ports and two output ports.

# DYNAMIC ROUTER

A router that automatically broadcasts routing information throughout the internet work at regular intervals. Other dynamic routers use this information to update their routing tables in case any changes have been made to the network.

# E - MAIL (ELECTRONIC MAIL)

Electronic messages that can be sent over a communications network from one computer to another.

# E-TDMA (ENHANCED TDMA)

Proposal by Hughes, and others, with DSI and lower bitrate vocoder to increase TDMA capacity.

#### E.164

Numbering Plan for the ISDN Era.

# **EAMPS** (EXPANDED AMPS)

Expansion of AMPS to utilize the extra 10MHz BW allocated by the FCC.

# EBCDIC (EXTENDED BINARY CODED DECIMAL INTER-CHANGE CODE)

An eight bit code that was developed by IBM Corporation and is widely used for the communication of text.

# **ECHO CANCELLATION**

A circuit that uses DSP technology in a full duplex communications node to remove echoes of the transmitted signal from the received signal.

# **ECHO DISTORTION**

A telephone line impairment caused by electrical reflections (echoes) where line impedances are dissimilar.

# EDSL (EXTENDED DIGITAL SUBSCRIBER LINE)

Old name for Primary Rate Interface (PRI).

# EMSR (ENHANCED SPECIALIZED MOBILE RADIO)

Enhanced Specialized Mobile Radio services proposed recently by Fleet Call to FCC. Would provide improved digital mobile radio and telephone service over aggregated channels in major markets. This is seen as competition to cellular. Would also provide FAX, vehicle location, and emergency service as well as dispatching and mobile phone services.

# **ENCODING**

The process of putting information into digital format.

#### **ENCRYPTION**

A technique of modifying a bit stream to make it appear to be a random sequence of bits to someone who does not have access to the encryption scheme.

# **END-TO-END**

An operation that proceeds from one end point to the other without being processed in each switch along the way. Not link-by-link.

# **ENVELOPE DELAY**

A type of distortion on an analog line where the signal delay is a function of frequency.

# **EQUALIZATION**

Compensation for frequency dependent attenuation in a communications circuit. Its purpose is to provide an equal signal attenuation over the circuit's full frequency range. See conditioning.

#### **ERROR CONTROL**

A method of detecting and correcting errors within a block of data.

#### **ERROR RATE**

The ratio of the number of data units received in error to the total number of data units. Also called bit error rate (BER).

# ET (EXCHANGE TERMINATION)

An ISDN interface located in the telephone company central office switch.

# **ETHERNET**

A LAN standard, also known as IEEE 802.3, that connects personal computers by means of coaxial cable or twisted pair conductors. Most Ethernet LANs operate at 10 megabits per second.

# EURO ISDN (EUROFILE TRANSFER STANDARD FOR ISDN)

An international ISDN standard for Europe that is presently being installed and will eventually replace national ISDN standards.

# **EXCHANGE AREA**

A geographical area with which there is a uniform set of charges for a communications service. In a telephone system, a call between any two points within an exchange are is a local call.

# **FACILITY**

A transmission path between two or more locations without terminating or signaling equipment.

# FAX (FACSIMILE)

A communications terminal for the transmission of graphics and documents.

# FCC (FEDERAL COMMUNICATIONS COMMISSION)

A U.S. Federal government agency made up of seven commissioners appointed by the president and having the power to regulate all radio communications and all interstate electrical communications within the US and all electrical communications between the US and other countries.

# FCS (FRAME CHECK SEQUENCE)

A CRC used in LAPD.

# FDDI (FIBER DATA DISTRIBUTED INTERFACE)

A line standard that uses fiber-optic cable or twisted pair wire to connect computers. FDDI LANs operate at 100 megabits per second.

# FDMA (FREQUENCY DIVISION MULTIPLE ACCESS)

A method of allowing multiple users to share the radio frequency spectrum by assigning each active user an individual frequency channel.

#### FDX (FULL DUPLEX)

A communications method where each end simultaneously transmits and receives.

# FEC (FORWARD ERROR CORRECTION)

Any system that allows a terminal to both detect and correct errors in received data.

# FEP (FRONT END PROCESSOR)

Synonym for IBM Communications Controller. Routes the traffic to and from the cluster controllers. Is usually colocated with the host computer, but can be remotely deployed either to save polling overhead or to serve as a routing device.

# FFS (For Further Study)

# FHSS (FREQUENCY HOPPING SPREAD SPECTRUM)

A spread spectrum technology in which the transmitted signal "hops" from one frequency to the next in discrete steps. Contrast with direct sequence spread spectrum.

# **FIBER NODE**

A field cabinet, or accessible service pint, served by fiber, in Cable Television or Telephone Company distribution plant.

# **FIBER OPTICS**

A transmission medium consisting of thin strands of glass or plastic through which data is sent over pulse-modulated light waves.

#### FIFO MEMORY (FIRST-IN, FIRST-OUT MEMORY)

A type of memory with separate input and output ports. The first data to enter the input port are the first to exit the output port. One use of FIFO memory is as buffer between a terminal and a LAN in a network interface controller.

#### **FILTER**

An electrical circuit that passes frequencies within a certain band and attenuates others.

#### **FIRM WARE**

A set of software instructions placed in a read-only memory (ROM).

# FKS (FREQUENCY-SHIFT KEYING)

A type of frequency modulation used by low-speed modems.

#### FLAG CHARACTER

Layer 2 start of transmission and end of transmission character. Value is 011111110.

#### FLOW CONTROL

A method for a receiver to govern the information flow from a transmitter. This avoids the receiver being overrun and losing data, or needing a potentially infinite number of buffers.

# FM (FREQUENCY MODULATION)

A method of impressing information on a carrier wave, in which the frequency of the carrier is modified according to a plan agreed to by the transmitter and receiver. Frequency Modulation can be analog (where the frequency modifications are continuous over a specified range) or digital (where the frequency modifications are according to discrete intervals which represent ones and zeros). Compare Frequency Modulation to Amplitude Modulation and Phase Modulation. Frequency Modulation has been used extensively in broadcast radio and traditional AMPS cellular service. FM has a useful characteristic that the receiver tends to "lock on" to the strongest signal at the given carrier frequency, and is therefore somewhat better able to withstand co-channel interference than other modulation techniques.

#### **FORMAT**

A specified arrangement of data that permits identification of control and information field by their location in the data stream.

# FOUR-WIRE CIRCUIT

A full-duplex communication channel over which transmission occurs over one pair of wires, and reception occurs over a separate pair.

# FPLMTS (FUTURE PUBLIC LAND MOBILE TELECOMMUNICATIONS SYSTEMS)

CCITT's term for the next generation(s) of wireless access to public mobile and personal network services. Sometimes pronounced "Flumpits" or "Flumpts". Another term for UMTS.

# FRAME (LAYER 1)

On digital transmission facilities in the telephone network the digital bit stream is organized into fixed units, called frames, which are transmitted every 125 microseconds (8000 times per second). Typically, on time division multiplexed lines, the frame consists of a block of data consisting of one time slot from each channel plus synchronization and other overhead bits.

# FRAME (LAYER 2)

Block of data at Layer 2. Begins and ends with a flag character.

#### FRAMING ERROR

A communications error that occurs when the receiving terminal is unable to determine where a data word begins and ends.

#### FRAME RELAY

Basically a stripped-down, souped-up X.25 optimized for low error rate networks carrying up to about 4000 bytes per frame. A connection-oriented, multiplexed, Layer 2, HDLC protocol with almost no procedures. In particular the HDLC control field is not included in the procedures. Two kinds of calls are defined, Permanent Virtual Circuits (PVCs), which are set up with administrative procedures and Switched Virtual Circuits (SVCs), which are set up with Q.931. Setting up a call creates a connection between one Data Link Connection Identifier (DLCI) on a user-to-network interface (UNI) and another DLCI on another UNI. Error recovery and flow control are not part of Frame Relay procedures and must be performed end-to-end. Congestion control procedures are defined using three congestion control bits.

# FRAMING (LAYER 1)

The method and process for locating the start of every 125ms Layer 1 frame. Then each time slot of element within a frame can be identified.

# FT1 (FRACTIONAL T1)

In TI carrier systems when a fraction of the total twenty-four 64kb/s channels are assigned to an individual customer. The remainder of the channels are then available to be used by other customers. This provides intermediate pricing levels between a DSO channel (56kb/s or 64kb/s) and a full T1. IECs are in the best position to share channels and generally offer these pricing levels.

# GAP (GROUND-TO-AIR PAGING)

The ability to page a station in an airplane from the ground.

#### GAIN

The amount by which a signal's strength is increased when it passes through an amplifier or a repeater. Gain is usually measured in decibels, but it can also be expressed as the ratio of output power to input power.

#### **GATEWAY**

A device that connects two or more networks of different types together and functions at OSI layers 1 through 3.

# **GCI** (GENERAL COMMUNICATION INTERFACE)

An ISDN inter-chip standard interface both basic rate and primary rate equipment.

# GFSK (GAUSSIAN FREQUENCY-SHIFT-KEYING MODU-LATION)

A form of filtered FSK that greatly reduces the bandwidth required to transmit information. The data stream passes through a Gaussian shaped digital finite-impulse response (FIR) filter, which uses DSP techniques to shape the signal.

# **GROUPE SPECIAL MOBILE**

Former name of the Global Systems for Mobile Communications (GSM) European digital cellular standard.

# GSM (GLOBAL SYSTEM FOR MOBILE COMMUNICA-TIONS)

The pan-European Digital Cellular Radio Standard (based on TDMA-8) in 900MHz band. Previously called Group Special Mobile after the standards committee that developed it.

# **GSO** (GEOSTATIONARY SATELLITE ORBIT)

A satellite orbit 23,000 miles over the equator with an orbit time of exactly 24 hours. Thus a satellite in a Geostationary Satellite Orbit appears motionless to an earth station which can receive it with a stationary antenna. One drawback is that a two way communication channel through a geostationary satellite incurs a round trip, speed of light delay of over one half second.

# **HO CHANNEL**

384kb/s channel (6 64kb/s channels or one-quarter of a T1 line).

#### H<sub>10</sub> CHANNEL

North American 1472kb/s channel from a T1 or primary rate carrier. Equivalent to 23kb/s channels.

#### H11 CHANNEL

North American primary rate used as a single 1536kb/s channel (24 64kb/s channels or an entire T1 line except for the 8kb/s framing pattern.)

# H12 CHANNEL

European primary rate used as a single 1920kb/s channel (30 64kb/s channels or an entire primary rate carrier, except the 64kb/s signaling channel and the 64kb/s framing and maintenance channel.)

# HALF DUPLEX

A communications method where one end transmits while the other end receives, then the process is reversed.

# **HAMMING CODE**

A forward error correction scheme named for its inventor that can correct single bit errors without the need for retransmission.

#### HANDSHAKING

A set of signals that coordinate the transfer of data from one device to another.

# **HARMONIC**

A frequency that is a multiple of a fundamental value.

# HARMONIC DISTORTION

A type of communications line distortion that is caused by erroneous frequency generation along the line.

# HDLC (HIGH-LEVEL DATA LINK CONTROL)

An ISO bit-oriented protocol Superset that is the basis for most modern Layer 2 protocols.

# HDSL (HIGH BIT-RATE DIGITAL SUBSCRIBER LINE)

A technology to transport T1 data (1.544 megabits per second) over 12,000 feet of 24-guage wire or 9,000 feet of 26-guage wire without the need for repeaters. It requires two pairs of wire, each of which carriers full-duplex data at half the total speed using 2B1Q modulation.

# **HETEROGENEOUS**

Made up of different systems, vendor's products, or architectures.

#### HIERARCHICAL NETWORK

A network topology organized in the form of a pyramid with one terminal at the top and increasing numbers of terminals at each lower level. Also called a tree.

#### HIT

Errors on a communications link caused by impulse noise.

#### **HOUSE CABLE**

Conductors inside a building used to connect communication equipment to outside lines.

#### HUB

A central node in a star network. All other nodes are connected to the hub by means of point-to-point communications links

# **HUFFMAN ENCODING**

A data compression scheme that uses fewer bits to represent frequently occurring characters. Huffman encoding works well with text.

# **HYBRID**

A telephone circuit that joins a two-wire line to a four-wire line. Originally, hybrids were transformers, but today they are electronic circuits.

# **HYPERSTREAM**

The marketing name for MCI's SMDS service.

# Hz (CYCLES PER SECOND)

# I.441 (Q.921)

ISDN user-network interface - (D Channel) Layer 2 specification. Part of DSS1.

# IEC (INTEREXCHANGE CARRIER)

A long distance company such as AT&T, MCI, Sprint, or hundreds of smaller companies.

# IEEE (INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS)

A membership organization of engineers that, among other activities, produces data communications standards.

# **IEEE 802.11**

The IEEE 802 committee chartered to develop Physical Layer (PHY) and Medium Access Control Layer (MAC) specifications for wireless LANS.

# IMASS (INTELLIGENT MULTIPLE ACCESS SPECTRUM SHARING)

A method of utilizing spectrum "gaps" between existing private operational fixed microwave (OFM) systems. Avoid interference and displacement of current licenses.

#### IMPULSE NOISE

A type of communications line interference characterized by high amplitude and short duration.

# IMTS (IMPROVED MOBILE TELEPHONE SERVICE)

The pre-cellular mobile telephone service enhancement introduced in 1965 which permitted full duplex mobile radio communications.

# IN (INTELLIGENT NETWORK)

Initial services are 800, VPN, and calling card.

#### INBAND SIGNALING

Signaling that travels on the same circuit and uses the same frequencies as the call.

# INMARSAT (THE INTERNATIONAL MARITIME SATEL-LITE ORGANIZATION)

The international organization, with participation for the U.S. solely by Communications Satellite Corp., chartered to develop and operate global maritime facilities and service for the commercial and safety needs of U.S. and foreign countries.

# **INTEGRATED ACCESS**

The use of a single access service, such as T1, to transport multiple service types, such as switched voice and dedicated private lines. As an example a customer may purchase a T1 service from a LEC and arrange with an IEC to have some of the channels connected to a voice switch and some connected to private lines for data.

# INTELSAT (INTERNATIONAL TELECOMMUNICATIONS SATELLITE ORGANIZATION)

The international organization, of which the U.S. Is a party, established to develop and operate a global commercial communications satellite system.

#### **INTERFACE**

A common boundary between two or more systems, integrated circuits, or pieces of equipment that ensures a proper connection between them.

# **INTERNATIONAL STANDARDS ORGANIZATION (ISO)**

The standards organization that developed the Open Systems Interconnect Model and other international communications standards.

#### INTERNETWORKING

The technique of connecting individual LANs to form a larger network.

# INTEROFFICE TRUNK

A telephone circuit that connects two telephone company offices.

# IRAC (INTERAGENCY RADIO ADVISORY COMMITTEE)

A government committee which advises the Commerce Secretary on the government's spectrum needs.

# IS-54 (EIA/TIA INTERIM STANDARD-54)

The North American Digital Cellular proposed standard recommended by the CTIA. It is based on TDMA.

#### **IS-94**

A CDMA standard for use in the U.S.

# **IS-136**

A digital cellular standard proposed for North America. An earlier version of the standard is called IS-95. Commonly referred to as TDMA, even though it is only one of several digital cellular standards that use this technology.

# ISDN (INTEGRATED SERVICES DIGITAL NETWORK)

An evolution of the Integrated Digital Network providing end-to-end digital connectivity to which users have access to a wide range of services through a limited set of standard user-to-network interfaces.

# ISI (INTERSYMBOL INTERFERENCE)

The interference resulting when delayed signal symbols (e.g., reflected signals) interfere with the symbols of the direct signal.

# ISM BANDS (Industrial Scientific and Medical Bands)

Abbreviation for the North American "industrial, scientific, and medical" bands that were originally set aside for heating devices including welders and microwave ovens but which are now open to certain unlicensed communications technologies including digital cordless telephones and wireless LANs.

# ISO (INTERNATIONAL ORGANIZATION FOR STANDARD-IZATION)

Best known for the 7-layer OSI Reference Model. See OSI

# ITU (INTERNATIONAL TELECOMMUNICATIONS UNION)

A telecommunications agency established by the United Nations to provide standardized communication procedures and practices including frequency allocation and world-wide radio regulation. The ITU is the successor organization to the CCITT. Has four permanent organs, the CCITT, CCIR, International Frequency Registration Board (IFRB), and General Secretariat. Founded in 1865.

#### **JITTER**

A short-term timing deviation.

# J-TACS (JAPANESE TACS)

Narrow band analog FM analog cellular system. 12.5kHz wide channels.

#### **KEY SET**

Telephone set having more buttons than the normal 12 button keypad. Additional buttons are for access to multiple lines. Directory numbers, hold, etc.

km (KILOMETER) 3.3 kilofeet

#### LAN (LOCAL AREA NETWORK)

As defined by IEEE Committee 802.6: A non-public data network in which serial transmission is used without store and forward techniques for direct communication among data stations on a user's premises. Examples are ethernet (802.3) and token ring (802.5).

#### LAPB (LINK ACCESS PROCEDURE BALANCED)

Bit-oriented data link protocol standards published by the CCITT that specify the functions of the data link level of CCITT Recommendation X.25. They are compatible subsets of HDLC. (See High-Level Data Link Control).

# LAPD (LINK ACCESS PROCEDURE D)

Layer 2 protocol defined in CCITT recommendations I.440/44l/442 cross referenced as Q.920/921/922. Reliably transfers blocks of information across a single Layer 1 link. Unlike LAP and LAPB, supports multiplexing of different connections at Layer 2.

Originally used on the ISDN D Channel, LAPD is the foundation for V.120, frame switching and frame relay.

# LAPM (LINK ACCESS PROCEDURE FOR MODEMS)

An error correction scheme.

# LATA (LOCAL ACCESS TRANSPORT AREA)

Upon divestiture, the United States, Puerto Rico, Guam and the Virgin Islands were divided into 198 areas for the purpose of interconnectivity, known as Local Access Transport Areas (LATAs). Population density was a primary consideration when LATA boundaries were determined. High population areas, like the North-East U.S., have relatively small LATAs, while places like Wyoming and South Dakota are contained with a single LATA. A LATA defines the boundary within which most LECs (the RBOCS and GTE) can provide end-to-end multi-switch service. If the called party is inside a different LATA than the call originator, then the affected LECs must hand off the call to an IEC (such as AT&T, MCI, Sprint, etc.). This restriction applies to any end-to-end information transfers, not just voice transmission. Currently regulatory interpretation considers SS7 messages as end-to-end information transfers. Thus, a signaling message for a remote LATA must be handed off to an IEC SS7 network for transport. Because the need to hand off inter-LATA requires that the signaling network as well as transport facilities be interconnected across the LATA boundaries, the LECs' implementation of SS7 is more complicated than that of the IECs. Even though the restriction to use an IEC for inter-LATA communications only applies to the BOCs and GTE, most of the smaller independent LECs operate within a single LATA and most inter-LATA communications are handled by and IEC.

# LAYER 1

Physical Layer in OSI Reference mode. Includes transmission of signals and the activation and deactivation of physical connections.

# LAYER 2

Link Layer in OSI Reference mode. Includes synchronization and some control over the influence of errors within the physical layer.

#### LAYER 3

Network layer in OSI Reference model. Includes routing and switching functions.

# LAYER 4

Transport layer in OSI Reference mode. Uses Layers 1 to 3 to provide an end-to-end service with the required characteristics for the higher layer functions.

#### LAYER 5

Session layer in OSI Reference model. Allows presentation entities to organize and synchronize their dialogue and to manage their data exchange.

# LAYER 6

Presentation layer in OSI Reference model. Includes data formatting and code conversion.

# LAYER 7

Application layer in OSI Reference model. Provides the means by which the user programs access the OSI environment and may contain part of these user programs.

# LCM (LINE CONCENTRATING MODULE)

Part of NT DMS-100. Handles up to 640 lines with up to 6 duplicated digital links. Occupies 1/2 Bay.

# **LEASED LINE**

A semi-permanent leased telephone circuit that connects two or more points and is continuously available to the subscriber.

# LEC (LOCAL EXCHANGE CARRIER)

Local telephone company. Bell company or independent such as Southern New England Telephone (SNET), Cincinnati Bell, GTE (Contel), United, Centel, Rochester Telephone, Warnego Telephone, or hundreds of others.

# LEO (LOW-EARTH ORBIT)

The use of satellites much lower than geostationary heights to keep delay low.

#### LINE

A communication path between a switch and one end user. Analog lines are termed tip and ring and carry one telephone call. ISDN lines are called Digital Subscriber Lines and can carry several calls.

# LINE PROTOCOL

A control program used to perform data communication functions over network lines and which consists of hand shaking and line-control functions that move the data between the transmit and receive terminals.

#### LINK

Circuit or channel from one switch to another.

# LINK-BY-LINK

An operation that proceeds sequentially, form one switch to the next over each successive line. Not end-to-end.

# LOCAL OFFICE SWITCH

A telephone switch that serves all subscribers connected to a single telephone exchange.

# LOOP

Pair of wires connecting the subscriber to the Telephone Company central office.

# LOOPBACK

Directing signals back toward the transmitting terminal at some pint along the communications path. Used as a method of troubleshooting.

# LPC (LINEAR PREDICTIVE CODING)

A method of speech coding which models the vocal tract of humans and transmits model parameters and one of a pair of simple excitation sources (a tone or noise) to recreate (predict) the next few milliseconds of speech sound.

# LSB (LEAST SIGNIFICANT BIT)

Lowest order bit in the binary representation of a numerical value. The LSB has the least impact on the value of the number which is digitally represented. For example, in voice encoding, the least significant bit can occasionally be dropped without causing noticeable degradation of speech quality.

# LT (LINE TERMINATION)

An ISDN interface used between the local loop and the telco central office switch.

# M13 (MULTIPLEXER DS1 TO DS3)

#### **MAGNITUDE BIT**

The second bit in a dibit (group of two bits) in a 2 binary, 1 quaternary modulation. The magnitude bit determines the voltage level of the transmitted signal. The other bit is called the sign bit and determines if the voltage is positive or negative.

# **MANCHESTER ENCODING**

A coding scheme used with several LANs. Manchester encoding has a logic transition in the center of each bit. A positive transition indicates a logic 1 and a negative transition indicates a logic 0.

#### MARK

Communications terminology for a binary 1 in a data communication.

# MAU (MEDIA ACCESS UNIT AND MULTI-STATION ACCESS UNIT)

A device used to connect a terminal to a 10BASE-5 Ethernet LAN. A Token Ring hub. The hub gives the Token Ring LAN the physical appearance of a star network, although electrically it is still a ring.

# MDS (MULTIPOINT DISTRIBUTION SERVICE)

A communication system that delivers video programming to subscribers over microwave radio links. From the consumer point of view, MDS is similar to cable television and it is popularly known as wireless cable.

# **MEDIUM**

The path information travels from the transmitter to the receiver in a communications systems.

# MESH NETWORK

A network topology that features numerous communications links among the terminals.

#### MESSAGE

An information package, typically in a specific digital code, that is transmitted over a communications system.

# MF (MULTI-FREQUENCY)

System of dual tones used for in-band trunk signaling. Similar to touch tone, but uses different frequencies.

# MFJ (MODIFIED FINAL JUDGMENT)

The agreement between AT&T and the Department of Justice, enforced by Judge Greene, wherein AT&T divested itself of the seven regional holding companies and their Bell Operating Companies (BOCs).

# MFLOPS (MILLIONS OF FLOATING POINT INSTRUC-TIONS PER SECOND)

A measure of the computing power measured in terms of its ability to do complex multiplication, division, addition, and subtraction with "floating point", (i.e., non-integer) numbers - e.g., in DSPs.

# MIDSPAN MEET

The ability to connect different vendors' equipment to each other on a communication network and have them function properly with each other.

# MIPS (MILLIONS OF INSTRUCTIONS PER SECOND)

A measure of the computing power measured in terms of the number of instructions it can execute in seconds. Its value is highly dependent, of course, on how powerful its instructions actually are.

# MIRS (MOTOROLA INTEGRATED RADIO SYSTEM)

Motorola's next generation of trunked SMR using TDMA/6 in bandwidth of one FM channel today. Fleet Call plans to use in its Enhanced Specialized Mobile Radio (ESMR) systems in LA.

# MIXED SIGNAL SEMICONDUCTORS

Integrated circuits that combine both analog and digital technology. Examples of mixed signal semiconductor devices are analog to digital converters, digital to analog converters, CODEC's, and vocoders.

# MNP (MICRON NETWORK PROTOCOL)

A system of error checking and data compression protocols that has become a defacto standard for modem communications.

# MODEM - MODULATOR/DEMODULATOR

A DCE. Used to modulate digital data onto an analog carrier so that it can be sent over an analog communications medium such as a telephone link and to demodulate the data at the receiving terminal.

#### MODULATION

The process of impressing information on a carrier wave. Modulators change either the amplitude, frequency, or phase of a carrier wave to represent ones and zeros (in digital modulation) or other signals.

# MPT (MINISTRY OF POSTS AND TELECOMMUNICATIONS)

Japanese government regulatory agency that oversees communications.

#### MPT1233

An analog cordless standard used in the U.K. Sometimes called CT0. The standard uses eight channel pairs with a base station transmit frequency near 1.7MHz and a hand-set transmit frequency near 47.5MHz.

# MSA (METROPOLITAN STATISTICAL AREA)

The largest (by population) U.S. 306 Cellular Market areas as defined by the FCC.

# MSB (MOST SIGNIFICANT BIT)

Highest order bit in the binary representation of a numerical value. The MSB has the most impact on the value of the number which is digitally represented. Loss of the MSB for any encoding, even speech, unacceptably corrupts the received information.

# MSC (MOBILE SERVICES SWITCHING CENTER)

A generic name for the main switching center supporting multiple base stations.

#### msec

Milliseconds. Thousandths of a second.

# MSS (MOBILE SATELLITE SERVICE)

A generic name for mobile services provided using earth satellites.

# MTA (MAJOR TRADING AREA)

To identify areas of economic integration, Rand McNally (1-800-284-6565) in their \$395 "Commercial Atlas and Marketing Guide," has divided the country into 47 Major Trading Areas (MTAs). An MTA consists of a number of counties; counties are never split between MTAs. For example, the Chicago MTA consists of 84 counties. Each MTA consists of one or more Basic Trading Areas (BTAs). For instance, the Chicago MTA includes 18 BTAs such as Rockford BTA, Springfield BTA, Ft. Wayne BTA, etc. Milwaukee is another MTA.

# MTSO (MOBILE TELEPHONE SWITCHING OFFICE)

A system that provides telephone switching services for a cellular telephone network. Wire telephone lines connect the MTSO to each of the cellular base stations that it serves, and trunk lines connect the MTSO to the telephone company's central office switch. An AMPS and cellular term for what is now generically called MSC (Mobile Service Switching Center).

# MTX (MOBILE TELEPHONE EXCHANGE)

The Northern Telecom term for MTSO (Mobile Telephone Switching Office).

#### **MULTICAST**

A service with one transmitter and more than one addressed receiver. (Compare to broadcast - With broadcast, all receivers on the network are addressed. With multicast, a subset of the receivers are addressed.)

#### **MULTI-MEDIA COMMUNICATIONS**

A communication that is made up of a combination of text, graphics, video, and audio.

# MULTIPLEXING

Dividing a transmission facility into two or more channels. Please refer to statistical multiplexing or deterministic multiplexing.

# MUX (MULTIPLEXER)

Equipment that divides a transmission facility into two or more channels. Please refer to statistical multiplexing or deterministic multiplexing.

# N-ISDN (NARROWBAND ISDN)

Includes basic interface (2B+D or BRI) and primary rate interface (23B+D or PRI). Copper based at speeds at or below 1.5Mb/s.

# N-TACS (NARROWBAND TACS)

The narrowband version of TACS from Motorola which doubles the capacity of TACS by splitting the 25kHz TACS channel into two 12.5kHz channels.

# NAMPS (NARROWBAND ADVANCED MOBILE PHONE SERVICE)

Motorola's narrowband AMPS getting three 10kHz channels in bandwidth of one 30kHz channel, along with improved signaling. Pronounced N-AMPS.

# NANP (NORTH AMERICAN NUMBERING PLAN)

Specifies the 10 digit telephone address.

3-digit Area Code or Numbering Plan Area (NPA) plus 7-digit directory number comprised of 3-digit Central Office (CO) code and 4-digit station number.

# **NETWORK**

A set of terminals, the communications links that joint them, and the protocols that allow them to function together and communicate with each other.

# **NETWORK ADMINISTRATOR**

A person who is responsible for the efficient operation of one or more LANs.

#### **NETWORK LAYER**

Layer 3 of the OSI model. It defines how data are switched and routed through the network.

# **NETWORK MANAGEMENT SYSTEM**

Software for managing the operation of a multi-point network from a central location.

# NETWORK-TO-NETWORK INTERFACE

An ATM interface that connects ATM switches to each other. Also see user-to-network interface.

#### **NETWORK OPERATING SYSTEM**

A software program that provides a network user interface and controls the network's operation to allow users to communicate with each other and share files and peripherals.

# NFS (NETWORK FILE SYSTEM)

A protocol for transparently sharing files across a computer network that was developed by Sun Microsystems and is now a defacto standard for UNIX computers. It is based upon TCP /IP and Ethernet.

# NIC (NETWORK INTERFACE CONTROLLER)

An interface that is usually located within a terminal and which connects a LAN to the terminals address, data and control buses.

# NMT450 (NORDIC MOBILE TELEPHONE AT 450MHz)

The Nordic Mobile Telephone system operating at 450MHz; introduced in 1981.

#### NMT900 (NORDIC MOBILE TELEPHONE AT 900MHz)

Essentially an upgrade of the NMT450 to 900MHz with enhancements and more channels.

# NNI (NETWORK NODE INTERFACE AND NETWORK-TO-NETWORK INTERFACE)

There are two different interfaces that are abbreviated NNI. Frame Relay defines a Network-to-Network Interface as the interface between two networks. This could be networks of two different carriers; for example between a Local Exchange Carrier and an Interexchange Carrier. Or, this could be between a customer frame relay network and an Interexchange Carrier network. Since the current definition of the Frame Relay NNI is NOT cell based, its use is not appropriate as an efficient interface between Frame Relay switches manufactured by a single vendor used in a single network. Instead vendor-specific interfaces are used. ATM and Broadband ISDN define a Network Node Interface as the interface between two network switches. This could be switches of two different carriers; for example between a Local Exchange Carrier and an Interexchange Carrier. The ATM NNI is also designed to be efficient enough to be the interface between ATM switches manufactured by a single vendor used in a single network.

# NODE

A terminal on a data communications network.

# NOISE

Random and undesired electrical signals that are introduced into a communications channel by circuit components, natural electrical activity, or the operation of electrical equipment.

# NORDIC MOBILE TELEPHONE (NMT)

A European analog cellular telephone standard derived for the U.S. AMPS standard. NMT is deployed in the Scandinavian countries, the Benelux countries, France, Spain, and in much of Eastern Europe.

# NPA (NUMBERING PLAN AREA)

Commonly known as "Area Code" (e.g., 212, 800, or 900).

NPRM (NOTICE OF PROPOSED RULEMAKING [BY FCC]) FCC Notification to the Industry of its intent to define new regulations.

# NT (NETWORK TERMINATION)

Network Termination, as in NT1, NT2 or NT12. An ISDN interface installed at a subscriber's premises that interfaces the customer's premises equipment to the telephone company local loop.

# NT1 (NETWORK TERMINATION 1)

In the U.S., a customer-owned device that converts from external telephone company transmission format (U interface) to internal building transmission format (T interface). Concerned only with Layer 1. Should contain loopback and other maintenance capabilities to enable problems to be isolated to the telephone network or customer's equipment. NT1 for basis interface contains digital hybrid circuitry. Before ISDN this type of equipment was formerly known as NCTE.

#### NT12 (NETWORK TERMINATION 1 AND 2)

Combination NT1 and NT2 in same unit.

# NT2 (NETWORK TERMINATION 2)

Customer premises device to fanout a user-to-network (T) interface into multiple T or R interfaces. Concerned with Layer 1, 2, and 3. Examples are a PBX, Key system, LAN, and terminal controller.

# NTACS (Nippon TACS)

A Japanese version of TACS.

# NTIA (NATIONAL TELECOMMUNICATIONS AND INFOR-MATION ADMINISTRATION)

U.S. Government agency responsible for, among other things, administering the use of spectrum allocated for government usage.

# NTSC (NATIONAL TELEVISION STANDARDS COMMITTEE)

# NTT (THE JAPANESE NIPPON TELEPHONE AND TELE-GRAPH CELLULAR SYSTEM)

The Japanese NTT systems are cellular systems operating at 450MHz and 800MHz.

# NX64 kb/S

The use of multiple 64kb/s channels as a single bit stream in digital carrier systems such as T1. This bit stream can be used for a single application like video conferencing or for a single customer. Also called Fractional T1 or FT1.

# OAM&P (OPERATIONS, ADMINISTRATION, MANAGE-MENT AND PROVISIONING)

That portion of the SONET and SDH standards that deals with the administration and management of the networks. The OAM&P standards are still under development.

# OC-n (OPTICAL CARRIER AT LEVEL n)

A multiple of SONET's basic optical speed of 51.84 megabits per second, where n is the multiple. The electrical equivalents are known as Synchronous Transport Signal at Level n (STS-n).

# OCTET

8 Bits grouped together (256 possible combinations) to form a character. CCITT lingo for a byte.

# **ORIGINATE MODEM**

The modem that originates communication in a full-duplex communications system.

# OSI (OPEN SYSTEM INTERCONNECTION REFERENCE MODEL)

International Standards Organization (ISO) model of how data communications systems can be interconnected. Communication is partitioned into seven functional layers. Each layer builds on the service provided by those under it.

# **OUT-OF BAND SIGNALING**

A system that uses a separate communications channel or frequencies outside of voice band for signaling. Digital examples are the ISDN D Channel and common channel signaling.

# **PACKET**

A grouping of data, typically from 1 to 512 characters in size, which usually represents on transaction. A packet is always associated with an address header and control information. The term "Packet" is usually used to refer to a Layer 3 data unit in X.25.

# **PACKET SWITCHING**

A method of transmitting units of data (called packets) through a mesh network. There is no physical circuit established between end points; instead, each packet is relayed from one switching node to the next, and individual packets may take different routes through the switching network.

# **PACKET-MODE TERMINAL**

Data terminal equipment that can format packets and transmit and receive them.

# PAD (PAD ASSEMBLER/DISASSEMBLER)

A PAD assembles packets by buffering asynchronous characters, then emitting them with an address header in

a burst to a packet switched network when 1) the buffer is full, or 2) an end of transaction character such as line feed is encountered, or 3) a timer expires for characters waiting in the buffer to be transmitted. A PAD disassembles packets by receiving them from a packet-switched network, opening them up, and emitting asynchronous characters to the attached non-packet device.

#### **PARITY**

An redundant bit added to each data word in a communication to aid in error detection. All words in the communication have either an even or an odd number of binary 1s.

#### PARITY ERROR

The error that occurs in a DTE when the received data has the wrong parity.

#### **PASSIVE BUS**

A configuration of the ISDN basic interface having up to eight Terminal Equipments (TEs) connected in parallel, each having physical access to the D channel and both B channels. Each TE has a different Terminal Endpoint Identifier (TEI) allowing the switch to individually access them using the point-to-multipoint protocol to LAPD. D channel collisions are resolved by the TE's Level 1 hardware. B channel contention is resolved by the switch using Q.931 messages. There are no active elements in the bus, hence the name.

# PBX (PRIVATE BRANCH EXCHANGE)

A customer premises telephone switch connecting 20 or more station sets to each other, to the public network, and possibly to a private network.

# PCM (PULSE CODE MODULATION)

A digital modulation scheme for representing analog information such as audio or video. To perform PCM, the analog signal is first sampled, and each sample is quantized. The amplitude of each sample is represented by a binary number, which can in turn be sent over a digital communications network.

# PCMCIA (PERSONAL COMPUTER MEMORY CARD INTERNATIONAL ASSOCIATION)

PC Card is the new acronym.

# PCN (PERSONAL COMMUNICATIONS NETWORK)

A generic term for a network supporting Personal Communications Service. Also, sometimes used to refer to the specific implementation of early PCS capabilities in the United Kingdom.

# PCS (PERSONAL COMMUNICATIONS SERVICE (SYSTEM)

A broad range of communications services that enable communications with PERSONS, wherever they are! Personal Communications System refers to the hardware and software providing Personal Communications capabilities.

# PDMA (PHASE DIVISION MULTIPLE ACCESS)

A new radio frequency multiplexing technique in which multiple FM signals share the same frequency division channel by being modulated by carrier signals which are maintained at different phases. Experimental military systems have achieved a 6 to 1 increase in capacity over existing FDMA systems by using carrier signals which are separated in phase by 60 degrees. Most information on PDMA is classified.

# PDN (PUBLIC DATA NETWORK)

A generic term for the collection of networks providing public data services.

# PDS (PREMISES DISTRIBUTION SYSTEM)

AT&T's twisted pair and fiber optic wiring scheme, which is also supported by other vendors including Xerox and Hewlett Packard.

# **PHOTONIC**

Carrying information with photons (light) rather than with electrons (electricity). While photonic transmission has been extremely successful, the information must still be converted into electrons for switching. Research and development projects are striving to switch information directly in photonic form.

# PHS (PERSONAL HANDYPHONE SYSTEM)

A cordless system and digital network that was developed in Japan. PHS uses TDMA and TDD. Each R.F. channel carries four full-duplex bearer channels, and information is transmitted over each R.F. channel at a raw data speed of 384 kilobits per second. Indoors, a PHS mobile telephone works in a manner similar to a conventional cordless telephone. Outside, PHS links with base stations that operate in microcells with ranges from 100 to 500 meters. Hand-offs from cell to cell can take place if the telephone moves through the cells at a walking speed.

# PHYSICAL LAYER

The lowest layer (layer 1) of the OSI Model that defines the physical medium for data communications.

# PL (PRIVATE LINE)

A non-switched communications channel from one location of a customer to another. Leased from an LEC or IEC.

# PLL (PHASE-LOCKED LOOP)

An electronic circuit that consists of a phase detector, low pass filter and voltage controlled oscillator. A PLL can be used as an FSK demodulator.

#### PLMR (PRIVATE LAND MOBILE RADIO)

PLMR Services include SMR and most traditional forms of radio dispatch of vehicles and personnel. PLMR Providers must be used for business communications. Cannot resell services for profit.

# **PLUG-IN MODEM**

A modem built onto a circuit board which plugs into a slot on the motherboard of a terminal or computer.

# PMR (PUBLIC MOBILE RADIO)

Traditional two-way radio, usually push-to-talk, but can be much more sophisticated.

# PN (PSEUDO-RANDOM NOISE)

A noise-like sequence of 1's and 0's, but with a predictable pattern which can be reproduced, provided that certain key information is known.

# POINT-TO-POINT NETWORK

A communications network consisting of a single combinations link that connects two terminals and is not shared by other terminals.

# **POLLING**

The method used on multi-drop communications line operating from a Front End Processor to multiple cluster controllers which keeps more than one from transmitting at the same time. Operates with a roll call, then speak, but only when asked.

# POP (POINT OF PRESENCE)

The physical location in each Local Access Transport Area (LATA) from which an interexchange carrier provides services to the local exchange carrier, and possibly directly to end users.

#### **PORT**

The hardware that permits data to enter or exit a computer, network node, or communications device. Also see communications port.

#### PRA

ISDN primary rate access. See PR1.

# **PRESENTATION LAYER**

Layer 6 of the OSI model. It performs code conversions and data reformatting, formats information for display on the terminal screen and performs data compression and decompression.

# PRI (PRIMARY RATE INTERFACE)

An ISDN User-to-Network Interface (based on T1 Carrier in North America and Japan) consisting of (in North America) twenty-four full duplex channels; twenty-three 64kb/s B Channels and one 64kb/s D Channel (23B+D). The physical medium is two twisted-pairs of wire.

#### **PRIMARY RING**

The data path that normally carries communication on an FDDI network. There is also a secondary ring, which serves as a backup if the primary ring is damaged.

#### **PRIVATE NETWORK**

Used by a single enterprise. Can refer to either Private Voice Networks or Private Data Networks. 1) Private Voice Networks: several PBXs connected together by private lines and/or VPN services. 2) Private Data Networks: often needs only minimal intra-net security and privacy features. Often billing capabilities not needed.

# **PRIVATIZATION**

The process of converting government owned businesses into privately owned companies. Privatization of telecommunications is a major global trend.

#### **PROTOCOL**

In general, any agreement that facilitates communications. In data communications, a public (standard) or private (proprietary) specification for communications between peer layers in a layered architecture.

# **PSEUDOTERNARY CODING**

A form of digital signaling that uses there signal levels to represent binary data. In ISDN, pseudoternary coding represents an binary 1 with no signal level and a binary 0 with alternately positive and negative pulses.

# PSK(PHASE SHIFT KEYING)

A type of phase modulation used by many modems.

# **PSTN** (PUBLIC SWITCHED TELEPHONE NETWORK)

A generic term for the collection of networks providing public telephone switching service.

# PTN (PERSONAL TELEPHONE NUMBER)

A telephone number assigned to a PERSON, rather than to a station or network port.

# PTT (POSTAL TELEPHONE AND TELEGRAPH)

Postal telephone and telegraph. A generic term for European telephone companies, which are generally operated by the country's postal service.

# **PUBLIC NETWORK**

Can be shared by independent and several competing customers. Thus has security and privacy features. Has high availability, reliability. Must offer billing capabilities and interexchange carrier selection. To fit well into telco's networks, equipment must support standard operations support systems, standard transmission equipment, and standard network equipment.

# Q.931(I.451)

Layer 3 protocol for out-of-band message-oriented signaling across user-to-network interface. Originally specified for the D channel of the ISDN Basic Interface (BRI) and Primary Rate Interface (PRI).

# Q.932

Q.931 signaling protocol extensions to add supplementary services. These include custom calling features.

# **QAM (QUADRATURE AMPLITUDE MODULATION)**

A combination of phase-shift keying and amplitude modulation used by high speed modems.

# **QUATERNARY**

A coding scheme that uses four different voltage levels to represent information, used over the local loop with basic ISDN.

# R INTERFACE

Generic interface between non-ISDN station equipment (TE2) and TA.

# RADIO TELEPHONE MOBILE SYSTEM (RTMS)

An analog cellular telephone standard similar to AMPS. RTMS is deployed in Italy.

#### **RADIOCOMM 2000**

One of the analog cellular telephone standards deployed in France.

# RAM (RANDOM ACCESS MEMORY)

The fastest type of computer storage for information.

# RBOC (REGIONAL BELL OPERATING COMPANY)

Local telephone operating companies that were split off from AT&T and which provide most local and interstate telephone services in the US. Also called Bell Operating Companies (BOC).

# RCC (RADIO COMMON CARRIER)

A Common Carrier (i.e. providing services uniformly to all desiring service) for Radio Services.

# RDSS (RADIO DETERMINATION SATELLITE SERVICE)

The use of satellites to do position location of the user.

### **RED BOOKS**

CCITT Recommendations published in 1984.

# REDUNDANT DATA

Data that is not necessary for the information content of a transmission. It is usually added to aide in the detection of communication errors.

# RELP (RESIDUAL-EXCITED LINEAR PREDICTIVE COD-

A method of enhancing LPC coders by determining the error or "residual", between the actual signal and that generated by the basic LPC coder, and transmitting some information about this residual to improve reconstruction of the signal at the receiver.

# **RENEGOTIATION PROTOCOL**

A protocol that enables two modems to negotiate such factors as the communication speed, date compression speed and error correction scheme that they will use to communicate.

#### REPEATER

A device that operates at OSI Model level 1 and connects two smaller LAN segments to form a larger network.

# **RING BACK**

Also known as audible alerting. The tones the calling party hears while the called party's phone is ringing.

# **RING NETWORK**

A network topology that connects its terminals in a loop or ring.

# RISC (REDUCED INSTRUCTION SET COMPUTING)

A computer processing technology in which the microprocessors understand a few simple instructions (when compared to Complex Instruction Set Computing, or CISC), for fast, predictable instruction flow.

# RMTS (THE ITALIAN CELLULAR SYSTEM)

The Italian cellular system, operating at 450MHz, introduced in 1985.

#### ROUTER

A device that connects two or more LANs to each other and that operates at OSI Model layers one through three. A router is able to select among multiple paths to rout a data packet through the network based on an address sent with the data.

# **ROUTING FIELD**

Information that a router adds to a frame to specify the path that the frame should take to travel from the LAN where it originated to the LAN where the destination node is located.

# **ROUTING TABLE**

A table of the addresses of the various nodes on the LANs served by a bridge or other internet working device. The routing table allows frames to be forwarded to the LAN where their destination node is located.

#### **RS-232**

A recommended serial standard that is frequently use to interface a DTE and a DCE.

# RS232C

Collection of specifications defining electrical and mechanical interfaces between terminals, computer, and modems.

#### **RS232C ASYNC**

Common interface for asynchronous terminals up to 19.2kb/s or unofficially faster.

# **RS232C SYNC**

Common interface for synchronous terminals at 9.6kb/s.

# **RS-422**

A recommended standard published by the EIA to specify electrical signal levels of a serial interface. RS-422 uses balanced circuits and it is designed to be used with the RS-449 mechanical specification.

#### **RS-423**

A recommended standard published by the EIA to specify electrical signal levels of a serial interface. RS-423 uses unbalanced circuits and it is designed to be used with the RS-449 mechanical specification.

# RS-449

A recommended standard published by the EIA to specify the functional and mechanical interface between a DTE and a DCE. RS-449 is designed to replace RS-232, but it does not specify the electrical signals.

# RSA (RURAL SERVICE AREA)

The smaller U.S. Cellular markets numbered 307 through 734 as defined by FCC.

# **RUN-LENGTH ENCODING**

A data compression scheme that replaces repeated characters in a data stream with a shorter code. Run-length encoding works well with many types of computer files.

# RTU (RIGHT-TO-USE)

Fee charged for software on switches, STPs, etc. A significant part of the cost of a modern switch.

#### SINTERFACE

ISDN interface between station equipment and NT2.

#### SABRE

The code name for Texas Instrument's ATM physical layer line interface chip, the TDC1500.

# SAPI (SERVICE ACCESS POINT IDENTIFIER)

Address indicator within a given layer of a protocol which identifies the protocol at the next higher layer for which the layer service is begin provided. A common example is LAPD which uses the SAPI field to identify whether the Layer 3 Protocol on ISDN D-channels is X.25 or Q.931.

# SAR (SEGMENTATION AND REASSEMBLY)

An ATM technology that involves dividing information into ATM cells for transmission over the network and reassembling cells into the original data packages at the receivers.

# SCP

A highly-reliable computer and database system which executes Service Logic Programs (SLPs) to provide additional customer services through a switch (SSP). Messages are exchanged with the SSP through the SS7 network.

Since the SCP can be accessed by many switches, it is often used for storage and retrieval of large common data bases, such as for 800 translations and calling card verification

# SDH (SYNCHRONOUS DIGITAL HIERARCHY)

The European and international version of North America's SONET standard for transporting digital information over optical fibers.

# SDL (SPECIFICATION DESCRIPTION LANGUAGE)

 $\ensuremath{\mathsf{CCITT}}$  symbolic language for state diagrams of finite state systems.

# SDLC (SYNCHRONOUS DATA LINK CONTROL)

A bit-oriented, full-duplex Layer 2 protocol invented by IBM. (SDLC was the first of the modern HDLC protocols.) At Layer 2, SNA networks use SDLC between Front End Processors (FEPs) and Cluster Controllers (CCs).

# SDN (SOFTWARE DEFINED NETWORK)

AT&T's name for their Virtual Private Network.

#### SECONDARY RING

A data path that serves as a backup on an FDDI network in case the primary ring is damaged.

# SELECTIVE FORWARDING

The ability of a bridge or other internet working devices to pass from one LAN to another only those frames that are addressed to a node on the output side of the bridge.

#### SELF-HEALING

A feature of an FDDI LAN that permits the nodes on either side of a break in the primary and secondary rings to connect the two rings together to bypass the break. The resulting configuration is sometimes called a ringwrap.

# SEQUENCE CONTROL

A method of numbering blocks of data so that no block will be lost or duplicated and so that the blocks will be placed in proper sequence at the receiver.

# **SERVER**

A computer on a network that serves as a central repository for data and programs and which can be accessed over the network by other computers, which are called clients.

# SESSION LAYER

Layer 5 of the OSI model. It provides a method for data exchange among different software applications and provides a way to recover from major data transfer problems.

# **SETUP MESSAGE**

The most important message in Q.931. Used by both the user and network to hand a call to each other. Specifies all important aspects of a call.

# **SHARED-BANDWIDTH SERVICES**

Common carrier packet-switched wide area networks that charge users only for the amount of information actually transmitted over the network.

#### SHIELDED PAIR

A pair of conductors that are wrapped with metallic foil to isolate the pair from electrical interference.

# SIGN BIT

The first bit in a dibit (group of two bits) in 2 binary, 1 quaternary modulation. The sign bit determines if the voltage level of the transmitted signal is positive or negative. The second bit is the magnitude bit and determines whether the voltage is positive or negative.

# **SIGNALING**

Communication between switches to set-up calls and tear them down. Also includes communication between station sets and switches. Signaling has used dial pulses, then dual tones, now digital messages.

#### **SIM** (SUBSCRIBER IDENTIFICATION MODULE)

A credit-card sized device that belongs to a GSM cellular telephone subscriber. When the subscriber inserts the SIM into a GSM telephone, the network recognizes the telephone as belonging to the subscriber.

# SIMPLEX

One way only communications.

#### SINGLE ATTACH NODE

An FDDI terminal that does not connect to the secondary ring of the network. It is connected to the primary ring by means of a concentrator.

#### SL-1

NT Small Digital PBX. Hardware is often similar to DMS-10.

# **SL-10**

NT Older X.25 Packet Switch.

#### **SL-100**

NT Large Digital PBX. Equipment is often similar to DMS-100.

# SLC (SUBSCRIBER LOOP CARRIER)

AT&T pair gain system. Digital Loop Carrier system.

# SLIC (SUBSCRIBER LINE INTERFACE CIRCUIT)

The telephone company electrical interface between the 2 wire analog copper local loop and the 4 wire (2 for Tx and 2 for Rx) paths in a central office switch.

#### SLOT

A unit of time in a time division multiplexed frame during which a sub-channel bit or character is carried to the other end of the circuit and extracted by the receiving demultiplexer.

# **SMART HIGHWAY**

A term for a range of technologies that is being developed by the U.S. Department of Transportation. The term has not been precisely defined, but it would likely involve radio communication between moving vehicles and roadside computers for the purpose of traffic control.

# SMDS (SWITCHED MULTI-MEGABIT DATA SERVICE)

A high speed packet switched metropolitan area data service that is offered by some telecommunications carriers. The largest use of SMDS is for communication of medical images.

# **SMR** (SPECIALIZED MOBILE RADIO)

A form of private (PLMR) mobile radio services, traditionally providing "dispatch" radio services, but evolving now to cellular-like services.

# SNA (SYSTEMS NETWORK ARCHITECTURE)

IBM's seven layer, vendor specific layered architecture for data communication. Specifies the rules governing interactions between network components in an IBM Environment.

#### SNR (SIGNAL-TO-NOISE RATIO)

The ratio of desired signal level to noise on a communications link, expressed in decibels.

# SONET (SYNCHRONOUS OPTICAL NETWORK)

A data transmission standard for sending high-speed data over a fiber-optic network.

# SPACE

Communications terminology for a binary 0 in a data communication.

# SPECTRUM

A continuous range of frequencies within which signals have some common characteristic.

# SS (SPREAD SPECTRUM)

A radio communications technique that "spreads" the transmitted signal across a wide band of frequencies by constantly shifting its frequency. The receiver must be capable of tracking the signal's frequency changes. Also see direct sequence spread spectrum and frequency hopping spread spectrum

#### STAND-ALONE MODEM

A modem that connects to a terminal by means of an RS-232 or other serial interface.

# **STANDARD**

A specification for data communication that is widely accepted and implemented by communications vendors. Standards may be formal (published by a recognized standards organization) or de facto (accepted without formal publication)

# STAR NETWORK

A network topology with a central hub and a number of remote terminals. Each remote is connected to the hub by a point-to-point network.

# START BIT

A space placed at the beginning of each data word in asynchronous communications.

# STATIC ROUTER

A router whose routing table must be reprogrammed by the network manager every time there is a change made to the network.

# **STATION**

A terminal on the Network.

# STATION EQUIPMENT

All parts of the telephone network that are located on the subscriber's premises including the telset, switchboards and wiring.

# STATISTICAL DELAY

Delay which can only be determined by knowing the probability distributions of some events: Sending a character, Sending a file, File Lengths, etc. The delay is, itself, a probability distribution and is often expressed as "95% of the time the delay will be less than 100 milliseconds."

# STATISTICAL ERROR

Errors, like dropped packets, that are a result of the probability distributions of some event. For example, more than (x) packets in some time interval with the same destination.

#### STOP BIT

A mark placed at the end of each data work in asynchronous communications.

# STORE AND FORWARD

A data communication technique that accepts packets, stores them until they are validated and complete, and then forwards them to the next node on the packet path.

# STP (SS7) (SIGNAL TRANSFER POINT)

High speed, ultra-reliable special purpose packet switch for signaling messages in the SS7 network. Since operation of the entire network depends on them, STPs are installed in mated pairs each in a different location. The interexchange carriers install the two STPs of a mated pair hundreds of miles from each other. Each STP in the mated pair is connected to every switch they directly serve and has sufficient capacity to handle all the signaling traffic should its mate fail.

# STP (WIRE) (SHIELDED TWISTED PAIR)

A pair of wires that is twisted and shielded with metallic foil or braid to minimize interference with and from other pairs, radio stations, etc.

# STS-n (SYNCHRONOUS TRANSPORT SIGNAL AT LEVEL n.)

At the electrical circuit level, a multiple of SONET's basic speed of 51.48 megabits per second. The equivalent optic speeds are known as Optical Carrier at Level n (OC-n).

#### SUBSCRIBER

A customer of a telephone company or other communications carrier.

# SUPERVISORY INFORMATION

Signaling information used to connect, maintain and disconnect a telephone circuit.

# SUPPLEMENTARY SERVICES

Additional services that a telephone company can make available to its subscribers in addition to basic telephone service. Examples include caller identification, call waiting, call rejection and call forwarding.

#### **SWITCH**

Generic term for machines that switch telephone calls from/to telephones and/or trunks. Includes private network machines such as a PBX and public network central office machines such as local exchange switches, tandem switches, toll switches, interexchange carrier switches, and gateway switches.

# **SWITCHED 56 SERVICE**

A switched 56-kilobit-per-second digital telephone service widely offered in North America and regarded as an interim technology until ISDN is in place. Switched 56 uses a 64-kilobit-per-second line, but 8 kilobits per second are reserved for in-channel signaling.

#### SWITCHING EQUIPMENT

Equipment located in the telco offices that makes the interconnection between the station equipment of two or more subscribers.

# SYNCHRONOUS COMMUNICATIONS

A form of communications in which the sending and receiving terminals operate from the same clock signal.

#### SYNCHRONOUS TRANSMISSION

Data communication protocol set where data is sent continuously. The receiver and transmitter are in constant bit synchronization. Character (byte) synchronization is achieved by a Layer 2 Flag character transmitted at the start of each block. Synchronous transmission is normally found on the faster circuits, e.g., rates of 4.8Kb/s and above.

# SYSTEM 75

AT&T medium-size digital PBX.

# **SYSTEM 85**

AT&T large digital PBX.

# T CARRIER (T1 CARRIER)

A transmission system using time division multiplexing to carry 24 digital voice or data channels each at 64kb/s over copper wire. Total speed is 1.544Mb/s which is called DS1. One pair of wire carries the channels in one direction. A second pair of copper wire in another binder group carries the signals in the other direction. Typically, T1 operates on 22 gauge cable requiring repeaters at least every 6000 feet.

# T INTERFACE

ISDN Interface between station equipment and NT1. For the Basic Interface this is a 4 wire connection limited to 1 km.

# T-MUX (T1 MULTIPLEXER)

The equipment which takes multiple various lower rate bit streams and multiplexes them into a single bit stream conforming to the DS1 standard (T1). The multiplexing can be either deterministic or statistical.

# T1(ANSI) (TELEPHONY COMMITTEE)

An ANSI committee open to the industry at large to develop U.S. Standards for telecommunications. Coordinates U.S. Participation in CCITT under auspices of the State Department. Agrees on content of CCITT recommendations to be included in the national standard. Fills gaps where CCITT is slow, ambiguous, has too many options, or doesn't address the issue. Organized into Working Groups on a topic basis. Uses a letter ballot process to establish standards.

# T1C (TI CARRIER C)

T1 Carrier running at the DS1C rate, which is twice the normal speed.

#### T1E1

Subcommittee of ANSI T1 Committee dealing with Network Interfaces.

#### T1M1

Subcommittee of ANSI T1 Committee dealing with Inter-Network Operations, Administration and Maintenance.

# T1Q1

The ANSIT1 Committee that has a general systems engineering responsibility for new study areas. The initial focus is on Personal Communications Service (PCS).

#### T1Q1

Subcommittee of ANSI T1 Committee dealing with Performance.

# T1S1

Subcommittee of ANSI T1 Committee dealing with Services, Architecture, and Signaling.

#### T1X1

Subcommittee of ANSI T1 Committee dealing with Digital Hierarchy and Synchronization,

#### **T1Y1**

Subcommittee of ANSI T1 Committee dealing with Specialized Subjects.

# **T2 CARRIER SYSTEM**

A digital communications link that is formed by multiplexing three T1 systems. North American T2 systems operated at 6.312 megabits per second.

# T3 CARRIER SYSTEM

A digital communications link that is formed by multiplexing seven T2 systems. T3 systems operate at 47.736 megabits per second.

# TA(BC) (TECHNICAL ADVISORY)

Bellcore draft requirements document.

# TA(ISDN) (TERMINAL ADAPTER)

ISDN customer-owned protocol converter. Converts from a standard non-ISDN interfaces (e.g., X.25, RS232) to ISDN S/T interface.

# TACS (TOTAL ACCESS CELLULAR SYSTEM)

The English rough equivalent of AMPS using 25kHz channels at 900MHz. Used in more than 20 countries.

# TCM (TIME COMPRESSION MULTIPLEXING)

A method of providing the appearance of full duplex communication over a single twisted pair half duplex copper loop. Data are buffered at each end and sent across the line at double the subscriber data rate with the two ends taking turns. Also called Ping pong multiplexing.

# TCP/IP (TRANSMISSION CONTROL PROTOCOL/INTERNET PROTOCOL)

A packet oriented communications protocol that was developed with funding from the Defense Advanced Research Projects Agency (DARPA) to link computers across large networks.

# TDM (TIME DIVISION MULTIPLEX)

The usual way digital facilities are deterministically multiplexed.

# TDMA (TIME DIVISION MULTIPLE ACCESS)

A method of multiplexing several digital signals onto the same channel. In cellular telephony, TDMA divides each radio channel into a series of time slots, and each cellular telephone is assigned a specific time slot in a specific radio channel. GSM and IS-136 are two cellular standards that use TDMA. TDMA is sometimes used in the press as a synonym for IS-136 or its predecessor standard, IS-54.

# TDMA-3

IS-54 Time division Multiplexing divides a frequency into 6 time slots. Initial "full-rate" vocoders require 2 time slots per user and thus support 3 users on each frequency. This is called TDMA-3. Future "half-rate" vocoders require only 1 time slot and support 6 users per frequency.

#### TDMA-6

IS-54 Time Division Multiplexing divides a frequency into 6 time slots. Initial "full-rate" vocoders require 2 slots per user and thus support 3 users on each frequency. Future "half-rate" vocoders require only 1 time slot and support 6 users per frequency. This is called TDMA-6.

# TE (TERMINAL EQUIPMENT)

ISDN equipment category including TDMA-6 and TE2s.

# TE1 (TERMINAL EQUIPMENT TYPE 1)

Terminal Equipment meeting ISDN interface specifications such as ISDN phones, ISDN terminals, etc.

# TE2 (TERMINAL EQUIPMENT TYPE 2)

Terminal Equipment providing interfaces other than ISDN, for example, non-ISDN equipment. Needs an appropriate terminal adapter (TA) to connect to ISDN.

# **TELEACTION SERVICE**

An ISDN service that provides telemetry service using slow packet speeds over the ISDN D channel. An example if the remote reading of electrical, water, and gas meters.

# TELEMETRY

Transmission and collection of data obtained by sensing conditions in a real-time environment.

#### **TELEPOINT**

A wireless pay telephone service through strategically placed stations that uses the CT2 cordless telephone standard. Telepoint was installed with much fanfair in the U.K., but the service failed to attract subscribers. Tele-

point service ceased to be offered in that country in 1993. However, there are active Telepoint systems in several Asian countries including China, Malaysia, Hong Kong, Singapore, and Thailand.

#### **TERMINAL**

The device on a network that sends or receives data. A terminal is often a computer.

#### **TERMINAL ADAPTER**

A circuit that permits non-ISDN equipment to be connected to an ISDN line.

#### **TERMINAL PROGRAM**

A communications software package that controls an intelligent modem and performs other communications functions.

#### **TETHERLESS**

Tetherless: Tetherless service is an all-encompassing term that includes the concepts of cordless mobility service, wireless network service plus the ability to roam freely among any wired or wireless network to make or receive calls.

# TIA (TELECOMMUNICATIONS INDUSTRY ASSOCIATION)

The Telecommunications Industry Association responsible for cellular standards in the U.S. Via its TR45 Committee. Will cooperate with T1P1 to set standards for PCS.

# TIME SLOT

Unit of digital time division switching. Normally occurs once every 125 microseconds and contains 8 bits of user data (plus any proprietary bits). Thus carries a DS0.

# TIP/RING

The positive and negative wires of an analog telephone line.

# **TOKEN**

A unique bit pattern that controls which terminal has permission to transmit on a Token Ring network. See token passing.

# **TOKEN PASSING**

A protocol that gives a terminal permission to transmit on a Token Ring LAN. The token circulates around the ring from terminal to terminal. The terminal that processes the token has permission to transmit.

# **TOKEN RING**

A LAN standard, also know as IEEE 802.5, that connects personal computers by means of coaxial cable. Token Ring LANs operate at 4 megabits per second or 16 megabits per second.

# TOPOLOGY

The physical layout of a communications network. Some popular topologies are bus, ring, star, and point-to-point.

# TOTAL ACCESS COMMUNICATIONS SYSTEM

A European analog cellular telephone standard derived from the US AMPS standard. TACS is deployed in Aus-

tria, Ireland, Italy, and the U.K.

# TR (TECHNICAL REQUIREMENT)

Bellcore final reference document.

#### **TRANSMISSION**

The encoding of information and its communication across a communications network.

#### TRANSMISSION EQUIPMENT

Telephone circuits that carry information from one subscriber to another.

#### TRANSPORT DEVICE

A device on a communications network that functions without making its presence known to the end terminals.

# TRANSPARENT TRANSMISSION

A type of transmission used in BISYNC in which the receiving DTE ignores the contents of the text field. Transparent transmission is used to communicate non-text data where a data word in the text field could be confused with a control character.

#### TRANSPORT LAYER

Layer 4 of the OSI model. It defines standards that make the network transparent to the user.

#### **TRUNK**

A communication path between two switches that carries one telephone call. Each digital trunk occupies one DS0.

# **TWISTED PAIR**

Two insulated wires, usually made from copper, that are twisted in a regular, six turns per inch spiral pattern used to connect most telephones. Also used as a medium by several local area networks.

#### TWISTED PAIR FDDI

A new FDDI LAN standard that uses twisted pair wire instead of fiber-optic cable as a communications medium. Twisted pair FDDI is more economical, because it eliminates the expensive interface between each node and the fiber optic cable.

# TWO WIRE CIRCUIT

A communications circuit that uses a single pair of wires for both transmitted and received information.

# **U INTERFACE**

A two-wire interface required by the FCC (not CCITT) between the Local Exchange Carrier and the customer's NT1. Specification completed during 1Q87 by ANSI T1D1.3.

# **UDI** (UNRESTRICTED DIGITAL INFORMATION)

CCITTese for Clear Channel Capability (CCC).

# UMTS (UNIVERSAL MOBILE TELECOMMUNICATIONS SERVICE)

ETSI's term for future mobile and personal wireless access to public network services. Similar to FPLMTS.

# **UNI (USER NETWORK INTERFACE)**

Point of access by the customer to the ISDN (narrowband or broadband) network.

# **UPS** (UNINTERRUPTIBLE POWER SUPPLY)

A powering system which can survive commercial power failures, generally by employing battery backup and/or generators.

# UPT (UNIVERSAL PERSONAL TELECOMMUNICATIONS)

The CCITT term for the network architecture and capabilities to support PCS.

# **UUI (USER-TO-USER INFORMATION)**

- 1) ISDN level 3 capability of passing small amounts of data between two ISDN users via the signaling network. Not a substitute for packet networks, but rather a way to use a small amount of data to improve a circuit switched (usually voice) call. A Network Interconnect issue is: how are revenues from U-to-U signaling shared?
- 2) SS7 Signaling information that is sent directly from one end user to another. It is carried transparently by the network and is not processed nor changed by the network. This includes all the information found in the following Q.931 information elements: Lower Layer Compatibility, Higher Layer compatibility, User-to-User Information; plus parts of the Bearer Capability Information element. These information elements are carried by the Access Transport Parameter and Use to User Information Parameters of user-to-user.

#### V.21

An international 300b/s full duplex FSK modem standard The North American version is Bell 103.

#### **V.22**

An international full duplex 4PSK modem standard that operates at 1200b/s and 600 baud. The North American version is Bell 212A

# **V.22** bis

An international full duplex QAM modem standard that operates at 2400b/s and 600 baud.

#### V.32

An international full duplex QAM modern standard that operates at 9600b/s and 2400 baud.

# **V.32** bis

An international full duplex modem standard that operates at 14,400b/s.

# V.32 TERBO

An interim proprietary modem standard published by AT&T that operates at a speed of 19,200 bits per second.

# V.35

A CCITT standard protocol for transmitting data. Normally run at speeds of 56 or 64Kb/s in the U.S.

# V.42

An error checking standard protocol published by the CCITT that is used for modern communications.

#### V 42 bic

A standard published by the CCITT that adds data compression the V.42 modem communications protocol.

#### V.fas

An interim modem standard that was used in 28,800 modems before the V.34 standard was finalized.

#### **V REFERENCE POINT**

An ISDN electrical reference point in the telephone company central office switch that is located between the line termination (LT) and the exchange termination (ET).

# VDSL (VERY-HIGH-BIT-RATE DIGITAL SUBSCRIBER LINE)

A proposed service that would provide a multi-megabit digital service to small businesses and homes over 2-wire lines.

# VIDEO DIAL TONE

Generally, any service designed to deliver video programs to consumers in their residences on demand. An example would be ADSL (Asymmetrical Digital Subscriber Line) which would provide video over telephone lines.

#### VIRTUAL CONNECTION

A data path between two terminals that performs as if the two devices were connected directly to each other, although in reality they are not connected.

# VIRTUAL POP (VIRTUAL POINT OF PRESENCE)

A Point of Presence (POP) which a carrier uses to price a service or calculate mileage, but which may not actually contain the equipment providing the service. The carrier uses internal private lines to carry the information to the office containing the equipment. Often refereed to as "backhaul".

# VOCODER

A technical term formed by combining the words "voice" and "encoder". A vocoder encodes and analog voice signal into a digital format.

# **VPN** (VIRTUAL PRIVATE NETWORK)

Uses information stored in the signaling network regarding customer configuration and dialing plans to allow the use of public network facilities as if they were dedicated to a specific private network. Usually includes special billing arrangements, company specific dialing plans and some limited end-to-end feature transparency.

# VSELP (VECTOR-SUM EXCITED LINEAR PREDICTIVE CODING)

A method of enhancing Linear Predictive Coders using a combination of a limited number of different excitations (sum of excitation vectors).

# **WANDER**

Long term timing deviation.

# WARC (WORLD ADMINISTRATIVE RADIO CONFERENCE)

A World Conference called by the CCIR to get international agreement on Spectrum Allocation. Most recent meeting was February, 1992, in Spain.

# WDM (WAVELENGTH DIVISION MULTIPLEXING)

A transmission technique in which two or more signals are sent through a fiber, driven by lasers at different wavelengths.

# WIRELESS CABLE

A communications system that delivers video programming to subscribers over microwave radio links. From the consumer point of view, see Multipoint Distribution Service.

# WLL (WIRELESS LOCAL LOOP)

Any method of using wireless communication in place of a wired connection to provide subscribers with standard telephone service. WLL is cheaper and faster to install than a wired telephone infrastructure, especially in areas where present telephone service is primitive or nonexistent.

# X.25

CCITT recommendation specifying how user equipment (DTE) is to connect to a public, packet-switched network (DCE). Specifies Layer 1, 2, and 3 Protocols.

# X.75' (PRIME)

Bellcore standard to allow connection of packet switches from difference manufacturers into a single logical X.25 packet network.

# M APPOTE

No. AN9667 February 1997

Harris Telecom

# Selecting the Proper Ring Trip Filter Capacitor (C<sub>2</sub>) for the HC5509B and HC5524 SLICs

Author: Don LaFontaine

# Introduction

The selection of the ring trip filter capacitor is critical to prevent a false ring trip and provide the removal of the AC ring signal once the subscriber goes off-hook. Ring trip is defined as the detection of an off-hook condition (subscriber answers the phone) during ringing. False ring trip can occur if the value of  $\mathbf{C}_2$  is too small for a given systems line noise and amplitude of the AC ringing voltage. System requirements dictate the removal of the AC ring signal within the specified time once the subscriber has gone off-hook. This time limit can be exceeded if the value of  $\mathbf{C}_2$  is too big. The solution is to make  $\mathbf{C}_2$  large enough to prevent false ring trip and yet small enough to provide removal of the ringing signal within the specified system timing requirements.

This application note will discuss the basic operation of the ring trip circuitry and provide the design equations for the ring trip filter. The results of this analysis are presented in a single graph (Figure 4) that will allow easy selection of the capacitor as a function of the AC loop current.

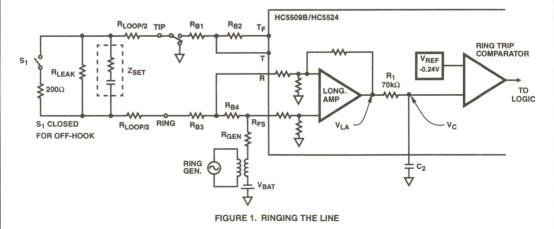
# Operation of the Ring Trip Circuitry

Ring trip is the detection of an off-hook condition during ringing. The off-hook status of a subscriber during ringing is detected by the flow of a DC current. This DC current flows from ground (tip in Figure 1) through the loop resistors

R<sub>LOOP</sub>, S<sub>1</sub>, 200 $\Omega$ , R<sub>B3</sub>, R<sub>B4</sub>, R<sub>GEN</sub>, to V<sub>BAT</sub> when the phone goes off-hook. The HC5509B and HC5524 use an internal difference amplifier (called the longitudinal amplifier) to detect the off-hook DC loop current. This DC current flows in the presence of the AC ringing current if the system is ringing the line. The output of the longitudinal amplifier is a voltage that is proportional to both the AC and DC currents. When ringing a line while the set is on-hook, the line is AC coupled and the output of the longitudinal amplifier is an AC voltage that is centered around a built in offset of about -100mV. When ringing a line while the set is off-hook, both AC and DC currents flow. The output of the longitudinal amplifier (V<sub>LA</sub>) is an AC voltage riding on an exponentially increasing negative DC voltage (see Figure 2).

Figure 2 illustrates the condition when the subscriber goes off-hook while the line is being rung. The DC ring current flows in the direction to cause  $V_{LA}$  to go negative. This in turn causes the external capacitor  $C_2$  to charge to a negative voltage. The voltage at  $C_2$  is compared to an internal threshold that when exceeded, directs the SLIC to stop ringing the line by means of the external ring relay.

If the impedance seen by the ring generator when ringing the line is small enough, the AC current that flows in the line would cause the output of the longitudinal amplifier to exceed the threshold value and cause a false ring trip to occur. Therefore, it is necessary to filter the AC ring signal



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prior to it being fed back to the Ring Trip comparator. Thus in a typical line card application, an external lowpass filter is formed by the internal  $\rm R_1$  resistor and the external  $\rm C_2$  capacitor to attenuate the AC ringing signal while maintaining a DC path so the off-hook condition can be detected.

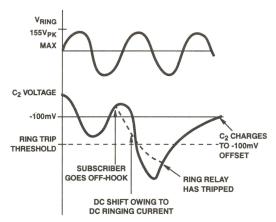


FIGURE 2. OFF-HOOK VOLTAGE ON C2 DURING RINGING

# Ring Trip Filter Design Equations

The minimum ring trip filter attenuation (e.g. largest permissible output level) is determined by the conditions causing the on-hook AC ring signal to be its largest and specifying the filter's maximum output to be below the detector's threshold. The conditions causing the maximum on-hook ring signal are minimum loop length, maximum number of phones connected to the 2W line (lowest line impedance) and maximum ring generator level. These conditions result in the largest on-hook AC ringing current. The maximum level of the on-hook AC ring signal at the comparator input C<sub>2</sub> needs to be less than the threshold value of -0.24V to prevent false ring-trip.

The minimum on-hook loop impedance is:

$$Z_{LOOPMIN} = 100 + R_{(GEN)} + Z_{SETS}$$
 (EQ. 1)

 $Z_{LOOPMIN}$  is the series combination of the following: the  $50\Omega+50\Omega$  feed resistance in the Ring lead;  $R_{GEN}$ , the ring generator source resistance; and  $Z_{SETS}$ , the resultant on-hook impedance of the phone(s) connected in parallel to the line

Using Z<sub>LOOPMIN</sub>, the maximum on-hook AC ringing current can be found as:

$$I_{ONACMAX} = \frac{V_{RINGMAX} \times \sqrt{2}}{|Z_{LOOPMIN}|}$$
 (EQ. 2)

 $I_{\mbox{ONACMAX}}$  is the worst case on-hook AC current in the 2W loop and  $V_{\mbox{RINGMAX}}$  is the largest value of the system's ring generator.

The following analysis is based on the user determining their maximum on-hook AC current. From this, the correct C<sub>2</sub> capacitor value to prevent false ring trip and meet the systems requirements of removing the ring signal is easily determined.

**On-Hook Calculations** (Determining the value for C<sub>2</sub> to prevent false ring trip).

Figure 3 shows the basic one pole RC ring trip filter. The only variable is the external capacitor  $C_2.$  The resistor  $R_1$  can vary anywhere between  $70k\Omega$  and  $110k\Omega.$  This analysis assumes the worst case value of  $70k\Omega$  for the AC ring trip detect threshold calculation and  $110k\Omega$  for the time to trip calculation.

Equation 3 is the voltage divider equation for the ring trip filter for the on-hook condition. The frequency of the ringer is assumed to be 20Hz.

$$V_{C} = \left(\frac{\frac{1}{j\omega C_{2}}}{R_{1} + \frac{1}{j\omega C_{2}}}\right) V_{LA} = \left(\frac{1}{1 + j\omega C_{2}R_{1}}\right) V_{LA}$$
 (EQ. 3)

Where  $V_{LA}$  is the output of the longitudinal amplifier and is equal to:

$$V_{LA} = I_{ONACMAX}(50\Omega)(A_{LA}) = 12.5(I_{ONACMAX})-V_{OFFSET}$$
(EQ. 4)

A<sub>LA</sub> equals 0.25 and is the gain of the longitudinal amplifier. V<sub>OFFSET</sub> equals -100mV and is the offset voltage of the Longitudinal amplifiers output.

The ring trip filter voltage (V<sub>C</sub>) is given in Equation 5.

$$V_{C} = \left(\frac{1}{1 + 40\pi C_2 R_1}\right) ((-12.5)(I_{ONACMAX})) - V_{OFFSET}$$
 (EQ. 5)

Rearranging terms and solving for C yields Equation 6.

$$C_2 = \left(\frac{-12.5(I_{ONACMAX})}{40\pi R_1(V_C + V_{OFFSET})}\right) - \frac{1}{40\pi R_1}$$
 (EQ. 6)

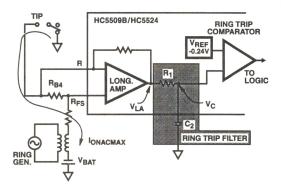


FIGURE 3. ON-HOOK AC VOLTAGE ON C2 DURING RINGING

From Equation 6, the  $C_2$  capacitor value to insure no false ring trip can be calculated. This is accomplished by setting  $V_C$  equal to -0.24V and  $V_{OFFSET}$  equal to -100mV. Quadrant 1 of Figure 4 gives the required capacitor value for a given maximum AC current ( $I_{ONACMAX}$ ).

Off-Hook Calculations (Determining the time to trip for removal of the ring signal).

The total response for the RC filter is given in Equations 7 to 10.

Total<sub>RESPONSE</sub> = 
$$V_{FORCED} + V_{NATURAL} = V_1 + Ae^{\frac{-T_1}{RC}}$$
 (EQ. 7)

Solving for the variable A, when t = 0

$$A = V_{FORCED} - V_{OFFSET} = 12.5(I_{ONDCMAX}) - V_{OFFSET}$$
(EQ. 8)

Where:

 $V_{FORCED} = I_{ONDCMAX}(50\Omega)(A_{LA}) = 12.5(I_{ONDCMAX})$  (EQ. 9)

$$T_{R} = (-12.5)(I_{ONDCMAX}) + (12.5(I_{ONDCMAX}) - V_{OFFSET})e^{\frac{-t}{RC}}$$
(EQ. 10)

Rearranging terms and solving for time yields Equation 11.

$$t = (R)(C) ln \frac{V_C + 12.5(I_{ONDCMAX})}{12.5(I_{ONDCMAX}) - V_{OFFSET}}$$
(EQ. 11)

From Equation 11, the time to trip can be calculated. The results for several capacitor values and DC ring currents are shown in quadrant four of Figure 4.

# Determining the Proper C<sub>2</sub> Capacitor Value for a Given AC Ringing Current

The procedure for selecting the proper ring trip filter capacitor value is as simple as determining your maximum AC ringing current. Once the maximum AC ring current is determined, the ring trip filter capacitor value (to insure no false ring trips) is found on the X axis in quadrant 1 of Figure 1. The second step is to verify that this capacitor value selected does not cause the ring trip detect time to exceed the systems requirements. This is accomplished by determining the worse case DC ring current. Once the maximum DC current is determined, the ring trip detect time is found on the Y axis in quadrant 4 of Figure 4.

# Example 1:

Suppose the following system design requirements are given:

Max Battery = -52V

 $R_{LOOP}$  ACMax = 2.33k $\Omega$  (3 REN)

 $R_{FFFD} = 100\Omega$  total

Ring Generator Voltage = 90V<sub>RMS</sub>

 $R_{I,OOP}$  DC Max = 1700 $\Omega$  (including  $R_{SFT}$ )

 $R(GEN) = 300\Omega$ 

 $R(phone) = 600\Omega$ 

$$I_{ONACMAX} = \frac{90V_{RMS} \times \sqrt{2}}{Z_{I,OOPMIN}} = \frac{127.7}{2.43k\Omega} = 52.37mA$$
 (EQ. 12)

Where:

$$Z_{LOOPMIN} = 2(R_{FEED}) + R(GEN) + Z_{SET} + R_{LOOPLENGTH}$$
(EQ. 13)

Assuming worst case: RFEED = 100 $\Omega$ , R(GEN) = 0 $\Omega$ , Z<sub>SET</sub> = 2.33k $\Omega$  and R<sub>I OOP</sub> length = 0 $\Omega$ 

From Figure 4 quadrant 1 the capacitor value for  $I_{ONACMAX}$  equal to 52.37mA is  $0.39\mu F$ . The next highest standard value is  $0.47\mu F$ . The  $0.4\mu F$  capacitor is 17% higher than the minimum value suggested in Figure 4. Therefore to account for capacitor tolerance a  $0.47\mu F$  10% is recommended in this case.

Verification of the time for ring trip detection requires the worse case I<sub>OFFDCMIN</sub> ring current:

$$I_{OFFDCMIN} = \frac{V_{BAT}}{Z_{LOOPMAX}} = \frac{52}{2.6k\Omega} = 20mA$$
 (EQ. 14)

where:

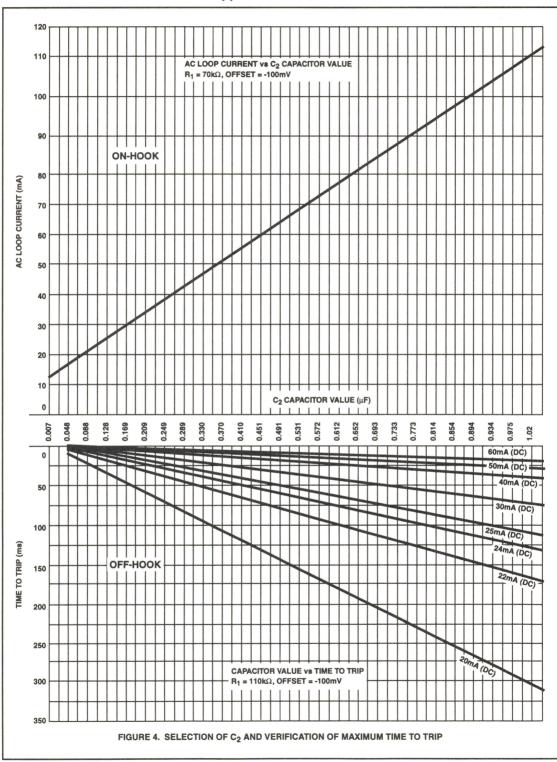
$$Z_{LOOPMAX} = 2(R_{FEED}) + R(GEN) + R(phone) + R_{LOOPLENGTH}$$
(EQ. 15)

Assuming worst case:  $R_{FEED} = 100\Omega$ ,  $R(GEN) = 300\Omega$ ,  $R(phone) = 600\Omega$  and  $R_{I,OOP}$  length = 1700 $\Omega$ .

From Figure 4 quadrant 4, the time to trip with a DC ring current of 20mA is about 145ms. If the systems time to trip requirement is greater than this, your selection of  $C_2$  is a good one.

#### Example 2:

Following the same procedure as above, if the worse case  $I_{ONACMAX}=110$ mA ( $V_{RINGMAX}=120V_{RMS}$ , 5 Ren load) from quadrant 1 of Figure 4  $V_{C}=1.02\mu F$ . Note, although Figure 4 indicates using a bigger value of capacitor that a 1.0 $\mu F$ , our lab tests indicate that our figure is very conservative at the higher AC currents and that a 1.0 $\mu F$  capacitor is more then sufficient to prevent false tripping. And if the minimum DC loop current was 24mA the time to trip would be 140ms.



# APPLICATIONS FOR COMMUNICATION ICs

## 5

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### **An Introduction to Digital Filters**

Authors: Dr. David B. Chester, Geoff Phillips, Stan Zepp

#### Introduction

Digital Signal Processing (DSP) affords greater flexibility, higher performance (in terms of attenuation and selectivity), better time and environment stability and lower equipment production costs than traditional analog techniques. Additionally, more and more microprocessor circuitry is being displaced with cost-effective DSP techniques and products: an example of this is the emergence of DSP in cellular base stations. Components available today let DSP extend from baseband to intermediate frequencies (IFs). This makes DSP useful for tuning and signal selectivity, and frequency up and down conversion.

These new DSP applications result from advances in digital filtering. This Application Note will overview digital filtering by addressing concepts which can be extended to baseband processing on programmable digital signal processors.

#### Essentials of Digital Filtering

A digital filter is simply a discrete-time, discrete-amplitude convolver. An example is shown in Figure 1 for three-bit amplitude quantization. Basic Fourier transform theory states that the linear convolution of two sequences in the time domain is the same as multiplication of two corresponding spectral sequences in the frequency domain. Filtering is in essence the multiplication of the signal spectrum by the frequency domain impulse response of the filter. For an ideal lowpass filter the pass band part of the signal spectrum is multiplied by one and the stopband part of the signal by zero.

## Analog Filters, Software-Based and Hardwired Digital Filters

Owing to the way that analog and digital filters are physically implemented, an analog filter is inherently more size- and power-efficient, although more component-sensitive, than its digital counterpart - if it can be implemented in a straightforward manner. In general, as signal frequency increases, the disparity in efficiency increases.

Characteristics of applications where digital filters are more size and power efficient than analog filters are: linear phase, very high stop band attenuation, very low pass band ripple; the filter's response must be programmable or adaptive; the filter must manipulate phase and; very low shape factors (a digital filter's shape factor is the ratio of the filter's pass band width plus the filter's transition band width to the filter's pass band width).

General-purpose digital signal microprocessors, now commodity devices, are used in a broad range of applications and can implement moderately complex digital filters in the audio frequency range. Many standard signal processing algorithms, including digital filters, are available in software packages from digital signal processor and third party vendors. As a result, software development costs are trivial when amortized over production quantities.

The architectures of digital signal microprocessors are usually optimized to perform a sum-of-products calculation with data from RAM or ROM. They are not optimized for any specific DSP function. However, to get extended sampling rate performance from a digital filter requires hardware designed to perform the intended filter function at the desired sampling frequencies.

For example, Harris Semiconductor offers a family of standard digital filter products with several others in development. Some hardware-specific digital filters can now sample at rates approaching 75 Megasamples per second (MSPS). Higher performance is possible for high volume applications by limiting the range of parameters. Standard filter products strike a balance between optimized filter architectures and programmability by offering a line of configurable filters. That is, these products are function-specific, with optimized architectures and programmable parameters.

#### **Conceptual Differences**

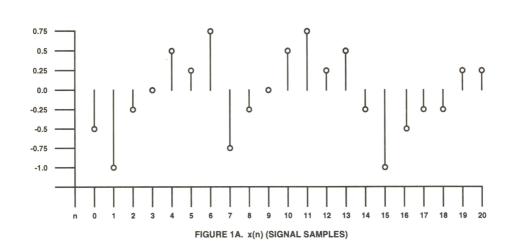
#### Frequency-Domain Versus Time Domain Thinking

Thinking about analog filters, most engineers are comfortable in the time domain. For example, the operation of an RC lowpass filter can easily be envisioned as a capacitor charging and discharging through a resistor. Likewise, it is easy to envision how a negative-feedback active filter uses phase shift as a function of frequency, which is a time domain operation.

A digital filter is better conceptualized in the frequency domain. The filter implementation simply performs a convolution of the time domain impulse response and the sampled signal. A filter is designed with a frequency domain impulse response which is as close to the desired ideal response as can be generated given the constraints of the implementation. The frequency domain impulse response is then transformed into a time domain impulse response which is converted to the coefficients of the filter.

5

STANDARD PRODUCTS



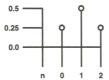


FIGURE 1B. h(n) (FILTER IMPULSE RESPONSE SAMPLES)

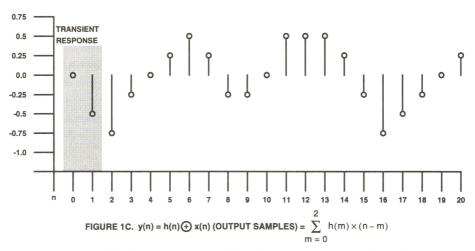


FIGURE 1. THE DISCRETE TIME AND DISCRETE AMPLITUDE CONVOLUTION OF h(n) WITH x(n)

#### **Mathematics Versus Physics**

The characteristics of an analog filter are directly attributable to the physics of the device that implements it. In contrast, the characteristics of a digital filter are only indirectly attributable to the physics of the device that implements it.

A digital filter's passband ripple, shape factor, stopband attenuation, and phase characteristics are all functions of the order and type of polynomial used to approximate the ideal impulse response, the number of bits used in performing the arithmetic, and the type of architecture used to implement the arithmetic. Actual frequencies have no meaning in a digital filter except in their relation to the sampling frequency. This is because the impulse response is generated as a function of z<sup>-1</sup>, the sample interval (the time between samples). For a smaller shape factor, the order of the filter and the number of bits in the arithmetic can be increased. The only physical limitation is the amount of arithmetic processing that can be integrated on a device or devices given the filter order and the input sampling rate.

#### Digital Filter Types

There are two basic types of digital filters, finite impulse response (FIR) and infinite impulse response (IIR) filters. The general form of the digital filter difference equation is

$$y(n) = \sum_{i=0}^{N} a_{i}x(n-i) - \sum_{i=1}^{N} b_{i}y(n-i)$$

where y(n) is the current filter output, the y(n-i)'s are previous filter outputs, the x(n-i)'s are current or previous filter inputs, the a<sub>i</sub>'s are the filter's feed forward coefficients corresponding to the zeros of the filter, the b<sub>i</sub>'s are the filter's feedback coefficients corresponding to the poles of the filter, and N is the filter's order. IIR filters have one or more non-zero feedback coefficients. That is, as a result of the feedback term, if the filter has one or more poles, once the filter has been excited with an impulse there is always an output. FIR filters have no non-zero feedback coefficient. That is, the filter has only zeros, and once it has been excited with an impulse the output is present for only a finite (N) number of computational cycles.

Figures 2 and 3 show common IIR architectures. Figures 4 through 6 show common FIR architectures.

#### Strengths and Weaknesses

Because an IIR filter uses both a feed-forward polynomial (zeros as the roots) and a feedback polynomial (poles as the roots), it has a much sharper transition characteristic for a given filter order. Like analog filters with poles, an IIR filter usually has nonlinear phase characteristics. Also, the feedback loop makes IIR filters difficult to use in adaptive filter applications.

Due to its all zero structure, the FIR filter has a linear phase response when the filter's coefficients are symmetric, as is the case in most standard filtering applications. An FIR's implementation noise characteristics are easy to model,

especially if no intermediate truncation is used. In this common implementation, the noise floor is at - 6.02 B + 6.02  $\log_2$ NdB where B is the number of actual bits used in the filter's coefficient quantization and N is again the filter order. This is why most Harris filter ICs have more coefficient bits than data bits.

An IIR filter's poles may be close to or outside the unit circle in the Z plane. This means an IIR filter may have stability problems, especially after quantization is applied. An FIR filter is always stable. FIR filters also allow development of computationally efficient architectures in decimating or interpolating applications, which will be described in more detail later.

#### Filter Response Design Methods

The total specification of the ideal filter includes the location of passbands and stopbands, the minimum stopband attenuation, the maximum passband ripple, the filter order, and perhaps the shape of the response in some of the specified bands.

Typically, there are three stages to the design of digital filter responses for passband filters. First, the ideal filter response is specified. Next, a floating point response is designed. Finally, the floating point coefficients are quantized to yield a fixed point response.

Creating a floating-point IIR filter response starts with a prototype analog filter. Then an s-domain to z-domain transformation is used to generate a set of digital filter coefficients. Common methods of designing floating-point FIR filter responses are windowing, frequency sampling, and optimal. All are described in general digital signal processing texts and are standard in most commercially available digital filter design software packages.

Converting floating-point coefficients into fixed-point coefficients requires quantizing the coefficients and calculating the frequency domain impulse response of the filter or filter model to verify that the filter meets the required specification. If it does not, either the number of coefficient bits can be increased, the filter response can be redefined and step two repeated, or the filter arithmetic can be redesigned, or a combination of these procedures can be performed. When filter hardware is at a premium, sophisticated simulated annealing techniques can be used for both fixed-point FIR and IIR filters to produce the best set of filter coefficients, given a fixed filter order and coefficient width.

#### **Decimation and Interpolation**

Decimation (Figure 7) is reducing the output sampling rate by ignoring all but every Mth sample. When a digital filter reduces the bandwidth of a signal of interest so the filter output is over-sampled if the input sample rate is preserved, it is inefficient to compute outputs that will be ignored in the decimation process. Thus, there is a one-to-one correspondence between decimation rate and gain in computational efficiency. However, this computational efficiency can not be fully realized in an IIR filter because the feedback path must be computed for every input cycle.

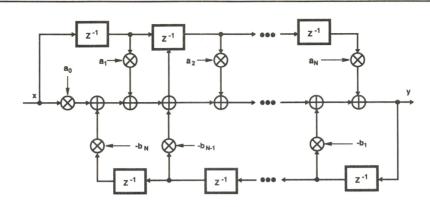


FIGURE 2. IIR FILTER DIRECT FORM 1

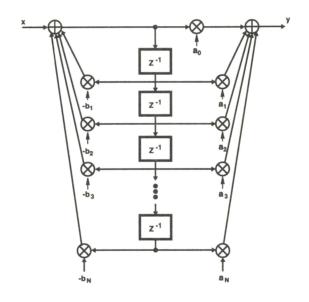


FIGURE 3. IIR FILTER DIRECT FORM 2

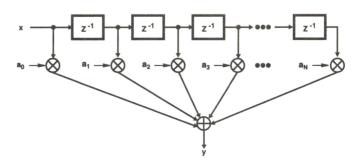


FIGURE 4. TRANSVERSAL IMPLEMENTATION OF AN FIR FILTER

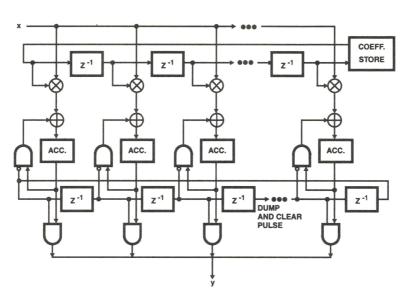


FIGURE 5. PARALLEL MULTIPLIER/ACCUMULATOR CELL FIR FILTER IMPLEMENTATION

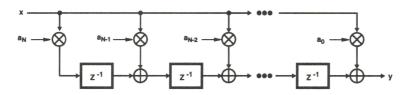


FIGURE 6. TRANSPOSED FIR FILTER IMPLEMENTATION

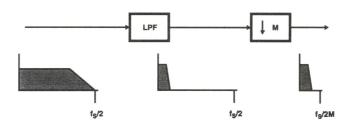


FIGURE 7. BLOCK DIAGRAM AND SPECTRAL REPRESENTATION OF THE DECIMATION PROCESS

Interpolation (Figure 8) means increasing the sampling rate. It is most often used when a narrowband signal will be combined with a signal that requires a higher sampling rate. Conceptually, the first step in interpolation is to stuff L-1 zero-valued samples between each valid input sample, expanding the sampling rate by L, and causing the original signal spectrum to be repeated L-1 times. To perform the actual interpolation, the zero-valued input samples must be converted to approximations of signal samples. This is equivalent to preserving the original signal spectrum. Effectively, the zero-stuffed input stream is filtered by a lowpass filter with a pass band at the original spectrum location. This filters out all of the repeated spectra.

In FIR filters, interpolation computational efficiency is possible because only every Lth data value is non zero and thus requires an actual multiply-add operation. Consequently, there is a one-to-one correspondence between interpolation rate and gain in computational efficiency. The efficient interpolation structure is called polyphase. Again, because of the feedback loop in an IIR filter, this computational efficiency can not be realized.

#### Hardware Versus Software

There is no difference between the mathematics and filter response design of a hardware versus a software implementation of a digital filter. The only differences lie in the implementation architectures.

#### **Optimal Architectures**

A digital filter implemented in software is typically run on a processor with a single computational element. This forces the filter to be implemented in a serial sum-of-products. An FIR is implemented as a single sum-of-products and an IIR is typically a sum of products for the feed-forward section and another sum-of-products for the feedback section.

Hardware can be optimized for each application. Low speed and low power can be achieved using a bit-serial implementation. Moderate speed and power may call for a single parallel multiplier-accumulator. High speed applications can utilize multiplier multiplier-accumulator structures with specialized memory address schemes. Decimating or interpolating filters can use optimized polyphase structures, multiple stages and specialized memory addressing schemes. Coefficient memory can be designed to take advantage of coefficient characteristics and accumulators can be custom-designed to take advantage of unity gain properties.

#### Speed/Flexibility Tradeoffs

When a digital filter is hard-wired for one specific task, its performance can be optimized because there is no control overhead associated with reconfiguring the IC.

Even with a hard-wired filter, however, some degree of flexibility can be achieved without sacrificing much computational efficiency. For example, an FIR filter with programmable coefficients and filter order and a limited selectable decimation rate requires only a modified memory and memory addresser added to a fixed FIR filter.

Harris Semiconductor's line of standard digital filtering devices focuses on reconfigurable function-specific devices. The standard products are specialized FIR filters; IIR filter implementations are limited to application-specific designs. Most of the Harris standard filters have programmable decimation rates. Some can interpolate. Most have programmable coefficients and filter orders and some provide up/or down-conversion.

#### General Applications

Traditionally, most digital filter applications have been limited to audio and high-end image processing. With advances in process technologies and digital signal processing methodologies, digital filters are now cost-effective in the IF range and in almost all video markets.

Digital filters are commonly used for audio frequencies for two reasons. First, digital filters for audio are superior in price and performance to the analog alternative. Second, audio analog-to-digital converters (A/Ds) and digital-to-analog converters (DACs) can be manufactured with high accuracy and are available at low cost. Thus, the combined cost of filtering and conversion (if necessary) is low. The cost trades are much more difficult in the 1MHz to 100MHz signal range, such as the IF ranges of many radio receivers.

While digital signal processing technology can now produce cost effective digital filters for IF, the cost or even the availability of data conversion products are limiting factors. Many IF digital filtering applications are band-limiting and decimating. In these cases the design engineer must not only know digital filters, but also understand the effects of narrow-band-filtering processing-gain on A/D requirements. Additionally, power dissipation must be considered. Currently, digital IF filter solutions are excluded from low power applications such as personal communication devices. In contrast, audio frequency digital filters are essential.

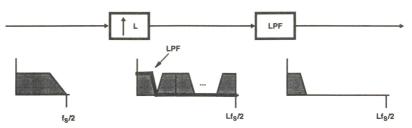


FIGURE 8. BLOCK DIAGRAM AND SPECTRAL REPRESENTATION OF THE INTERPOLATION PROCESS

#### IF Processing

Harris' HSP43216 Halfband Filter IC (Figure 9) can perform a quadrature split on a real signal. In this example, the input signal undergoes anti-alias filtering and is digitized and passed to the Halfband Filter IC. The quadrature f<sub>S</sub>/4 local oscillator (LO) and mixer circuits on the IC center the upper sideband of the real signal spectrum at DC. The Halfband Filter itself operates on the resultant complex signal to filter out the lower sideband, forming a quadrature signal (a characteristic of which is a single-sided spectrum). Other circuits in the IC then decimate the real and imaginary output by two to eliminate the unused spectral region.

To cite a more specific application, IF processing can be implemented in a cellular base station using the HSP50016 Digital Down Converter (DDC) and two HSP43124 Serial I/O Filters (Figure 10). In this example a 4MHz band of the GSM spectrum has already been mixed to a near baseband IF, has been appropriately anti-alias filtered, and digitized by an A/D. The spectral plot makes the point that aliasing may take place as long as it does not encroach on the band of interest.

Because this is a channelizing application, there is a signal-to-noise ratio (SNR) processing gain of 3dB for every factor of 2 that the noise bandwidth is reduced. In this example, the processing gain is approximately 17dB. As a result, the SNR

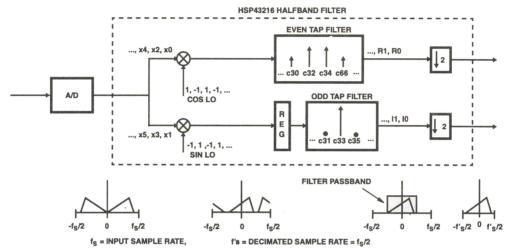


FIGURE 9. REAL TO QUADRATURE CONVERSION USING THE HSP43216 HALFBAND FILTER

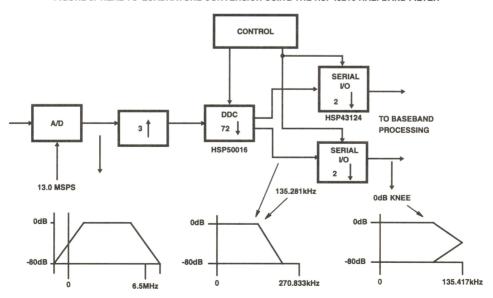


FIGURE 10. GSM BASE STATION EXAMPLE

of the A/D can be 17dB lower than the desired output SNR. The A/D's spurious free dynamic range (SFDR), however, must be equal to the desired output SFDR since there is no gain effect on in-band frequency spurs.

The DDC is a single-chip quadrature down-converter and two stage filter. It is used to tune the channel of interest to baseband, and to perform narrow-band filtering and decimation. The Serial I/O Filters are used to apply the GSM filter shape to the output quadrature data stream. This process includes decimation by two to modify the output sampling rate to that required by the GSM specification. This requirement forces the DDC to decimate at a rate below its minimum of 64 in quadrature-output mode. This is dealt with by placing a three-times sample rate expander in front of the DDC. The HSP50016 and HSP43216 data sheets provide greater detail.

#### **Application-Specific Architectures**

As can be seen in the example above, while reconfigurable function-specific digital filters provide viable solutions to specific applications, they may not be cost-effective in high volumes (Annual quantities in the 10 to 100 thousand range). This is where application-specific architectures play a role. In high volume applications, reconfigurable function-specific digital filters can be used initially for prototyping and refining an efficient architecture. Then, that architecture can be implemented in an application-specific device. In most cases, because of the sophisticated nature of digital filters, efficient architectures are likely to require semicustom or custom designs.

#### Imaging/Video Systems With Separable Dimensions

Most digital signal processing applications involving filter operations on two-dimensional data assume that the horizontal and vertical filtering operations can be separated. That is, (Figure 11) the image data can be filtered in one dimension (for example, the horizontal or row dimension) followed by filtering in the other dimension (the vertical or column dimension). This separability greatly simplifies the filter design compared to a two-dimensional filter.

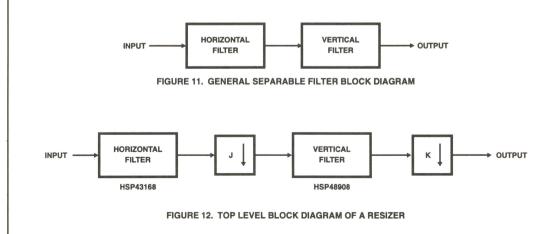
#### One- and Two-Dimensional Filters

One-dimensional DSP operations are widely used in imaging or video systems to perform down-conversion or filtering. In video, purely one-dimensional operations are almost always in the horizontal dimension because this is the dimension in which video is sampled in real time.

Two-dimensional operations are used primarily to alter the size and shape of the image or to filter in two dimensions. The latter operations include highpass filters, to sharpen edges in all directions, or lowpass filters, to limit high-frequency noise or to deliberately soften edges. An important case is image resizing, where the input image is resampled to a different sized output image. In reducing the image size, filtering is needed because simply down-sampling (throwing away pixels) vertically and horizontally produces unacceptable aliasing. A two-dimensional filter can be made from one-dimensional filters (Figure 12). Here, an HSP43168 Dual FIR Filter provides horizontal band-limiting prior to horizontal down-sampling. Its multi-rate capabilities allow it to perform the entire decimation operation. Then a HSP48908 Two-Dimensional Convolver is used as a three-coefficient vertical filter to reduce vertical bandwidth prior to vertical down-sampling.

#### **Row and Column Filters**

In terms of algorithms, there is no basic difference between row and column digital filters. The implementation difference is that horizontal filters have delay elements of z<sup>-1</sup> and vertical filters, while they have the same structure, are implemented with delay elements of z<sup>-L</sup>, where L is the line length in pixels. The importance of this is that vertical line delays (z<sup>-L</sup>) are more costly than horizontal sample delays, because lines are hundreds of pixels long. The result is that in low cost implementations, vertical filter functions tend to be very rudimentary (three coefficients or less) or nonexistent. Note that although vertical filters operate on pixels widely separated in time, they are still required to produce a new output at the horizontal pixel rate because new sets of inputs are presented at the horizontal rate.



#### **Video Applications**

A video A/D, for example the Harris HI5702, may sample the signal at twice the required sampling rate to ease analog anti-aliasing filter requirements. This would be followed by a halfband filter similar to the HSP43216 for decimation by two (Figure 13). To understand the usefulness of this operation, assume the required output rate is 13.5 MSPS (a CCIR 601 standard rate). With 4.5MHz input video bandwidth, the required anti-aliasing filter cutoff with a 13.5 MSPS sampling rate is 6.75MHz. This requires a filter shape factor of 6.75/ 4.5 = 1.5. If 2:1 oversampling is followed by a digital halfband filter with a decimation rate of 2, the required shape factor of the anti-aliasing filter is 13.5/4.5 = 3.0. Given the generally stringent passband requirements on video filters, this is a much more cost-effective solution than the more severe analog anti-aliasing filter. It allows the analog filter design to concentrate on passband performance rather than a sharp transition.

Another area that relies extensively on one-dimensional digital filtering techniques is NTSC or PAL decoding, which require operations like chroma/luma separation filters, quadrature down-conversion of the chroma information and chroma decimation by two filtering.

#### Conclusion

This application note has presented a brief overview of digital filtering and has highlighted the similarities and differences of filters implemented in software on general purpose digital microprocessors, in function-specific hardware, and in application specific hardware. Digital filter characteristics and performance have been compared to analog filters. Applications of high performance Harris function-specific digital filters in IF and Video signal processing were illustrated as examples of cost effective uses of digital filters with high throughput rates.

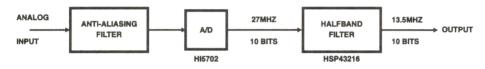


FIGURE 13. TOP LEVEL BLOCK DIAGRAM OF AN OVERSAMPLER TO REDUCE ANTI-ALIASING FILTER REQUIREMENTS



No. AN9657.1 May 1997

## Harris Digital Signal Processing

### **Data Conversion Binary Code Formats**

Author: John Henkelman

#### Introduction

Many of the Harris DSP products have selectable data formats for their input/output interfaces. Table 1 defines the codes as used in these interfaces. Because many applications involve conversion of the analog signals, the analog scale is given as a reference. This table should clarify the interface of the DSP parts to the data conversion device.

Table 1 also helps users understand the basis for each of these formats. The following definitions are offered as the basis for each code format:

Offset Binary: A binary code in which the code represents analog values between Full Scale and -Full Scale. All zero corresponds to -Full Scale. This code can be balanced by appending a 1 below the LSB.

2's Complement: A binary code in which positive and negative codes of the same magnitude sum to all zero's plus a

carry. The 2's complement can be generated from the Offset Binary code by inverting the MSB. A negative number is generated by inverting each bit of the positive number, then adding one.

Example:  $011 (+3) \rightarrow 100 + 1 = 101 (-3)$ 

1's Complement: Bipolar binary code in which positive and negative codes of the same magnitude sum to all one's. A negative number is generated by investing each bit of the positive number.

Example: 011 (+3)  $\rightarrow$  100 (-3)

**Sign Magnitude:** A binary code in which the MSB represents positive (1) and negative (0) polarities. The code in the table uses a offset binary code to represent the magnitude portion of the number.

TABLE 1. BINARY DATA FORMATS FOR DATA CONVERSION

SCALE	OFFSET BINARY	2'S COMPLEMENT	1'S COMPLEMENT	SIGN MAGNITUDE
+Full Scale	11111111	01111111	01111111	11111111
+0.75 Full Scale	11100000	01100000	01100000	11100000
+0.5 Full Scale	11000000	01000000	01000000	11000000
+0.25 Full Scale	10100000	00100000	00100000	10100000
+0	10000000	00000000	00000000	10000000
-0			11111111	00000000
-0.25 Full Scale	01100000	11100000	11011111	00100000
-0.5 Full Scale	01000000	11000000	10111111	01000000
-0.75 Full Scale	00100000	10100000	10011111	01100000
-Full Scale + 1 LSB	00000001	10000001	10000000	01111111
-Full Scale	00000000	10000000		

As an example, let's plot a cosine wave in each of the data formats. Assume that full scale is  $\pm 1\,\text{V}$ . Table 2 details the values of the sampled sinusoid in each of the data formats. Fig-

ures 1 through 4 illustrate these signals when converted back to analog using an offset binary converter.

TABLE 2. SAMPLED COSINE SIGNAL REPRESENTATION

n	COS(nπT/16)	OFFSET BINARY	2'S COMPLEMENT	1'S COMPLEMENT	SIGN MAGNITUDE
0	1	11111	01111	01111	11111
1	0.980785	11111	01111	01111	11111
2	0.92388	11110	01110	01110	11110
3	0.83147	11100	01100	01100	11100
4	0.707107	11010	01010	01010	11010
5	0.55557	11000	01000	01000	11000
6	0.382683	10101	00101	00101	10101
7	0.19509	10010	00010	00010	10010
8	0	10000	00000	00000	10000
9	-0.19509	01100	11100	11101	00010
10	-0.38268	01001	11001	11010	00101
11	-0.55557	00110	10110	10111	01000
12	-0.70711	00100	10100	10101	01010
13	-0.83147	00010	10010	10011	01100
14	-0.92388	00001	10001	10001	01110
15	-0.98079	00000	10000	10000	01111
16	-1	00000	10000	10000	01111
17	-0.98079	00000	10000	10000	01111
18	-0.92388	00001	10001	10001	01110
19	-0.83147	00010	10010	10011	01100
20	-0.70711	00100	10100	10101	01010
21	-0.55557	00110	10110	10111	01000
22	-0.38268	01001	11001	11010	00101
23	-0.19509	01100	11100	11101	00010
24	0	10000	00000	00000	10000
25	0.19509	10010	00010	00010	10010
26	0.382683	10101	00101	00101	10101
27	0.55557	11000	01000	01000	11000
28	0.707107	11010	01010	01010	11010
29	0.83147	11100	01100	01100	11100
30	0.92388	11110	01110	01110	11110
31	0.980785	11111	01111	01111	11111
32	1	11111	01111	01111	11111

#### Data Conversion Binary Code Formats

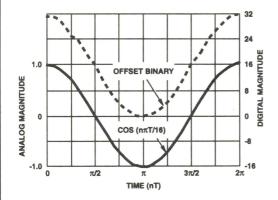


FIGURE 1. OFFSET BINARY CODE PLOTTING  $\cos(nT)$ 

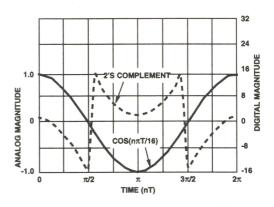
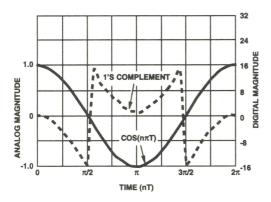


FIGURE 2. 2'S COMPLEMENT BINARY CODE PLOTTING COS(nT) †





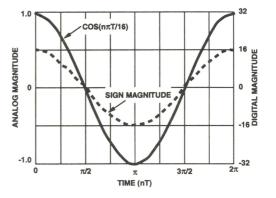


FIGURE 4. SIGN MAGNITUDE/OFFSET BINARY CODE PLOTTING COS(nT)  $\dagger$ 

<sup>†</sup> Note that the solid line denotes the regular cosine wave and the dashed line denotes the plot of the digital format code, connected to decimal.

No. AN9658 January 1997

## Digital Signal Processing

## Implementation of a High Rate Radio Receiver (HSP43124, HSP43168, HSP43216, HSP50110, HSP50210)

Authors: John Henkelman and David Damerow

#### Features

- Modulation Formats: BPSK, QPSK, SQPSK, 8-PSK, FM, FSK
- Symbol Rates: To 22.5 MSPS (4 Samples/Symbol)
- Programmable: Reconfigurable to Data Rate, Modulation Format, and Order/Type of Tracking Loop
- Digital: Repeatable Performance Over Temperature and Time
- High Performance Reception: Bit Error Rate Approaches Less Than 0.5dB From Theory

## TABLE 3. HARRIS DSP PRODUCTS FOR HIGH RATE DIGITAL RADIO RECEIVERS

FUNCTIONAL BLOCK	HARRIS PART
VCA	Analog Discrete
140MHz Quadrature Output 6-Bit A/D Converter (8-Bit A/D Converter)	HI3086JCQ, CXA3086Q (HI3026JCQ, HI3026AJCQ)
Decimating Filter	HSP43216 Halfband Filter
Digital DownConverter	HSP50110 Digital Quadrature Tuner
Matched Filter	HSP43168 Dual FIR Filter
Carrier & Symbol Tracking Loops	HSP50210 Digital Costas Loop
AGC Loop Filter	Analog Discrete

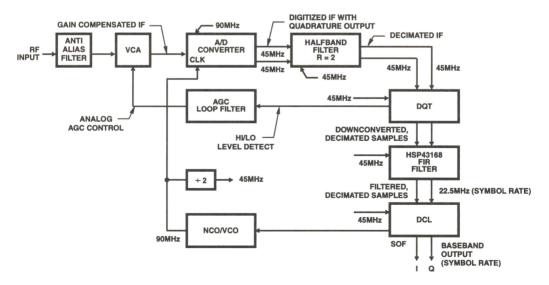


FIGURE 5. BLOCK DIAGRAM OF A HIGH RATE DIGITAL RADIO RECEIVER

#### Introduction

The present HSP50110/210EVAL board provides capabilities for evaluating received modulated signals with symbol rates up to 2.5 MSPS. This high end limit on symbol rate is based on 20 samples per symbol. Many applications do not require such a large number of samples per symbol, and can still use the HSP50110/210EVAL evaluation board to breadboard and test these applications. Two limitations come into play as higher rates are implemented with this evaluation board:

- 1.The Serial FIR Filter maximum clock rate is (45MHz/10 bits) = 4.5MHz.
- The transport delay, or propagation delay in the loop causing loop instability for input rates above 4.5MHz.

It is these limitations that prompts the presentation of a high symbol rate receiver implementation using the HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL) chip set. Figure 1. illustrates a high rate receiver configuration using the DQT and DCL demod parts. This implementation will be offered as the design solution, after the design considerations and trades have been presented.

#### High Rate Design Concerns

The primary limitations on a high speed design are the maximum operating speed of the digital parts and the bandwidth and resolution on the A/D converter. These key parameters are listed for the parts that will be configured for our high rate receiver design.

Maximum Clock Speed of HSP43216: . . . . . . . . . 52MHz

Maximum Clock Speed of HSP50110:	52MHz
Maximum Clock Speed of HSP43168:	45MHz
Maximum Quadrature A/D	
Conversion Speed:	140 MSPS with 6 Bits
	120 MSPS with 8 Bits
Minimum Number Samples	

..... 4 Samples/Symbol

#### Selecting An A/D Converter

per Symbol . . . . . . . . .

The design begins with selecting a high speed, wide bandwidth, high resolution D/A converter. Devices exist that output dual demultiplexed data samples at half the sample rate. This relaxes the maximum clock rate of the following devices by 2. Such a device is the HI3086JCQ Harris A/D. It is a 6-bit 140 MSPS Flash A/D Converter with quadrature output samples. (The HI3026 A/D, an 8-bit 120 MSPS device with dual demultiplexed output is also a design candidate.) Subsequent DSP parts could operate up to a 70MHz maximum clock rate if the HI3086 is used.

#### Selecting The DSP Sample Rate

#### The Clock Rate Criterion

Selecting 4 samples per symbol yields the desired bandwidth. This sets the rate at which the HSP50110 Digital Quadrature Tuner will output symbol data. We can construct a DSP processing chain from this baseline symbol rate. The clock rate of the IF signal into the HSP50110 Digital Quadra-

ture Tuner is set to be four times the symbol rate. By using an HSP43216 Halfband Filter in the Downconvert and Decimate mode (INT/EXT# = 0), the dual channel demultiplexed sampled data from the A/D can be input at four times the symbol rate. By noting that the A/D outputs 2 synchronous samples at half the A/D sample clock rate, the A/D sample rate is effectively four times the symbol rate.

The Re-Sampler in the DQT eliminates the need for the sample clock and the symbol rate to be exact integer related. (An even integer is used as an example for clarity and to yield a "ball park" solution for applications with non integer relationships.) Note that an external NCO is used to drive the A/D clock port. This minimizes the clocking jitter in the system. Use of the DQT Re-Sample NCO in addition to a separate clock generator for the A/D and halfband will inherently have more jitter than the configuration shown. The DQT is used in the complex input mode.

#### **Determining the DSP System Limiting Rate**

The next limiting clock DSP element is the Halfband Filter which has a maximum clock rate at 52MHz. The rate through this decimating filter part can be optimized by using it in the Downconvert and Decimate Mode (INT/EXT# = 0). This allows dual (demultiplexed) inputs at the maximum clock rate. This sets the maximum system sustainable clock rate at the output of the A/D converter at 52MHz per data stream. The maximum system sustainable A/D input sample clock becomes twice the A/D output clock, or 104MHz. The decimate by two HalfBand filter output becomes a quadrature data stream at 52MHz and the symbol rate is one half of this, or 26MHz (2 samples on I, 2 samples on Q = 4 samples per symbol).

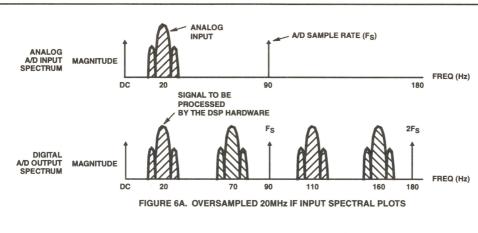
#### System Design Considerations

## Frequency Domain Considerations for the A/D Sample Rate

Determining the appropriate A/D sample rate, requires more than just consideration of the clocking criterion of the DSP parts. The frequency plan of the receive system must compliment the digitizing hardware and not produce alias components that will impede the ability to recover the signal of interest. Thus it is equally important that the sample rate be selected in a location relative to the IF signal, in a way that will not cause alias signals to fall in band. Many applications use undersampling techniques to recover signals from IF carriers by locating a harmonic of the sample frequency at a strategic distance from the IF signal. An alias of the high frequency IF carrier is then processed by the DSP hardware.

Figure 2A and 2B illustrate two examples of how a 90MHz A/D sample clock can be used to downconvert and process modulated IF signals. Figure 2A shows an oversampled 20MHz IF, while Figure 2B shows an undersampled 160MHz IF.

Figure 3 illustrates the spectral development at several points in the data path in the block diagram, from IF input to baseband output. The example has  $F_S' = F_S/2$  (Decimate by 2) in the HBF and  $F_S'' = F_S'/8$  (Decimate by 8) in the DCL.



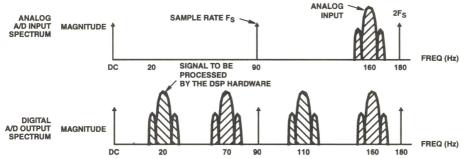
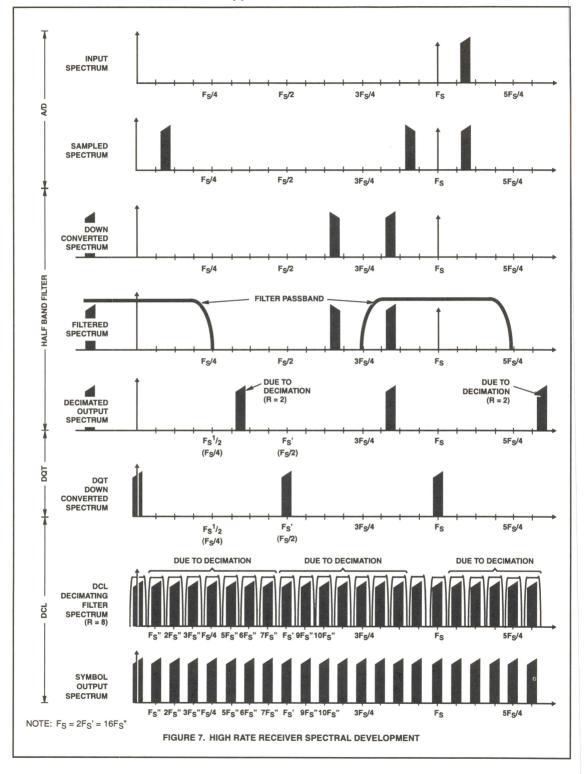


FIGURE 6B. UNDERSAMPLED 120MHz IF INPUT SPECTRAL PLOTS

Additionally it is insufficient to just consider the signals of interest. Those signals that fall in the band of the A/D converter, must be removed by any anti-aliasing filters ahead of the A/D converter. These in band signals; if not filtered out, will also alias around the clock frequency and may appear directly on top of the signal of interest. In example B of Figure 2, a 70MHz signal will interfere in such a way. The anti alias filter should be designed to attenuate the undesired signals to the point that it prevents such signal degradation. Note that an important system trade is the implementation of the anti-alias filter and the selection of the A/D clock frequency.



#### **Matched Baseband Filter Requirements**

The final receiver design consideration is the construction of a matched baseband filter for the received signal. The DQT/DCL chipset offers two filters integral to the chip: 1) Integrate and Dump and 2) Square Root of Raised Cosine  $\alpha$  = 0.4. If one of these filters meets your system performance requirements, then no further design is required.

If your application requires a different filter, the HSP43168 or the HSP43124 can be inserted between the DQT and the DCL. The serial I/O filter (HSP43124) is limited to CLK = (45MHz/bit width). The Dual FIR filter (HSP43168) is limited to CLK = 45MHz. These parts may become the limiting factor for the maximum clock speed. This translates to an A/D sample rate at 90MHz, an A/D dual demultiplexed data output rate of 45MHz, a Halfband Filter dual data Output Rate of 45MHz, and a symbol rate of 22.5MHz. In general, filtering requirements may demand that greater than eight taps be used in the filter, and two HSP43168 chips may be required (one for I, one for Q) for adequate shaping.

#### Summary

Figure 1 outlines the implementation of the high symbol rate receiver. The solution assumes the need for an application specific matched filter, limiting the symbol rate to 22.5MHz. Key elements of the design are: the anti-alias filter, the quadrature output A/D converter, the dual input decimating Halfband Filter, the Digital Quadrature Tuner and the Digital Costas loop. The design uses the level detection feature of the HSP50110 to drive a Voltage Controlled Attenuator to keep the level at the converter input at an optimum value.

For information relative to setting the internal PLL parameters in the DQT/DCL chipset, refer to the HSP50110/210 EVAL Users Manual.



No. AN9659

January 1997

## Digital Signal Processing

## Using the HSP50110/210EVAL Example Configuration Files

Authors: John Henkelman and David Damerow

#### Introduction

Every HSP50110/210EVAL evaluation kit contains a floppy disk labeled DEMOD CHIPSET EVALUATION SOFTWARE. This disk contains the DEMODEVB.EXE file and other software necessary to configure and operate the evaluation card which is provided in the demod chipset kit. This kit provides all the software required for the configuration, operation and evaluation of the HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL). Additional software is provided to demonstrate the various filtering features of the evaluation board. The software provided in the kit ensures that a user can quickly set up the evaluation board, configure it, and output data for test evaluation. This Evaluation Kit will leave the user confident that these parts can be easily ported into an application specific design. Four directories (folders) are provided to assist in familiarizing the evaluator with key features of the chipset. These four directories are labeled "examples", "filters", "schemat" and "serinade" are provided for this purpose.

#### The "EXAMPLES" Folder

The first directory is filled with example configuration files which have been tested and proven to provide BER performance that is better than 1dB from theory. It is the use of these example configuration files that is the focus of this application note. This application note will detail the location, use and application of the example configuration files. The quickest way to configure the evaluation board for your application, is to find a configuration file that most closely matches your symbol rate, and load that file. The file can then be edited to change any of the parameters (such as IF frequency, Filtering, etc.) as needed.

Figures 1A and 1B detail the test Hardware configurations used to verify the BER performance of each configuration file. A study of these figures reveals that Figure 1A utilizes a 70MHz IF, while Figure 1B utilizes a 5MHz IF. These are the only two IF frequencies that will be found in the example files.

#### The "FILTERS" Folder

This folder contains example FIR filter configuration files. These files have been created with SERINADE, a software package developed for Harris Semiconductor to assist in the design of digital filters of the type found on the evaluation board. This application note will provide information on the description, and use of these filter files.

#### The "SCHEMAT" Folder

This folder contains the schematic of the evaluation board, as captured using the ORCAD application. The files are provided for design re-use and should help shorten the critical "Time to Market" development time. These schematics, which were used to generate the evaluation board, are offered for use in designs, it is the user's responsibility to secure the proper ORCAD revision and any ORCAD technical assistance in porting, opening and editing these schematics.

#### The "SERINADE" Folder

This folder contains the latest version of the SERINADE software. This software will assist in any application specific FIR filter design. The "filters" folder contains examples of filters already designed using this software; and should be used to verify results until the user is proficient with the application. All SERINADE generated filters are readily ported into a format that the HSP50110/210EVAL kit can import.

It is highly recommended that the distribution disk provided in the evaluation kit be backed up prior to use. Obtain a printout of the files in the "EXAMPLES" and "FILTERS" and use it to maintain a fully functional software package.

#### The "EXAMPLE" Configuration Files

The example configuration files included on the distribution disk are labeled according to the key shown below and in Appendix H of the User's Manual. The first field is an alphanumeric digit which indicates the modulation type. Options are: B for BPSK, Q for QPSK, and E for 8PSK. In the future F will be used to denote FSK, while M will denote MSK.



The second field is numeric and represents the symbol, or baud rate of the signal, expressed in KHz. The symbol rate numeric field utilizes a "p" to represent a decimal point. For example, a data rate of 1200bps is represented as 1p2. Similarly 9600bps is expressed as 9p6.

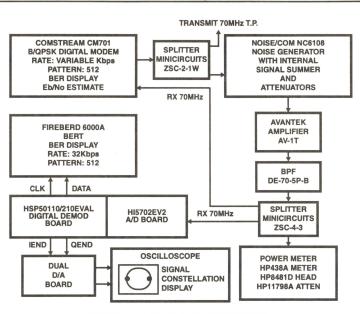


FIGURE 1A. 70MHz IF TEST CONFIGURATION

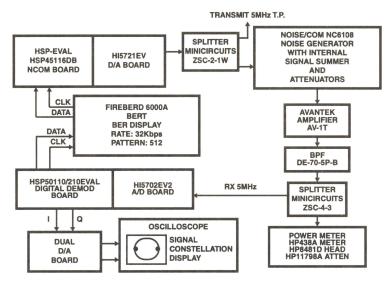


FIGURE 1B. 5MHz TEST CONFIGURATION

Care must be taken not to confuse symbol rate with data rate. Recall that for BPSK, data rate and symbol rate are identical. For QPSK, however, the symbol rate is 1/2 the data rate, because two bits of data are used to form a symbol. For 8PSK the symbol rate is 1/3 the data rate, because three bits of data are used to form a symbol. Figure 2 details how a typical QPSK modulator is implemented, while Figure 3 illustrates the data to quadrature symbol relationship for QPSK for both the

in-phase and quadrature components. Two data bits will determine in which of four phase states the carrier will be placed: 0<sup>0</sup>, 90<sup>0</sup>, 180<sup>0</sup>, or 270<sup>0</sup>. This phase shift is accomplished using the I (in-phase) and (Q) quadrature orthogonal vectors as shown in Figure 4. Figure 5 illustrates the data and symbol relationship for 8PSK, while Figure 6 shows the possible carrier vectors created for a symbol.

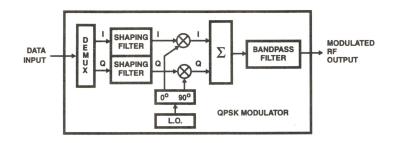


FIGURE 2. TYPICAL QPSK MODULATOR

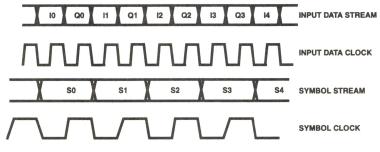


FIGURE 3. DATA TO SYMBOL RELATIONSHIP FOR QPSK

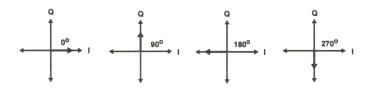


FIGURE 4. VECTOR REPRESENTATIONS OF THE QPSK SYMBOLS CREATED FROM TWO DATA BITS

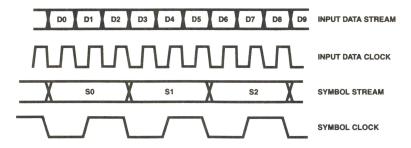


FIGURE 5. DATA TO SYMBOL RELATIONSHIPS FOR 8PSK MODULATION

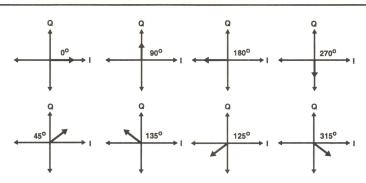


FIGURE 6. VECTOR REPRESENTATIONS OF THE 8PSK SYMBOLS CREATED FROM THREE DATA BITS

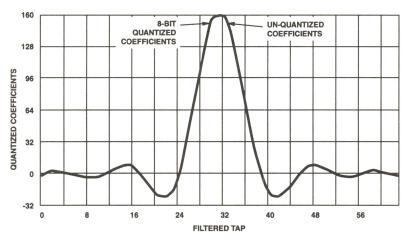


FIGURE 7. COEFICIENTS FOR THE SQUARE ROOT OF RAISED COSINE  $\alpha$  = 0.4 FILTER

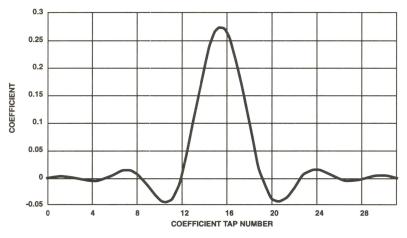


FIGURE 8. COEFFICIENTS FOR THE b128fir.cfg CONFIGURATION FILE FILTER: rrc4a4x.imp

The final field of the file name is the filter type. The options are RRC for Square Root of Raised Cosine  $\alpha=0.4$  filtering (for bandlimited applications), I&D for Integrate and Dump filtering (for unfiltered data applications), and FIR filtering (for creating application specific onboard serial FIR filters). Figure 7 details the coefficients of the RRC Cosine  $\alpha=0.4$  filter. The FIR selection implies that the DCL RCC and I&D filters are bypassed. In this case the file represents the coefficients for the FIR filter. Figure 8 details the coefficients for the FIR filter in example configuration file. Table 1 lists the configuration files provided as examples with the EVAL kit and details the modulation format, data rate and filtering associated with each file.

When using the "fir" filter configuration, the FIR filter coefficient file that is used can be changed. Figure 8 illustrates that the Data Path/Modulation Menu Item (14) must be selected and changed from "0" (Bypassed) to "1" (enabled). After selecting "1", the user is prompted for the file name of the filter. The software will automatically append a ".rpt" suffix to the file name, indicating a SERINADE generated file, so do not enter a suffix with your file name. A number of example FIR filter files have been included on the distribution disk in the kit under the FILTERS directory, for the evaluation of a variety of Square Root of Raised Cosine filters. The files with the ".imp" suffix are files ready to import into SERINADE. The SERINADE FIR filter design software is included on the evaluation kit distribution disk, allowing the user to create files for specific applications. The files with the ".rpt" and ".ser" suffixes are generated by SERINADE. The HSP50110/210EVAL software uses the files with the ".rpt" suffix. Table 2 defines the available FIR filter coefficient files.

#### HSP50110/210 Evaluation Board Software

Current File Name \R128BBC

#### DATA PATH/MODULATION MENU

Current File Name.\B128RRC	
(1) Master Clock Freq 40000000Hz	<u>.</u>
(2) Input Sample Rate 40000000Hz	
(3) Input Mode Gated	1
(4) DQT Input Samples	l
(5) DQT Input Format Offset Bin	1
(6) L.O. Center Freq +5000000 Hz	_
(7) Data Modulation	
(8) Baud Rate	
(9) DQT Output Rate	۷.
(10) I.F. NBW750000Hz	٠.
(11) DQT Filter CIC w/Comp	)
(12) DCL RRC Filter Enabled	ı
(13) DCL I&D Bypassed	ı
(14) HSD43124 Byrngesed	_
(14) 113743124bypassed	
(15) Es/No (min) +0dB	
	3
(15) Es/No (min)+0dB	3
(15) Es/No (min). +0dB (16) Es/No (max. +100dB	3
(15) Es/No (min).       +0dB         (16) Es/No (max.       +100dB         (17) Es/No (design)       +6dB	3
(15) Es/No (min).       +0dB         (16) Es/No (max.       +100dB         (17) Es/No (design)       +6dB         (18) A/D backoff (min.)       12dB	3 3 3 3 3
(15) Es/No (min).       +0dE         (16) Es/No (max.       +100dE         (17) Es/No (design)       +6dE         (18) A/D backoff (min.)       12dE         (19) A/D backoff (max.)       18dE	3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
(15) Es/No (min).       +0dE         (16) Es/No (max.       +100dE         (17) Es/No (design)       +6dE         (18) A/D backoff (min.)       12dE         (19) A/D backoff (max.)       18dE         (20) DCL Output Vector       -6dBFS	3 3 3 3 5 5 6 6 6 6 6 6 6 6 6 6 6 6 6 6
(15) Es/No (min).       +0dE         (16) Es/No (max.       +100dB         (17) Es/No (design)       +6dE         (18) A/D backoff (min.)       12dE         (19) A/D backoff (max.)       18dB         (20) DCL Output Vector       -6dBFS         (21) DQT Output Level       -12dBFS         (22) DCL Detect. Level       -12dBFS         (23) Slicer Threshold       0.25	3 3 3 3 5 5 5 5
(15) Es/No (min).       +0dE         (16) Es/No (max.       +100dB         (17) Es/No (design).       +6dE         (18) A/D backoff (min.).       12dB         (19) A/D backoff (max.)       18dB         (20) DCL Output Vector.       -6dBFS         (21) DQT Output Level.       -12dBFS         (22) DCL Detect. Level       -12dBFS         (23) Slicer Threshold       0.25         (24) DQT AGC Slew Rate       30dB/sec	
(15) Es/No (min).       +0dE         (16) Es/No (max.       +100dB         (17) Es/No (design)       +6dE         (18) A/D backoff (min.)       12dE         (19) A/D backoff (max.)       18dB         (20) DCL Output Vector       -6dBFS         (21) DQT Output Level       -12dBFS         (22) DCL Detect. Level       -12dBFS         (23) Slicer Threshold       0.25	
(15) Es/No (min).       +0dE         (16) Es/No (max.       +100dB         (17) Es/No (design)       +6dB         (18) A/D backoff (min.)       12dB         (19) A/D backoff (max.)       18dB         (20) DCL Output Vector       -6dBFS         (21) DQT Output Level       -12dBFS         (22) DCL Detect. Level       -12dBFS         (23) Slicer Threshold       0.25         (24) DQT AGC Slew Rate       30dB/sec         (25) DCL AGC Slew Rate       10dB/sec         (26) AGC Limits       FULL RANGE	
(15) Es/No (min).       +0dE         (16) Es/No (max.       +100dB         (17) Es/No (design)       +6dE         (18) A/D backoff (min.)       12dB         (19) A/D backoff (max.)       18dB         (20) DCL Output Vector       -6dBFS         (21) DQT Output Level.       -12dBFS         (22) DCL Detect. Level       -12dBFS         (23) Slicer Threshold       0.25         (24) DQT AGC Slew Rate       30dB/sec         (25) DCL AGC Slew Rate       10dB/sec         (26) AGC Limits       FULL RANGE         (27) Output Mux Control       7	
(15) Es/No (min).       +0dE         (16) Es/No (max.       +100dB         (17) Es/No (design)       +6dB         (18) A/D backoff (min.)       12dB         (19) A/D backoff (max.)       18dB         (20) DCL Output Vector       -6dBFS         (21) DQT Output Level       -12dBFS         (22) DCL Detect. Level       -12dBFS         (23) Slicer Threshold       0.25         (24) DQT AGC Slew Rate       30dB/sec         (25) DCL AGC Slew Rate       10dB/sec         (26) AGC Limits       FULL RANGE	

FIGURE 9. DATA PATH/MODULATION MENU ITEM (14) IS USED TO SELECT THE ONBOARD SERIAL FIR FILTERS

**TABLE 1. EXAMPLE CONFIGURATION FILE DEFINITIONS** 

	MODULATION SYMBOL RATE DATA RATE				
NO.	FILE NAME	FORMAT	(KSps)	(KBps)	FILTER TYPE
1	b1024rrc.cfg	BPSK	1024	1024	Square Root of Raised Cosine
2	b128fir.cfg	BPSK	128	128	Serial FIR
3	b128i&d.cfg	BPSK	128	128	Integrate and Dump
4	b128rrc.cfg	BPSK	128	128	Square Root of Raised Cosine
5	b19p2i&d.cfg	BPSK	19.2	19.2	Integrate and Dump
6	b1p23i&d.cfg	BPSK	1.23	1.23	Integrate and Dump
7	b1p2i&d.cfg	BPSK	1.2	1.2	Integrate and Dump
8	b256rrc.cfg	BPSK	256	256	Square Root of Raised Cosine
9	b2.4i&d.cfg	BPSK	2.4	2.4	Integrate and Dump
10	b32i&d.cfg	BPSK	32	32	Integrate and Dump
11	b32rrc.cfg	BPSK	32	32	Square Root of Raised Cosine
12	b4p8i&d.cfg	BPSK	4.8	4.8	Integrate and Dump
13	b512rrc.cfg	BPSK	512	512	Square Root of Raised Cosine
14	b64i&d.cfg	BPSK	64	64	Integrate and Dump
15	b64rrc.cfg	BPSK	64	64	Square Root of Raised Cosine
16	b9p6i&d.cfg	BPSK	9.6	9.6	Integrate and Dump
17	q1024rrc.cfg	QPSK	1024	2048	Square Root of Raised Cosine
18	q128i&d.cfg	QPSK	128	256	Integrate and Dump
19	q128rrc.cfg	QPSK	128	256	Square Root of Raised Cosine
20	q1544rrc.cfg	QPSK	1544	3088	Square Root of Raised Cosine
21	q2048rrc.cfg	QPSK	2048	4096	Square Root of Raised Cosine
22	q256rrc.cfg	QPSK	256	512	Square Root of Raised Cosine
23	q32i&d.cfg	QPSK	32	64	Integrate and Dump
24	q32rrc.cfg	QPSK	32	64	Square Root of Raised Cosine
25	q512rrc.cfg	QPSK	512	1024	Square Root of Raised Cosine
26	q64i&d.cfg	QPSK	64	128	Integrate and Dump

TABLE 2. EXAMPLE FIR FILTER COEFFICIENT FILES

NO.	FILE NAME	SQUARE ROOT OF RAISED COSINE FILTER α	NUMBER OF TAPS	FILTER SPAN (SYMBOLS)	FILTER DECIMATION	REQUIRED DQT OUTPUT RATE
1	rrc2a2x	0.2	16	8	None	2 x Symbol Rate
2	rrc2a4x	0.2	32	8	2	4 x Symbol Rate
3	rrc2a8x	0.2	64	8	4	8 x Symbol Rate
4	rrc35a2x	0.35	16	8	None	2 x Symbol Rate
5	rrc35a4x	0.35	32	8	2	4 x Symbol Rate
6	rrc35a8x	0.35	64	8	4	8 x Symbol Rate
7	rrc4a2x	0.4	16	8	None	2 x Symbol Rate
8	rrc4a4x	0.4	32	8	2	4 x Symbol Rate
9	rrc4a8x	0.4	64	8	4	8 x Symbol Rate
10	rrc5a2x	0.5	16	8	None	2 x Symbol Rate
11	rrc5a4x	0.5	32	8	2	4 x Symbol Rate
12	rrc5a8x	0.5	64	8	4	8 x Symbol Rate

#### Summary

The HSP50110/210EVAL kit includes software that enables the user to configure the hardware for data processing. Example configuration files represent a variety of symbol rates, filtering and modulation formats. Additional files are provided for using the onboard serial FIR filters. The following recommendations will facilitate your use of the HSP50110/210EVAL kit:

- It is recommended that users conform to the conventions used for naming both the configuration and FIR filter files, minimizing confusion when seeking application assistance.
- 2. It is critical that the user understand that the evaluation board outputs data at symbol rate, not the data rate. Setup problems masked when operating in the BPSK format, come to confuse the operator when higher level modulation formats are invoked. Review of the material on the first section of this application note can avoid the most common mistakes in modulator and demodulator test setups. QPSK and 8PSK modulators are likely to input data at the data rate, rather than the symbol rate, especially if the units have integral encoders. The HSP50110/210EVAL outputs I and Q data at the symbol rate, not the data rate. External generation of 2X or 3X clocks may be required to re-multiplex the data into a single data stream if decoding is not employed. Decoders generally require the I and Q symbols to properly perform decoding.
- 3. It is also recommended that users begin with one of the example configurations, rather than attempt an original configuration creation. The user needs to become familiar with the operation of the evaluation board before attempting the process of configuration design.

- 4. Users that wish to design application specific FIR filters should begin with the FIR configuration example. The second step should be to select a different FIR filter file for the example configuration. The third step is to use SERINADE to create an application specific FIR file. Following these steps will introduce the user to the operation of the evaluation board, the example configuration files, the example filter files and the SERINADE filter design software in a methodical order, minimizing confusion and reducing the likelihood of mistakes.
- 5. In standard Bit Error Rate Testers (BERT), maximal length sequences are used as the PseudoRandom test sequences. Common code lengths are 2<sup>7</sup>-1, 2<sup>10</sup>-1, 2<sup>15</sup>-1. and 223-1. One of the properties of these codes is that if every other bit of the sequence is selected, the original sequence will be generated at the lower rate at a new phase of the code. This property can be useful when testing the card in the QPSK mode when regeneration of the composite data rate cannot be done. The receive BERT should be set to the same code length as the transmit BERT but the symbol rate is entered as the operating rate. Either I or Q is connected to the BERT. Bit Error Rate data can be taken at the symbol rate. Note that imperfections in implementing the modulator (I/Q imbalance, d.c. offset, orthogonality, etc.) may degrade the BER of the individual channels (I or Q) at one or more of the lock points. Ideally, the BER at each lock point (2 for BPSK, 4 for QPSK, and 8 for 8PSK) will be identical. By taking an average of the BER on the I and Q Channels at the various lock points, the composite I/Q BER can be calculated.

# M APROTE

No. AN9661

January 1997

## Digital Signal Processing

## Implementing Polyphase Filtering with the HSP50110 (DQT) HSP50210 (DCL) and the HSP43168 (DFF)

Authors: John Henkelman and David Damerow

#### Introduction

Polyphase resampling filters are often used for timing adjustments in bit synchronizer loops. They are most commonly used at high baud rates where the sample rate to baud rate ratio ( $F_{\rm s}/R_{\rm Baud}$ ) is low. The HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL) chips support NCO driven polyphase resampling filtering when the HSP43168 Dual FIR Filter (DFF) is inserted between them. This application note will address use of the DQT, DFF and DCL in the polyphase filtering configuration.

#### Polyphase Filtering Overview

In polyphase resamplers, the process can be conceptually described as interpolation to a high rate, followed by a decimation to the desired lower rate. In practice, the process is done in a single step by changing the filter coefficients.

For example, in a 3/5 resampler, the input is interpolated by three using three sets of coefficient phases 0, 1, and 2. The interpolated signal is then decimated by 5, discarding 4/5 of the phases. The two steps are combined by computing three outputs for every five inputs. The resulting phases are:

 $IOUT_0 = 0_A;$ 

 $IOUT_1 = 2_B;$ 

 $IOUT_1 = 1_D;$ 

 $IOUT_2 = 0_F$ ;

 $IOUT_3 = 0_F;$ 

as shown in Table 1. One can see by inspection, that the same result can be accomplished by providing unique sets of coefficients and applying the appropriate filter coefficient set to the input data at the desired output rate. A unique coefficient set is required for every interpolated phase of the data, in this example - 3.

#### **DQT/DCL Resampling Capabilities**

The DQT/DCL have four design elements which enable polyphase filtering to be accomplished:

- 1. A resampling NCO with carry output
- 2. A latched resampling NCO phase word: SPH(4:0)
- 3. A programmable clock counter with carry output
- 4. A strobe, SSTRB, latched synchronous to both the Resampler NCO carry and the programmable clock counter carry.

In the DQT/CDL implementation, the resampling ratio is controlled by the resampling NCO. The ratio can be both irrational and variable. The DQT is fixed (controlled by a counter) at an output sample rate faster than the desired rate. The resampling NCO and the DFF are used to choose when to compute the next output and which interpolation phase to use. The DFF can store up to 32 filter phases (coefficient sets). This gives a timing resolution of ~3% of a symbol time.

**TABLE 1. INTERPOLATE BY 3 DECIMATE BY 5** 

INPUT DATA	INTERPOLATE BY 3 DATA	DECIMATE BY 5 DATA
IA	0 <sub>A</sub>	IOUT <sub>0</sub>
	1 <sub>A</sub>	
	2 <sub>A</sub>	
lΒ	0 <sub>B</sub>	
	1 <sub>B</sub>	
	2 <sub>B</sub>	IOUT <sub>1</sub>
lc	0 <sub>C</sub>	*
	1 <sub>C</sub>	
	2 <sub>C</sub>	
ID	0 <sub>D</sub>	
	1 <sub>D</sub>	IOUT <sub>2</sub>
	2 <sub>D</sub>	
ΙE	0 <sub>E</sub>	
	1 <sub>E</sub>	
	2 <sub>E</sub>	
IF	0 <sub>F</sub>	IOUT <sub>3</sub>

The DQT resampling NCO is programmed for the desired output sample rate. When the NCO rolls over, it sets a flag internally so that the NCO's phase, SPH(4:0), is sampled and the SSTRB signal is asserted aligned with the next output sample. The SSTRB signal indicates that a FIR computation is required. The SPH(4:0) signals hold the NCO phase at the output sample time, indicating which filter interpolation coefficient set to use.

#### PolyPhase Filter Design

The coefficients for the interpolation phases are generated by designing the filter at the interpolated rate (32x the input sample rate since there are five bits of phase represented in SPH(4:0)) with desired passband at <1X in input sample rate. With the DFF (without alternating the FWD and RVRS data), the prototype filter would have (32 phases x 8 taps) 256 taps. These taps are divided into the 32 filter phases by taking every 32<sup>nd</sup> sample and storing the result as coefficient sets 0 through 31. The first coefficient set would be C0, C32, C64, C96, C128, C160, C193, and C224. The last coefficient set would be C31, C63, C95, C127, C159, C192, C223, and C255. Note: Preadders in the DFF cannot be used since interpolation phase coefficients are asymmetric.

Decimation can be used if fewer interpolation phases are used - for example 16 coefficient phases can be realized by decimating by two. Because the resampling filter has only an 8 sample span (4 symbol), the short span yields relatively gradual transition band roll off, making it a poor shaping filter.

## Implementing a Resampling Filter Using the DQT, DCL and the DFF

There are several configurations for implementing polyphase filtering using the HSP50110 (DQT) and HSP50210 (DCL) with external FIR filters. Three distinct operational cases which are related to the selected input mode of the input controller of the DQT are: Normal, Gated, and Interpolated. This application note addresses only the Normal Input Mode, which has the \$\overline{ENI}\$ input to the DQT tied low. Bit position 1 of Control Address = 4 should be set high (1), selecting the gated mode. Hardwiring \$\overline{ENI}\$ will continuously gate the input.

Consider the implementation shown in Figure 1. The SSTRB and the SPH0-4 are used to gate the output of the filter address the filter and the coefficients respectively. Note that the SSTRB must be delayed an amount equivalent to the filter, to properly gate the filter output into the HSP50210 via the SYNC input signal. Using the fine phase address bits in SPH0-4, 32 filter phases (coefficient sets) can be realized.

The clocking and control of the FIR using CLK, SSTRB, SYNC, DATARDY and SPH0-4 becomes critical. Figure 2 outlines the configuration required. It is very important to understand the relationship between the various DQT clock and control outputs.

## CLK, the Programmable Divider, and the Re-Sampler NCO

The Programmable Divider must be configured to have CLK (the DQT input sample clock) as the clock source, rather than the Re-Sampler NCO carry out. To select CLK as the source, BIT 18 of DESTINATION ADDRESS 5 must be set to "1". The Programmable Divider (Destination Address 5 Bit 6 to 17) is set to a value of 2<sup>n</sup>, where n = 0, 1, 2, or 3. This generates a CIC Filter Clock that is CLK, CLK/2, CLK/4 or CLK/8, respectively. This clock will be gated to become the DATARDY signal, and will be used to gate the data into the external FIR filter. This selection of the Programmable Divider determines the SPH\_OUT\_SEL settings for the shifter or the Re-Sampler Phase output bits. Table 2 details the required settings.

**TABLE 2. DIVIDER AND PHASE SHIFT SETTINGS** 

PROGRAMMABLE DIVIDER	SHIFTER SETTINGS
0H	11
1H	10
3H	01
7H	00

Note that when the CIC Filter is clocked at CLK rate, no shifting occurs. Similarly, when the CIC Filter is clocked at CLK/8 rate, the shifter selects the phase bits fourth from the top as the MSB.

We desire finer phase resolution of a single decimated sample time. The Programmable Divider output, which is DQT CIC and DQT CIC compensation filter clock, is one positive (programmable positive or negative) pulse the width of one input sample clock period.

Note that the input sample clock (CLK) is the clock that should be used to clock the FIR filter input. The DATARDY signal will be used to enable the FIR filter input data sampling at the decimated rate.

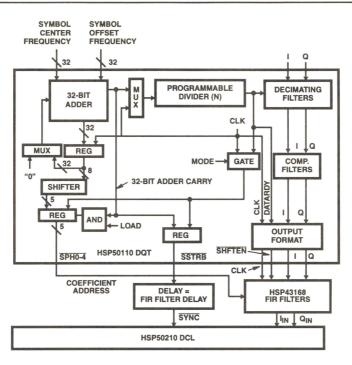


FIGURE 1. SIGNAL GENERATION FOR POLYPHASE FILTERING WITH HSP50110/HSP50210

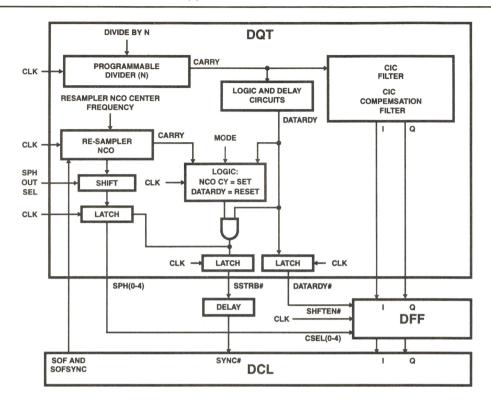


FIGURE 2. CLOCK AND CONTROL CONNECTIONS FOR POLYPHASE FILTERING

#### The SSTRB Signal and the Re-Sampler Phase Output

The Re-Sampler NCO is programmed to the desired sample frequency of the DCL input. It is not connected to clock any hardware in the DQT. This NCO provides a carry output, which identifies the zero phase location. Additionally, 5 bits of phase resolution are provided. The SSTRB signal is the gated version of the carry out of the Re-Sampler NCO.

There are two selectable modes of operation for the SSTRB signal. The first mode is an asynchronous continuous mode, where the carry out is passed directly out of the chip without concern for the timing of the programmable counter. The carry out is updated with every CLK rising edge. Do not use the asynchronous continuous mode for this application.

The second mode synchronizes the carry output pulse with the rising clock edge out of the programmable counter. Program BIT POSITION 13 of DESTINATION ADDRESS = 6 to be "0". This gating will "synchronize" the SSTRB and the 5 bits of sampler phase to the DATARDY signal. The synchronization occurs during gating and the gate will occasionally prevent the SSTRB and phase signals from their expected location, because they did not occur aligned with the DATARDY signal (during that output sample period).

The frequency of the Re-Sampler NCO carry out is equal to the programmed Re-Sampler NCO Center Frequency value multiplied by the frequency of CLK, scaled to 32 bits of resolution. If there is a Symbol Offset Frequency offset term, the sum of the offset and the center frequencies is multiplied by the frequency of CLK, and scaled to 32-bit resolution. This is detailed in Equation 1.

$$FCO = Fs \times (SCF + SOF)/2^{32}$$
 (EQ. 1)

where FCO = the frequency of the Re-Sampler NCO carry out; Fs = the DQT input sampling frequency (CLK); SCF = the Sampler Center Frequency; SOF = Sampler Offset Frequency.

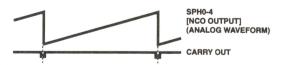


FIGURE 3. THE CARRY OUT SIGNAL RELATIONSHIP TO RE-SAMPLER PHASE BITS

#### NOTES:

- Because the SCF and SOF are both 32-bit words, the maximum value for the parenthetical expression is (FFFFFFFF + FFFFFFFF)/2<sup>32</sup>= 2, which yields an erroneous value of greater than one for the multiplier of the sampling frequency F<sub>S</sub>. This will cause the NCO to "rollover". If the sum of these two values (SCF + SOF) are kept less than 2<sup>32</sup>, rollover will not be an issue.
- 2. If the value of SCF is a multiple of 2, then there will be no jitter on the carry out of the NCO (and thus no jitter on the decimation filter clock or the DATARDY signal) so long as the SOF is zero. But as SOF adjusts the phase of the NCO, jitter on the order of one NCO clock will be introduced due to the non-integer value of the sampling frequency multiplier (SCF + SOF)/ 2<sup>32</sup>.
- 3. If the value of SCF is not a multiple of 2, then there will be jitter on carry out of the NCO on the order of one NCO clock due to the non-integer value of the sampling frequency multiplier (SCF)/2<sup>32</sup>. As the SOF signal adjusts the phase of the NCO, the jitter will remain, except on those rare moments when the sum of SOF and SCF is a multiple of 2.

Figure 3 shows the relationship to the NCO output values and the frequency of the NCO carry out signal. SPH (0-5) are 5 MSB's selected from the top 8 bits of the NCO output word. It is these bits that will be used to provide finer sampler phase resolution to address the coefficient sets in the FIR filter. A programmable shifter selects which 5 of the 8 MSB's are used as the sampler phase output. Up to thirty two symbol phase values can be achieved with these 5 bits. The shifter scaling retains the 32 state resolution for most NCO frequencies. These 5 bits should be connected to the FIR filter coefficient address lines.

#### The External FIR Filter

A FIR filter is used to provide for the resampling of the DQT output with timing associated with the Re-Sampler NCO frequency. Figure 4 shows a typical filter response for this FIR filter. The filter is designed as an Interpolate by 32/Decimate by n filter. The Interpolate by 32 is a "virtual" interpolation, since the part is being clocked at CLK rate, but enabled at the DATARDY rate. The FIR decimation rate is with respect to the DATARDY enable rate, which is the rate at which the FIR shifter is enabled. As shown in Figure 5, the filter must be designed to ensure that the RRC filter in the DCL chip is well within the flat passband of the FIR filter and not corrupted by aliasing. The DFF will aid in, but not be, the primary shaping filter in the receive path.

The HSP43168 dual FIR filter provides the capability to provide both the I and Q filters in a single chip if a 8 tap symmetric filter meets the customer requirements. Each of the 8 taps is used with 32 coefficient sets to yield a total filter of up to 8 x 32 = 256 taps. Another way to look at this is that this provides 8 filter taps per phase. Each of the 32 filter coefficient sets should be programmed with coefficients for different phases of the response. A typical single phase filter response is shown in Figure 6. This response becomes just one of 32 phase responses that as a composite will represent the filter. The main lobe response of composite filter, with 32 phases, is shown in Figure 7.

#### A Typical Single Phase Filter Response

The DCL will accept the output of the FIR Filter at the FIR decimated rate. These inputs will be enabled by the \$\overline{SYNC}\$ input, which is the \$\overline{SSTRB}\$ signal delayed by exact processing delay of the FIR Filter. Note that the \$\overline{SSTRB}\$ represents the "zero or start" phase sample of the 32 phases of the resampled rate clock. The designer must provide the input processing clock. This processing clock can be the CLK signal from the DQT, since the DCL inputs are enabled by \$\overline{SYNC}\$. Thus the effective sampling rate of the DCL is determined by the \$\overline{SSTRB}\$ (\$\overline{SYNC}\$) signal. The symbol loop filter output of the DCL, SOF and \$\overline{SOFSYNC}\$, should be routed to the DCL Re-sampler inputs of the same name.

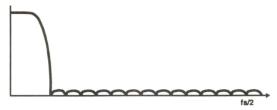


FIGURE 4. A TYPICAL DATA FILTER FOR THE FIR FILTER STRUCTURE

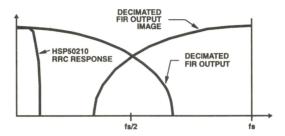


FIGURE 5. KEEPING THE DCL RRC FILTER WELL WITHIN THE FLAT PASSBAND

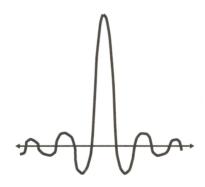


FIGURE 6. A TYPICAL SINGLE PHASE FILTER RESPONSE



FIGURE 7. THE "MAIN LOBE" COMPOSITE COEFFICIENT FILTER RESPONSE FOR A 32 PHASE FILTER

5

# APPIOTE

No. AN9676 May 1997

## Digital Signal Processing

## Loading Custom Digital Filters Into the HSP50110/210EVAL

Author: Paul Chen

#### Introduction

The HSP50110/210EVAL was intended to showcase the demodulation capabilities of the HSP50110 Digital Quadrature Tuner (DQT) and the HSP50210 Digital Costas Loop (DCL). This chipset was designed to handle primarily BPSK, QPSK, and OQPSK 10-bit sampled input waveforms data rates up to 52MHz. While many aspects of the chip are programmable, the filter coefficients are fixed. The filters provided within both chips will yield acceptable BER for most QPSK systems. However, if the system requires unique matched filtering or a nonstandard data convolution, then an additional digital filter must be placed either in front of the DQT, between the DQT and DCL, or after the DCL. Filtering before the DQT requires a digital filter to operate at rates greater than 52MHz (in order to ensure the convolution sum is completed every 19ns). Filtering after the DCL, which is after demodulation and symbol detection, allows aliasing and other corruption to pass through the downconversion into the baseband. Thus, the HSP50110/210EVAL platform provides for additional filtering between the DQT and DCL, where the aliasing and other corruptions can be removed prior to the baseband filtering and symbol detection at a reasonable processing rate.

The HSP50110/210EVAL provides the user the option of using a programmable HSP43124 Serial I/O filter for data shaping and frequency characterizing. This application note discusses how to program the serial filter using the SERINADE™ software development tool and the HSP50110/210EVAL configuration control software (demodevb.exe).

First, the paper discusses square root of raised cosine (RRC) filters, since the HSP50210 has an internal 15-tap  $\alpha=0.4$  RRC filter. A prototype RRC filter impulse response will be created. This coefficient set will be used to demonstrate the process of programming the serial filter. Custom coefficient sets for other filter types can be loaded using the same steps detailed in this process.

Second, the coefficients are then stored in a text file. This file will have a special header attached to it so that SERINADE can import it.

Next, SERINADE will then be used to generate a report file and configure decimations rates between the DQT and DCL. Serinade parameters that need to be changed will be highlighted.

Finally, the RRC filter created in the first step and formatted in the second and third steps will actually be loaded into HSP50110/210 Evaluation Board.

## Root-Raised Cosine Background Information

The square root raised cosine filter is derived from a broader class of filters called raised cosine filters. Raised cosine (RC) filters have zero crossings where the adjacent symbols are suppose to occur. Figure 1 is an example of a raised cosine filter. The center of the symbols are designated by the dotted lines. If the received signal contains a lot of intersymbol interference (ISI), the raised cosine filter suppresses the information from adjacent symbols. The adjacent information is zeroed out during the convolution.

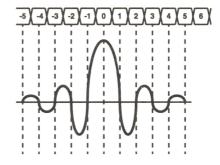


FIGURE 1. RRC FILTER CONVOLVING WITH A DATA SOURCE

Figure 2 shows some conceptual placements of the RC filter for a system with ISI. The third option uses two filters called root raised cosine (RRC) filters. The RRC filter has a frequency response equal to the square root of the frequency response of an RC filter. Remember that convolution in the time domain is equal to multiplication in the frequency domain. The data is convolved with the first RRC filter; the result is transmitted over a medium. The recovered data is again convolved an RRC filter. Thus the resulting frequency responses are equal to the original RC filter. Due to the one-to-one properties of transforms, equivalent frequency responses implies that the time domain responses are equivalent. The HSP50110/210 yields optimum BER performance when the transmitted data has been shaped by an RRC filter.

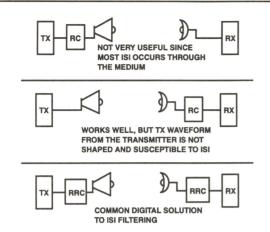


FIGURE 2. CONCEPTUAL ISI FILTERING; THE FILTERING
WOULD OCCUR WITHIN THE TX AND RX SYSTEM

The general RRC filter impulse response can be defined as

$$h(t) = \frac{4\alpha}{\pi\sqrt{T}} \left[ \frac{\cos\left((1+\alpha)\pi\frac{t}{T}\right) + \frac{\sin\left((1+\alpha)\pi\frac{t}{T}\right)}{4\alpha t/T}}{1 - \left(4\alpha t/T\right)^2} \right]$$
 (EQ. 1)

where t is time index, T is how many times faster the filter is operating than the symbol rate, and  $\alpha$  is the ratio of excess bandwidth past the 3dB point to the total bandwidth of the filter.

Lets examine an  $\alpha=0.2$  2xSymbol Rate RRC filter case. The code in Figure 3 was developed using a popular commercial software tool and Equation 1. Sixteen taps were selected to enable the user to regenerate an identical filter as rrc2a2x.imp from the filters directory of the HSP50110/210 distribution disk. Figure 4 shows the resulting gain of 1 impulse response filter.

n=-7:8; % n is an integer index from -7 to 8 in steps of 1. alpha = 0.2, T = 2, delta= -.5;

n=n+delta+.0001; % creates proper offset in index for cases % where intersymbol interference attenuation is needed.

scale = 4\*alpha/(pi\*sqrt(T));

 $A = \cos((1+alpha)*pi*n/T);$ 

 $B = \sin((1-alpha)*pi*n/T)./(4*alpha*n/T);$ 

 $C = 1-(4*alpha*n/T).^2;$ 

h = scale\*(A+B)./C;

h=h/sum(h); % sets the filter gain to 1

FIGURE 3. PSEUDO-CODE USED TO GENERATE AN RRC FILTER

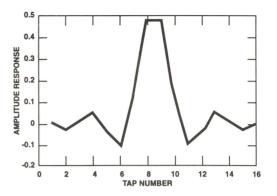


FIGURE 4. IMPULSE RESPONSE OF THE 16 TAP RRC FILTER

Figure 5 shows the frequency response of the 16 tap filter convolved with itself. Recall that this frequency response is equal to the frequency response of the system's raised cosine filter. Note that  $\alpha$  approximately equals (79-61)/61 = 0.295. By limiting the number of taps to 16, the IIR filter response given in Equation 1 is in effect, windowing. This windowing will result in the frequency response of the original IIR filter being convolved with a  $\sin(x)/x$  function. The lower number of taps, the bigger the ripples in the passband due to the  $\sin(x)/x$  frequency response of the smaller window. So with 16 taps, the  $\alpha$  can only be approximated, and ripples exist in the passband.

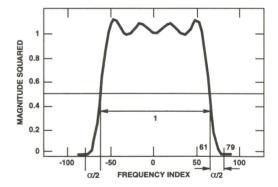
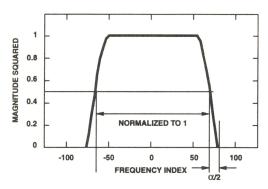


FIGURE 5. 256 POINT FFT OF THE 16 TAP RRC FILTER CONVOLVED WITH ITSELF

The frequency response of the raised-cosine filter is the main concern, since the RRC on the transmit side is convolved with the RRC on the received side. Together, they provide the intersymbol interference suppression required. A theoretical frequency response of an RC filter is given in Figure 6.

The RRC filter in Figure 6 was created with the same code used to generate the 16 tap filter. The index went from -127 to 128 instead of -7 to 8. This filter is essentially a 256 tap version of the previous filter. The greater the number of taps, the closer measured  $\alpha$  reaches the theoretical.



#### FIGURE 6. FREQUENCY RESPONSE OF AN IDEAL RRC

In our example we used a 2xbaud RRC filter. If we are running at a sampling frequency Fs that is 2 times faster than baud, then the filter cut off frequency should be half the sampling frequency, or Fs/2, which is equal to the baud rate. There is no reason why the filter can not run at Nx baud, making -Fs/N to Fs/N the filter passband.

To compute  $\alpha$ , always normalize the frequency ranges so that the range -Fs/N to Fs/N equals one. As shown in our 256 tap  $\alpha$  = 0.2 2x RRC filter on the previous slide,  $\alpha$  can be verified using the RC frequency response by measuring the bandwidth between the 3dB point (= 0.5 on the linear scale) down to the zero magnitude point.  $\alpha$  is obtained by dividing this measurement by Fs/N. As seen in the previous examples, the practical value of these calculations may or may not exactly matched the theoretical  $\alpha$  used in Equation 1 to generate the impulse response.

An additional characteristic of RRC filters is that mismatched RRC  $\alpha$ 's will have minimal effect on bit error rate tests. The mismatch acts similar to a noise source of relative amplitude shown in Figure 7 also add the mismatch filter reference. All mismatches have at least -28dB of degradation which translates into a negligible addition to the probility of error on the BER curve. Thus, for typical  $\alpha$  values between 0.3 and 0.7, there is no need to use a RRC custom filter.

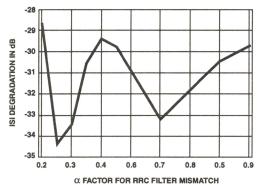


FIGURE 7. EFFECTS OF  $\alpha$  MISMATCH TO THE  $\alpha$  = 0.4 RRC FILTER ON THE HSP50110/210EVAL

#### Modifying Custom Filter Impulse Responses For SERINADE

In our commercial software package, we saved our filter file coefficients as a text file. To this text file, a 7 line header needs to be added in order for SERINADE to read it. The first six lines are not really read by SERINADE; however users should take advantage of this space to define the filters verbally. The 7th line requires an "r 1 16", where r tells SERINADE that the text file is a real data set, 1 tells SERINADE to read one column, and 16 tells SERINADE that 16 lines of data should be read. For an M-tap filter, an M should be used instead of 16. The modified file needs to have the "\*.imp" suffix attached to the desired file name. The SERINADE software assumes this suffix is a text file of the format describe in column 2 of Figure 8.

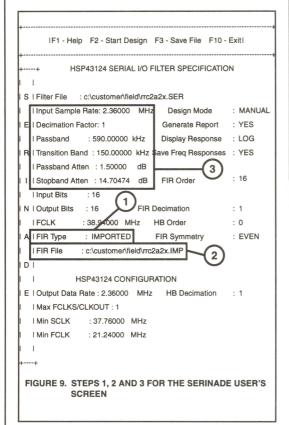
SAVED TEXT FILE	SERINADE "IMP" FILE
	"rrc2a2x.imp"
	Root Raised Cosine Filter Coefficient File
	Alpha = 0.20
	Tap Spacing = 0.5-0.001 Baud
	D.C. Gain = 1
	Maximum Output = 1.682
	r 1 16
0.0000	0.0000
-0.0296	-0.0296
0.0108	0.0108
0.0529	0.0529
-0.0367	-0.0367
-0.1018	-0.1018
0.1284	0.1284
0.4760	0.4760
0.4760	0.4760
0.1283	0.1283
-0.1018	-0.1018
-0.0367	-0.0367
0.0529	0.0529
0.0108	0.0108
-0.0296	-0.0296
0.0000	0.0000

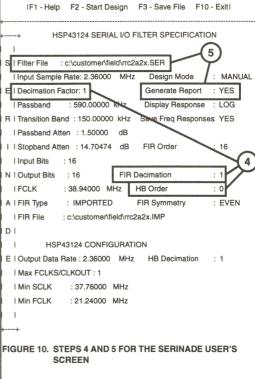
FIGURE 8. TEXT TO SERINADE FILE CONVERSION

## Using SERINADE to Import Custom Filter Responses

This section will detail how to import the modified text file created in the previous section into SERINADE. The SERINADE parameters that need to be changed will be highlighted and a SERINADE report file will be created. Assume that the name of our file modified text file is "rrc2a2x.imp". Figures 9 and 10 have each parameter that is changed highlighted with the step number from the following instructions:

- 1) Set FIR type to IMPORTED by toggling with space bar.
- Select filter path and name. The impulse response filter "rrc2a2x.imp" is located in the C: drive in the customer/field subdirectory of our PC. Users may place there \*.imp files elsewhere.
- Note that these values don't really mean anything. In the display, these are used to draw the nice green lines which really do not mean anything. The filter is set by the impulse response in rrc2a2x.imp.
- 4) If a Decimation error flashes on the screen, make sure to set the FIR decimation and the Halband filter decimation to the desired configuration. If the input of the DCL is equal to the output of the DQT, the FIR decimation should be set to 1 and Halfband order to 0.
- 5) Set Serinade up to save RPT file. Add filter name and path that is custom to current configuration.





Hit F2, and the SERINADE software creates the proper filter report filer. Figure 11 shows the frequency response that is displayed on the screen.

#### SYSTEM FREQUENCY RESPONSE

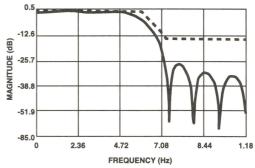


FIGURE 11. FREQUENCY PLOT GENERATED BY SERINADE

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#### **Application Note 9676**

A copy of SERINADE can be obtained from the Harris Semiconductor web site located at http://www.semi.harris.com. Select the DSP Products button. From the DSP Standard Product page, select the Product Development tools. Select the SERINADE software tools and download the needed files. Once loaded, run "serinade.exe" from either windows or from the DOS prompt. The report file created by SERINADE is stored as a \*.RPT file. This file is used by the HSP50110/210EVAL kit's software to program the on-board HSP43124.

#### Loading RPT Files into the HSP50110/210 Evaluation Board

The HSP50110/210EVAL kit includes a distribution disk so that users can easily program the evaluation board. The executable that should be run is called "demodevb.exe". When software demodevb.exe is executed, the menu shown in Figure 12 appears.

# HSP50110/210 EVALUATION BOARD SOFTWARE MAIN MENU (1) Data Path/Modulation Setup (2) Carrier Tracking Loop Setup (3) Bit Sync Loop Setup (4) Acquisition and Tracking Setup (5) Load Configuration File (6) Save Configuration File (7) Generate Output Files (8) Configure Hardware (9) Exit ENTER SELECTION:

## FIGURE 12. MAIN MENU FOR THE HSP50110/210EVAL SOFTWARE

The following steps detail loading the HSP50110/210 with the \*.RPT report file created by SERINADE. The rrc2a2x.rpt file will be used as the file. When a custom file has been generated, that report file's name should be used instead.

Enter a '1' to select the Data Path/Modulation setup. The menu appears as shown in Figure 13.

#### HSP50110/210 EVALUATION BOARD SOFTWARE DATA PATH / MODULATION MENU Current File Name...\EXAMPLES\Q1024RRC (1) Master Clock Freq.. 40000000 Hz (15) Es/No (min)....... +0 dB (2) Input Sample Rate.. 40000000 Hz (16) Es/No (max)...... +100 dB (3) Input Mode...... Gated (17) Es/No (design)..... +4 dB (4) DQT Input Samples.. Real (18) A/D backoff (min)... 12 dB (5) DQT Input Format... Offset Bin. (19) A/D backoff (max)... 18 dB (6) L.O. Center Freq... +5000000 Hz (20) DCL Output Vector... -6 dBFS (7) Data Modulation BPSK (21) DQT Output Level .... -12 dBFS (8) Baud Rate........ 128000 Hz (22) DCL Detect. Level... -12 dBFS (9) DQT Output Rate.... 256000 Hz (23) Slicer Threshold.... 0.25 (10) I.F. NBW...... 6000000 Hz (24) DQT AGC Slew Rate...20 dB/sec (11) DQT Filter....... CIC w/ comp (25) DCL AGC Slew Rate... 5 dB/sec (12) DCL RRC Filter .... Enabled (26) AGC Limits:..... Full Range (13) DCL I&D..... Bypassed (27) Output Mux Select... 7 (14) HSP43124 ..... Bypassed (0) Main Menu ENTER SELECTION: (C) Harris Semiconductor 1996 Version 1.01

#### FIGURE 13. DATA PATH/MODULATION MENU

Enter a 12 and disable DCL RRC Filter. The software will revert to the Data Path/Modulation menu. Notice item 12 has changed from "Enabled" to "Bypassed" as shown in Figure 14.

#### **Application Note 9676**

<u> </u>	<u></u>
HSP50110/210 EVALUATION BOARD SOFTWARE	HSP50110/210 EVALUATION BOARD SOFTWARE
DATA PATH / MODULATION MENU	DATA PATH / MODULATION MENU
Current File Name\EXAMPLES\Q1024RRC	Current File Name\EXAMPLES\Q1024RRC
(1) Master Clock Freq 40000000 Hz (15) Es/No (min) +0 dB	(1) Master Clock Freq 40000000 Hz (15) Es/No (min) +0 dB
(2) Input Sample Rate 40000000 Hz (16) Es/No (max) +100 dB	(2) Input Sample Rate 40000000 Hz(16) Es/No (max) +100 dB
(3) Input Mode Gated (17) Es/No (design) +4 dB	(3) Input Mode Gated (17) Es/No (design) +4 dB
(4) DQT Input Samples Real (18) A/D backoff (min) 12 dB	(4) DQT Input Samples Real (18) A/D backoff (min) 12 dB
(5) DQT Input Format Offset Bin. (19) A/D backoff (max) 18 dB	(5) DQT Input Format Offset Bin. (19) A/D backoff (max) 18 dB
(6) L.O. Center Freq +5000000 Hz (20) DCL Output Vector6 dBFS	(6) L.O. Center Freq +5000000 Hz (20) DCL Output Vector6 dBFS
(7) Data Modulation BPSK (21) DQT Output Level12 dBFS	(7) Data Modulation BPSK (21) DQT Output Level12 dBFS
(8) Baud Rate 128000 Hz (22) DCL Detect. Level12 dBFS	(8) Baud Rate 128000 Hz (22) DCL Detect. Level12 dBFS
(9) DQT Output Rate 256000 Hz (23) Slicer Threshold 0.25	(9) DQT Output Rate 256000 Hz (23) Slicer Threshold 0.25
(10) I.F. NBW 6000000 Hz (24) DQT AGC Slew Rate20 dB/sec	(10) I.F. NBW 6000000 Hz (24) DQT AGC Slew Rate20 dB/sec
(11) DQT Filter CIC w/ comp (25) DCL AGC Slew Rate 5 dB/sec	(11) DQT Filter CIC w/ comp (25) DCL AGC Slew Rate5 dB/sec
(12) DCL RRC Filter Bypassed (26) AGC Limits: Full Range	(12) DCL RRC Filter Bypassed (26) AGC Limits: Full Range
(13) DCL I&D Bypassed (27) Output Mux Select 7	(13) DCL I&D Bypassed (27) Output Mux Select 7
(14) HSP43124 Bypassed	(14) HSP43124\filters\rrc2a2x
(0) Main Menu	(0) Main Menu
ENTER SELECTION:	ENTER SELECTION:
(C) Harris Semiconductor 1996 Version 1.01	(C) Harris Semiconductor 1996 Version 1.01

#### FIGURE 14. DATA PATH/MOD MENU MODIFIED IN ITEM 12

Enter 14 at the Data Path/Mod Menu. The first four lines of Figure 15 will appear. Enable HSP43124, and the program will ask for a file name to be entered. If a name is not entered, the prefix listed in the "Current File Prefix" is used as the default. Note that in the "filters" directory is one directory below where the demodevb.exe is being operated. Thus the specific data path must precede the file name in order for the program to find the report file.

Current Value: 0

0 = HSP43124 filters bypassed

1 = HSP43124 filters enabled

Enter New Value [0]: 1

Current File Prefix: rrc8xa5

Enter File Prefix (.RPT exten. assumed): .\filters\rrc2a2x

## FIGURE 15. THE SUBMENU FOR ITEM 14 OF THE DATA PATH/MOD MENU

The filter name is the rrc2a2x.rpt without the rpt extension. The program will automatically look for the file name with the \*.rpt suffix.

The program, after recording this change, will return to the Data Path/Mod Menu as shown in Figure 16. Note that item 14 has changed.

#### FIGURE 16. DATA PATH/MOD MENU MODIFIED IN ITEM 14

Enter 0 and return to the main menu in Figure 12.

In the Main Menu, enter 7 to generate the proper output files. If the wrong path to the rrc2a2x.rpt file was entered for item 14 of the Data Path/Mod menu, the program will notify you and kick back into the Main Menu. If this occurs, go back to the Data Path/Mod Menu and correct item 14.

Otherwise, the program will process all the files and load the microcontroller. When the processing is complete, it will return you to the main menu. Hit 8 and do a full initialization. The HSP50110/210 should now be operating with a rrc2a2x filter.

The RRC filter in item 12 was disabled before implementing the rrc2a2x. Some applications may actually have a need for both matched filter and RRC filter. If the RRC filter internal to the HSP50210 is sufficient, then the match filtered should be loaded into the HSP43124, and item 12 should be enabled. If a different RRC filter is required, then the RRC coefficients should be convolved with the matched filter coefficients. The resulting filter should be loaded into the HSP43124, and item 12 should be disabled.

#### Summary

Two topics were covered in this application note that will help users of the HSP50110/210EVAL. For those unfamiliar with root-raised cosine filters, the fundamentals of RRC filters were discussed. The second topic covered the loading of custom filter coefficients into the HSP43124 Serial I/O filters. An example RRC filter was used to demonstrate the total process of loading custom coefficients.

# MAPPIOTE

No. AN9715 April 1997

# Harris Digital Signal Processing

## Ten Tips for Successful HSP50110/210EVAL Board Operation

Authors: John Henkelman and Paul Chen

Listed below are ten tips to guide you quickly to successful HSP50110/210EVAL board operaton . While these tips do not address complex problems, simple configuration mistakes can keep the board from operating properly. The HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL) demod chip set implement a very capable, flexible PSK receiver. By reading this list of solutions to common mistakes, you can proceed immediately to obtaining BER performance of less than 1dB from theory (0.5dB typical). When you have completed reading this Application Note, you will want to read Application Note AN9659: Using the HSP50110/210EVAL Example Configuration Files.

#### How to Use This Application Note

It is important that you read through the HSP50110/210EVAL User's Manual prior using the evaluation board and software. Following the setup instructions will minimize the time spent on configuration/setup so that performance evaluation can begin. Once you have entered your first configuration and are ready to download that configuration to the board, take time to read the list below and see if you made one of the top ten most common setup/configuration errors.

#### 1) Confusing Bits and Symbols when Setting Symbol Rate

Bit Rate is the rate of the single data stream input to a modulator. Symbol Rate is the rate that I and Q are output from the HSP50110/210EVAL demodulator. Table 1 shows the symbol to bit rate relationship for different modulation formats.

NOTE: The HSP50110/210EVAL outputs SYMBOLS not BITS.

TABLE 1.

MODULATION FORMAT	BIT RATE	SYMBOL (BAUD) RATE
BPSK	R	R
QPSK	R	R/2
8-PSK	R	R/3
16-PSK	R	R/4

The HSP50110/210EVAL outputs symbols, which enables a variety of Forward Error Correcting (FEC) decoders to be used with the DQT/DCL chip set.

#### 2) Incorrect LO Setting for Input IF

When undersampling the input IF, one has to remember that the desired signal set in the software screen is the downconverted IF.

#### Example:

Sample clock = 40MHz; Input RF = 70MHz

Set the LO to 10MHz because 80 - 70 = 10; 2f<sub>S</sub>-RF = aliased digital IF desired in this case.

For input RF signals below the Nyquist of the sample clock,  $\mathsf{RF} = \mathsf{LO}.$ 

The example files supplied on the distribution disk use either 5MHz or 10MHz LO. 5MHz files were generated and tested with the NCOM (HSP45116) as a 5MHz IF modulator. The 10MHz files were generated and tested using a 70MHz IF modulator. (See AN9659 for details of the two test configurations.)

#### 3) Clock Jumpers Not Set Properly

Determine if the sampling clock source, f<sub>S</sub>, is onboard or external. The HSP50110/210EVAL can be sourced with an external clock from the A/D or from test equipment.

 For onboard clocking, jumper JP2 pins 29 to 31 and 30 to 32.

In the Data Path/Modulation menu, enter the Oscillator Frequency as the Master Clock Frequency. The onboard crystal oscillator is 40MHz. The clock is output on P1 pin 20.

Make sure that the A/D does not source this pin.

 For external clocking, jumper JP2 pins 29 to 30, leave pins 31 and 32 open.

The clock can be input on P1C pin 20 (sourced from A/D), or from an external source, JP2 pin 30. See page 7 of the HSP50110/210EVAL User's Manual for clock inversion jumpering (JP2 pins 25/26; pins 27/28).

#### 4) Output Select Not Set Properly

Typical operation sets the Output Multiplexer Mux Control to 7 (0111). This configuration outputs the following signals:

#### **ISOFT Decisions**

(AOUT9-7): P2 pins C19 (MSB), A19, C18(LSB).

#### **QSOFT Decisions**

(AOUT6-4): P2 pins A18 (MSB), C17, A17(LSB).

#### **IEND Decisions**

(AOUT3-0; BOUT9-7): P2 pins C16, A16, A15, C14, A10, C9, A9(LSB).

#### **QEND Decisions**

(BOUT6-0): P2 pins C8, A8, C7, A7, C6, C5, A5(LSB).

The MSB's of the I and Q soft decisions can be used as hard decisions for the I/Q symbols. These signals can be routed to the bit error rate tester (BERT). IEND and QEND can be sent to D/A convertors for displaying constellation and transient responses on an oscilloscope.

#### 5) Not Selecting SymbCLK as the Data Clock

The DQT/DCL demod chip set outputs symbols. The clock accompanying these symbols is SMBLCLK (PIN 70 of the DCL) and GPOUT (P2-C21) of the EVAL board. JP5 pins 29-30 must be jumpered together.

The evaluation board clock CLKOUT on P2-C20 is a reference clock derivative. DO NOT USE CLOCKOUT FOR TYP-ICAL DATA OUTPUT.

The evaluation board clock CLKIN on P1-C20 is a reference clock derivative/input. DO NOT USE CLKIN FOR TYPICAL DATA OUTPUT.

The SLOCLK is brought to JP4-20 for use in outputting data from the loop filters. DO NOT USE SLOCLK FOR DATA OUTPUT (not used with DQT).

#### 6) A/D Eval Board Not Properly Set

Identify the A/D board properly. Harris offers a HI5702EV, HI5702EV2, and an HI5703EV. Use the appropriate alignment procedure for that board. Determine which input, Video or RF, to use and jumper the board accordingly. The fundamental difference is that Video assumes a single ended input while RF is differential.

Either works fine for most of SATCOM applications. The RF input is needed for wideband high rate applications. If using the RF input, verify that the RF transformer is installed. Harris does not supply transformers with all of the evaluation boards.

On all Harris A/D evaluation boards, begin the setup by aligning the reference voltages. This is usually accomplished by adjusting several potentiometers. Follow the alignment sequence recommended by the evaluation board user's manuals, since one adjustment/alignment may actually influence another.

Next align the clock reference to get 50% duty cycle using its DC offset pot. Jumper for the evaluation boards for correct Data Format. Jumper for the correct Clock polarity.

Application Notes AN9412 and AN9534 are supplied with the converter evaluation boards and are instructive in the alignment procedure.

#### 7) Unused Input MSB Not Pulled High

Typical use of the DQT has a "real" signal as the input. A real signal can be input on either the I or Q input pins. When operating in the offset binary mode, pull MSB of the unused input signal high to set the input bus to midscale.

The A/D evaluation boards that mate directly to the HSP50110/210EVAL use the Q input pins for the RF input signals, so pull IIN9 (the MSB) high.

Do not tie unused output bits to ground or V<sub>CC</sub>.

Do not tie input bits together if they are to be supplied by different sources.

#### 8) Input to A/D Not Set to a Proper Level

After complete alignment, the A/D input level should be less than 1Vpp input. Typically, the input level is 500mVpp. Having an A/D input that is too low can degrade the demodulator performance because insufficient bits are available for processing.

The evaluation boards do not have an AGC circuit for setting the optimal level into the A/D. The input level should be set using total power (signal plus noise) for the maximum signal density in the input band. Do not consider the signal alone. Failure to do this may cause clipping of the A/D under these full power conditions.

#### 9) Modulator Configuration Does Not Match Demod Configuration

This common error is related to Item #1 of this list. When setting the modulator data input rate, know whether you are setting the bit or symbol rate. On the Tx BERT it is usually bit rate.

On SATCOM modem equipment, it may be either bit rate or symbol rate, so find out which it is.

One clue is whether the device has an integrated encoder. If it does, than it can be assumed that the modulator is adjusted by symbol rate. Remember that the symbol rate is lower than the bit rate for higher order modulations of PSK.

#### 10) Incorrect COM Port Selected

The primary symptom is that the computer is not talking to the eval board. The typical cause of this error is having mistaken the identification of the PC serial port to which the evaluation board cable is connected (COM1 or COM2). Thus, the software is sending information to the wrong COM port on the PC. The software menu will allow users to set the COM port to 1 or 2. Be sure that the selected port is not already allocated to some other device.

#### Other Common Problems

#### Data Path/Modulation, Menu Item 9.

The question is usually:

"What should I set the DQT output rate to, relative to the baud rate (item 8)?"

- Typical operation sets this value to twice the baud (symbol) rate. Set the DQT output rate to:
  - 2 times the baud rate with the DCL RRC filters
  - N times the baud rate with the DCL I&D filters, where N is the number of samples integrated.
- · With external FIR filters:
  - Twice the baud rate, if not decimating
  - Four times the baud rate, if decimating by 2
  - Eight times the baud rate, if decimating by 4

#### Data Modulation = 0

There are the two characteristics of this setting:

- 1. No modulation expected on input (CW)
- 2. Output will be 1 on the I channel, 0 on the Q channel.

#### The NCOM As A Modulator

A common question when using an NCOM evaluation board as a modulator, is how do I set the carrier frequency?

The answer is that you need to run both the NCOM and DQT/DCL software packages on the same computer. One will use the parallel port (DB25 connector) and the other will use the serial (DB9) port.

Configure the NCOM first and then run the DEMODEVB software for the demod chip set. It is always a good idea to run NCOM\_CHK to verify proper operation of the NCOM evaluation board.

To set the carrier frequency of the NCOM, type the following hexadecimal value into the "Center Frequency" window:

NCOM F<sub>C</sub> Parameter = [(Desired F<sub>C</sub> (Hz)/Sampling frequency (Hz))  $2^{32}$ ]<sub>HEX</sub> = [(F<sub>C</sub>/F<sub>XO</sub>)  $2^{32}$ ]<sub>HEX</sub>

NOTE: The evaluation boards can have a number of different oscillators, so check the frequency of the one on your particular board. Write the frequency,  $F_{\chi O}$ , on the daughter board for future reference. 40MHz is a common value for  $F_{\chi O}$ , of the onboard oscillator, for the HSPEVAL/HSP45116 and the HSP50110/210EVAL.

BPSK data input is SB-24; QPSK data inputs are SB-24, 25. Grounds are JB-24, 25. Set the PM select to zero.

# External Filtering with an NCOM Modulator

A common question is: "When using an NCOM evaluation board as a modulator, do I need any external filters?" "Amplifiers?"

It is always a good idea to employ a filter after the D/A converter. A low pass filter will do just fine, but a bandpass with sufficient bandwidth will also do.

The need for an amplifier is application specific. In general you wish to set the signal output level high enough to properly match the noise power to yield the SNR desired. A filter is required when adding wideband noise to keep from aliasing the out of band noise into the band of interest and reducing the SNR.

Keep in mind that the NCOM allows programming of the output signal amplitude in binary increments. This can be helpful in finely setting the signal power. Do not use amplitudes so low that the resolution of the output is compromised, however.

# D/A Considerations When Using the NCOM Evaluation Board

The HI5721EV D/A Board can be readily used with the NCOM evaluation board to generate an analog, modulated IF. The HI5721 is a 10-bit, 125MHz D/A converter. Application note AN9410.1 is instructive in the proper use of this converter.

# MAPROTE

No. AN9720 June 1997

# Digital Signal Processing

## Calculating Maximum Processing Rates of the PDC (HSP50214)

Authors: John Henkelman and Dave Damerow

#### Introduction

Configuring the Programmable Digital Downconverter (PDC) requires selecting clock, decimation and interpolation rates for the various filter sections. Each filter section has limitations due to the hardware implementation. Furthermore, the input and output rates of the various sections must match in order for the composite configuration to be valid. In many cases, there may be multiple configurations that will yield the desired composite conversion and filter. In a few applications, a particular hardware constraint or specification will drive the complete configuration. This application note reviews the application of system requirements to the PDC, details the hardware constraints, introduces design approaches to the PDC, then details the hardware constraints; section by section.

For this application note the input sample rate, CLKIN, is 52MHz, and that the PROCCLK rate is 35MHz. REFCLK is a local reference input that can be used to phase lock the PDC output sample rate to local clocks. External clock recovery loop filters are required to process the PDC "Timing Error" into a valid Re-Sampler VCO control input. Since the rates of the PDC output and the local clocks can be different, refer to the Polyphase Filters and Interpolating Halfband Filters section for guidance in selecting the NCO and REFCLK frequencies.

# Mapping System Constraints into PDC Configuration

Three system parameters that will drive the PDC configuration are: 1) IF frequency, 2) the Bandwidth of Interest, and 3) the baud rate of the baseband data. This section details the first pass design configuration of the PDC based on these three system parameters. Once this first pass is completed, the remaining information in this application note will be used to optimize the PDC design configuration.

#### **System Input Specifications**

The IF frequency and the Bandwidth of Interest are used to set the minimum input sampling frequency, F<sub>S</sub>, of the PDC. Considerations are: 1) A/D Full Power Input Bandwidth, 2) the maximum clock rate of the A/D converter, and 3) the 52MHz maximum PDC input sampling rate. If the IF frequency is in the upper portion of the A/D bandwidth and that bandwidth is greater than the maximum sample rate of the A/D or PDC, then use of undersampling techniques to pro-

cess a lower frequency sampling alias of the IF signal should be considered. If the IF is in the lower portion of the A/D bandwidth and is below the maximum rate of the A/D and the PDC, then traditional oversampling techniques should be considered. In both cases, consideration of signals outside the band of interest, but inside the A/D converter bandwidth must be considered to avoid alias interference or reduction of dynamic range. The design of the IF alias filter (bandwidth, rolloff, rejection and cost) will be an important part of this consideration. It is likely that selecting the input sampling rate to meet the Nyquist rate for the bandwidth of interest and the spectral purity requirements, will involve reviewing several frequency plans with a variety of sampling frequencies.

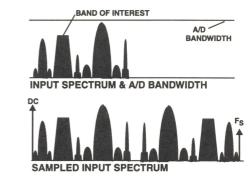


FIGURE 1. CONSIDERING IF FREQUENCY, A/D BANDWIDTH,
AND ALIASING IN SELECTION OVERSAMPLING

#### Hardware Constraint Overview

#### **System Output Specifications**

The system output specifications that affect the configuration of the PDC are the baseband baud rate and/or baseband bandwidth. The baud rate or equivalent low pass bandwidth sets the PDC output sample rate or the minimal PDC bandwidth. In some digital systems the baseband output rate is required to be a submultiple of the A/D converter sample rate. The relationship between input and output sampling rate, or total decimation is fixed and must be distributed among the various filter elements while creating a composite filter meeting the equivalent low pass bandwidth and the PDC hardware constraints. The detailed section of this document will provide the possible decimation rates for each filter section.

The 255 tap FIR filter input sampling rate should be set at greater than or equal to twice the equivalent lowpass bandwidth, since this is the narrowest filter section in the PDC. If use of even one stage from the Halfband filter is required, then the 255 tap FIR filter input sampling rate should be set at greater than or equal to four times the equivalent lowpass bandwidth, to minimize the alias effects on dynamic range. Setting the 255 tap FIR filter input rate sets the number of PROCCLKS available for filter calculations, and thus determines the number of filter taps possible.

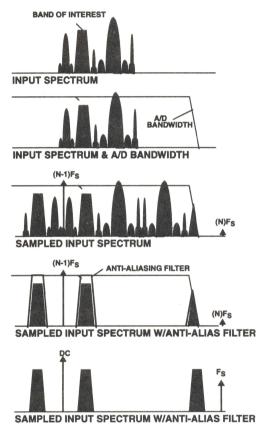


FIGURE 2. CONSIDERING IF FREQUENCY, A/D BANDWIDTH,
AND ALIASING IN SELECTION UNDERSAMPLING

The Halfband filter input sample rate is set at  $2^N$  times the FIR input sample rate, where N is the number of halfband filter stages active. Note that each halfband stage will decimate by 2.

The CIC filter input is sampled at F<sub>S</sub>, so that it must provide a decimation of F<sub>S</sub>/F<sub>HBIN</sub>. The CIC filter also affects the dynamic range. At a bandwidth of 1/8 the input sample rate, the CIC filter provides 84dB of dynamic range. At a bandwidth of 1/10 the input sample rate, the CIC filter provides 96dB of dynamic range. At a bandwidth of 1/12 the input sample rate, the CIC filter provides 100dB of dynamic range.

With the FIR, halfband filter, and CIC rates set two checks must be performed to validate this first pass PDC configuration: 1) the composite dynamic range - set primarily in the CIC and Halfbands, and 2) the number of clocks required for filter calculation must be met. Information provided in the detailed filter sections will provide the parameters needed to complete these checks.

#### Hardware Constraint Overview

This section provides an outline overview of the clocking and timing constraints of each major functional block in the PDC. More details on these constraints can be found in the respective section of this application note, or in the HSP50214 data sheet [1]. The intention of this outline overview is to introduce the reader to timing issues that should be kept in mind as the detailed sections of the PDC data sheet and this application note are studied.

#### 1. Summary of Rate and Bandwidth Constraints

The PDC contains a set of very flexible filter blocks. Each filter set offers a unique design feature. The CIC offers a broad passband and initial broad stopband capability. The Halfband offers sample rate reduction and bandwidth reduction in multiples of 2. The 255 tap FIR offers high resolution filter response shaping and contouring. The Polyphase Re-Sampling FIR offers non-integer rate changes. The Interpolation HalfBand filters offer oversampling. The discriminator FIR offers bandwidth reduction. Figure 3 summarizes the rate changes (in terms of decimation) and bandwidth adjustments that occur in the various filter blocks of the PDC.

	DECIMATION	3dB BANDWIDTH
CIC FILTER	4 TO 32	1/8 F <sub>S</sub> (84dB DYNAMIC RANGE BW)
HALFBAND FILTERS	2 <sup>N</sup>	1/2 <sup>(2+N)</sup> F <sub>S</sub> (ALIAS FREE)
255 TAP FIR FILTER	1 TO 16	BY DESIGN (1/4 F <sub>S</sub> FOR GOOD DYNAMIC RANGE)
RE-SAMPLER POLYPHASE FIR FILTER	1 TO 4 (NON-INTEGER VALUES OK)	1/4 F <sub>S</sub>
INTERPOLATING HALFBAND FILTERS	1/2 OR 1/4	2 OR 4 F <sub>S</sub>
FREQUENCY DISC. FIR FILTER	1 TO 8	BY DESIGN

♦ NOTE: F<sub>S</sub> = INPUT SAMPLE RATE OF THE FILTER BLOCK

#### FIGURE 3. OVERVIEW OF RATES AND BANDWIDTHS

#### 2. CIC Filter

Decimation: 4 - 32

The CIC filter runs at CLKIN rate (up to 52MHz). If the CIC is bypassed, the sync circuitry requires that the  $\overline{\text{ENI}}$  signal drop low, then go high to pass data from the CIC input to the output.

#### 3. Halfband Filter

Decimation: 20 to 25

The Halfband filter computes at PROCCLK rate (up to 35MHz) The HB filter input sample rate is required to be less than PROCCLK by an amount determined by the number of halfband filters selected. The range of the divisor is 3 to 9.75 (See Table 2 in the HB Filter section). NOTE: If the Halfband is bypassed, decimation may be required in the 255 tap FIR filter to lower the sample rate to the PROCCLK/6 requirement of the AGC.

#### 4. 255 Tap FIR

Decimation:  $1 \le R \le 16$ Number of Taps: 3 - 255

Filter bypass is achieved by setting the center tap to 1 and taps  $C_{-1}$  and  $C_{1}$  to zero. A rule of thumb used for the largest number of taps that can be achieved is:

$$((PROCCLK)/(f_{FIROLIT}) \times 2) - (R) = TapNumber$$
 (EQ. 1)

#### 5. AGC

Requires 6 PROCCLKS to process data - **always**. The AGC functional bypass can be effected by setting the upper and lower AGC limits to an identical number. The bypass mode still requires 6 PROCCLKS to complete the calculation.

#### 6. Re-Sampler and Interpolating HalfBand Filters

The number of PROCCLK cycles required for the Re-Sampler and interpolating HalfBand filters to compute is dependent on the configuration. The valid configurations are:

<ul> <li>Re-Sampler</li> </ul>	Filter 6 clock
Re-Sampler	and 1 Halfband 13 clock
Re-Sampler	and 2 Halfbands 23 clock
• 1 Halfband .	7 clock
• 2 Halfbands	17 clock
. D	0 1 - 1

#### 7. Cartesian to Polar Coordinate Converter

The Coordinate converter requires 17 clocks to yield 16 bits of resolution on the phase and magnitude outputs. If new input samples arrive prior to the completion of 17 clock cycles, the calculation is terminated and the interim result is latched with reduced resolution. The minimum resolution possible is 4 bits.

#### 8. Discriminator FIR Filter

The Discriminator FIR filter output is clocked at the input sample rate, so that if the filter is decimating, multiple data outputs will result until the decimation requires the next output sample to appear.

#### Design Approaches for the PDC

The PDC contains an NCO/Mixer and six filter blocks which can be configured for various applications. A natural question to ask about the PDC is "What is the maximum operation rate?" Because there are three internal clocks: CLKIN for the front end blocks; PROCCLK for back end blocks; and the Re-Sampling NCO clock for the Re-sampling polyphase FIR, Interpolating Halfband filters, and output blocks, the answer is not so simple. Likewise, determining the maximum output bandwidth can be somewhat complex. A top level approach to PDC configuration is necessary to understand and to maximize the many features of each filter block in this very flexible downconverter.

#### 1. Begin with the FIR

The 255 tap FIR is the key filter element in the PDC. This filter provides the most flexibility in establishing spectral shaping, complying with the out of band rejection, passband bandwidth and transition band specifications. The FIR establishes the narrowest bandwidth in the downconverter, and thus is related to the Nyquist rate of the bandwidth of interest in any application. Three design parameters, 1) out of band rejection, 2) transition bandwidth, and 3) number of taps, offer three degrees of design freedom in approaching a digital downconverter. These three degrees of freedom allow optimizing dynamic range, sample rates, number of filter taps and out of band rejection throughout the filter blocks in the converter. All three approaches begin with the FIR filter design. Many of the requirements for the FIR filter are set by the transmit baseband filtering.

The first design approach fixes the number of taps and varies the out of band rejection and transition band until a compliant design is implemented. The fixed number of filter taps may be set because of some clocking restraint of one of the filter blocks in the PDC or somewhere in the overall system.

The second design approach sets an out of band specification and varies the number of filter taps or the transition band to create a compliant design.

The third design approach sets a fixed transition band specification and varies the number of filter taps and the out of band rejection, to create a compliant design. An overview of these three approaches is illustrated in Figure 4.

The 255 tap FIR should be designed to have an output bandwidth no greater than 1/4 of the FIR input sample rate. This prevents the halfband filter from introducing interfering alias terms in the band of interest. Excellent passband dynamic range is achieved when the FIR output rate is set to 1/4 the HB5 Halfband Filter input sample rate,

$$\left(\mathsf{F}_{\mathsf{HBS}} = \frac{\mathsf{CICOutputRate}}{2^{\mathsf{N}}}\right), \tag{EQ. 2}$$

because it ensures significant attenuation of the composite filter alias profile in the passband. Figure 5 illustrates such a filter design.

Use of the Interpolating Halfband Filters further down the processing chain can allow the FIR to run at reduced rate to maximize the number of taps available in the 255 tap FIR filter.

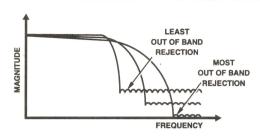


FIGURE 4A. FIXED NUMBER OF FILTER TAPS, VARIABLE OUT
OF BAND REJECTION, VARIABLE TRANSITION
BAND

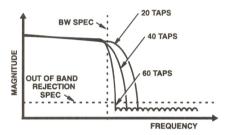


FIGURE 4B. FIXED OUT OF BAND REJECTION, VARIABLE NUMBER OF FILTER TAPS, VARIABLE TRANSITION BAND

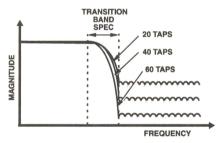
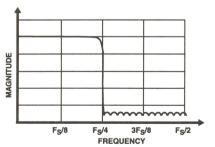


FIGURE 4C. FIXED TRANSITION BAND, VARIABLE OUT OF BAND REJECTION, VARIABLE NUMBER OF FILTER TAPS

FIGURE 4. FREQUENCY DOMAIN VIEW OF DESIGN TRADES



 $F_S$  = RE-SAMPLER/INTERPOLATING HALFBAND INPUT RATE FIGURE 5. RULE OF THUMB DESIGN OF FIR PASSBAND

#### 2. Re-Sampler and Interpolation Considerations

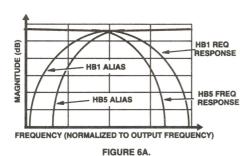
The second filter block to be considered is the Polyphase Re-Sampler FIR/ Interpolation Filters. While the 255 Tap FIR establishes the bandwidth of interest, the Polyphase Re-Sampler/Interpolating Halfband filter is used to establish the output rate of the PDC. The output sample rate of the polyphase re-sampling filter is less than its input sample rate. The rate change is set by the ratio of the Re-Sampler NCO frequency to the Re-Sampler input sample rate. The range of the rate change is from 1/4 to ~1, of FS, the Re-Sampler filter input sample rate. This value is not required to be an integer! The 3dB passband of the polyphase re-sampler filter is located at 1/4 the Re-Sampler filter input sampling frequency. Use this filter to establish the non-integer rate changes from the input sampler to the output (user) sample rate. The Re-Sampler NCO update rate is the input sample rate to the Re-Sampler filter.

The Interpolation Halfbands offer the designer the ability to oversample the re-sampled polyphase filtered data by twice or four times the polyphase filter output rate. Thus, the rate change of this filter block can vary from 0.25 to 4. These halfband filters allow the 255 tap FIR filter to be run at a lower rate to obtain more filter taps. The output rate of this filter block is the sample rate of the coordinate converter, the discriminator, the discriminator FIR and the output block.

#### 3. Halfband Filter Considerations

The third filter block to be considered is HalfBand filter block. The halfband filters are used to dramatically reduce the sampling rate and bandwidth of the input signal. This filter block allows the user to set an even multiple of 2 rate reduction and bandwidth reduction. Rate changes from 1 to 1/32 are possible with bandwidth reductions of up to 1/32 using this filter block. The halfband filters have a flatter passband and a wider "alias free" output bandwidth than the CIC filter.

Use of this block requires an understanding of the alias profile to ensure that the desired dynamic range is achieved prior to entering the 255 tap FIR filter. Recall that the FIR filter bandwidth was set to 1/8 of its input frequency to avoid the alias images of the last halfband filter, which fall at 1/4 of the FIR input sample rate. The effect of the alias on full dynamic range is illustrated in Figure 6, which compares the full dynamic range bandwidth of the first and last stage of the Halfband filter block. By establishing a dynamic range specification, the bandwidth can be selected from any combination of the halfband filters, although the filters are typically enabled from stage 5 down to stage 1, as increasing number of stages are required.



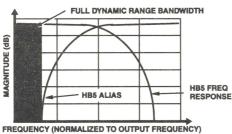


FIGURE 6B.

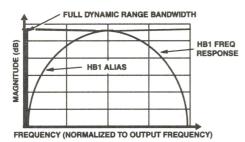


FIGURE 6C.

FIGURE 6. HALFBAND FULL DYNAMIC RANGE BANDWIDTHS

#### 4. CIC Filter Considerations

The final filter stage to be considered is the CIC filter. The CIC filter is the only filter stage that is running at the CLKIN rate (when CLKIN > PROCCLK). This filter provides the rate reduction necessary to meet the back end processing rate, PROCCLK. This allows for maximum sampling speed into the part. The CIC filter does rate reduction and out of band signal filtering. The CIC filter response has a main lobe extending to Fs/R, where R is the decimation rate of the filter and ranges from 4 to 32.

#### 5. Filter Implementation Trades

With the initial pass of the PDC internal filter configuration process complete, the next step is to optimize the filters. Begin by verifying that all of the filter sample rates match at the interfaces. From an input performance perspective, the highest sampling rate is most desired. From the output performance perspective, the filter requirements may require

lower clock rates to implement a more complex FIR filter. These can abe opposing system constraints.

FSAMP is set to a few frequencies in GSM (multiples of the baud rate). The FIR output sample rate must be a submultiple to find acceptable FIR input sample rates and make sure it can be designed. Then check the alias of the halfband (BW < 1/4 FSAMPLE FIR).

Remember that the CLKIN rate limit is 52MHz, while the PROCCLK is 35MHz. This means that the CLKIN input sample rate must be decimated by at least 2 to make the interface compatible. PROCCLK must always be greater than or equal to the CIC filter output rate discussed in the Polyphase Re-Sampling filter section.

After configuring the filters, the next step is to confirm that the dynamic range is acceptable. Finally, check the FIR filter taps available and ensure that the out of band attenuation and transition band filter performance are acceptable. The final check is verify that the output rate is sufficient for the application.

#### **Detailed Filter Block Descriptions** Fifth Order CIC Filter

This filter has a minimum decimation rate of R = 4 and a maximum decimation rate of R = 32 (Note 1). The minimum rate of 4 is set by the hardware multiplex and throughput delays. This section is clocked at CLKIN rate, defining the maximum input rate as 52 MSPS.

TABLE 1. CIC FILTER OUTPUT RATE vs DECIMATION RATE

CIC	(NOTE 1) DECIMATION RATE (R)	(NOTE 2) MAXIMUM FILTER OUTPUT RATE (MSPS)	COMMENTS
Bypass	-	52	No Decimation
CIC	4	52/4 = 13.0	Minimum Decimation is 4
CIC	5	52/5 = 10.4	
CIC	6	52/6 = 8.67	
CIC	7	52/7 = 7.43	
CIC	8	52/8 = 6.50	
CIC	9	52/9 = 5.78	
CIC	10	52/10 = 5.20	
CIC	11	52/11 = 4.73	
CIC	12	52/12 = 4.33	
CIC	13	52/13 = 4.00	
CIC	14	52/14 = 3.71	
CIC	15	52/15 = 3.47	
CIC	16	52/16 = 3.25	
CIC	17	52/17 = 3.06	

#### **Application Note 9720**

TABLE 1. CIC FILTER OUTPUT RATE vs DECIMATION RATE (Continued)

-			
CIC MODE	(NOTE 1) DECIMATION RATE (R)	(NOTE 2) MAXIMUM FILTER OUTPUT RATE (MSPS)	COMMENTS
CIC	18	52/18 = 2.89	
CIC	19	52/19 = 2.74	
CIC	20	52/20 = 2.60	
CIC	21	52/21 = 2.48	
CIC	22	52/22 = 2.36	
CIC	23	52/23 = 2.26	
CIC	24	52/24 = 2.17	
CIC	25	52/25 = 2.08	
CIC	26	52/26 = 2.00	
CIC	27	52/27 = 1.93	
CIC	28	52/28 = 1.86	
CIC	29	52/29 = 1.79	
CIC	30	52/30 = 1.73	
CIC	31	52/31 = 1.68	
CIC	32	52/32 = 1.63	Maximum Decimation is 32

#### NOTES:

- It is possible to achieve a decimation of 64 using a 10-bit converter shifted to the bottom of the input bits, a non-standard configuration.
- 2. The maximum rate may be limited in subsequent blocks.

### Decimating Halfband Filters

The decimating halfband filters are clocked by the PROC-CLK, which makes the maximum input rate for this filter section equal to 35MHz. It is important that this section must be able to support the output rate of the CIC section for proper operation. Five selectable decimating halfband filters in this block have progressively narrower alias free transition bandwidths, ranging from 0.5 to 0.125 times the input sample rate. The 6dB bandwidth of all five filters is 0.250 times the input sample rate. Each halfband section will decimate by two, (i.e the output rate will be half the input rate). Note that the filter sections may be enabled in any combination. Filters should be selected based on the required transition band steepness and acceptable clock rate. The equation used in Table 2, to calculate the ratio of the PROCCLK to Sample Rate is:

$$\begin{split} F_{PROCCLK}/F_S & \geq [(7)(HB5)(2^{HB5}) + \\ & (6)(HB4)(2^{(HB4 + HB5)}) + \\ & (5)(HB3)(2^{(HB3 + HB4 + HB5)}) + \\ & (4)(HB2)(2^{(HB2 + HB3 + HB4 + HB5)}) + \\ & (3)(HB1)(2^{(HB1 + HB2 + HB3 + HB4 + HB5)})]/2^T \end{split}$$

#### where

HB1 = 1 if HB1 is selected and 0 if it is bypassed;
HB2 = 1 if HB2 is selected and 0 if it is bypassed
HB3 = 1 if HB3 is selected and 0 if it is bypassed
HB4 = 1 if HB4 is selected and 0 if it is bypassed
HB5 = 1 if HB5 is selected and 0 if it is bypassed
T = number of Halfband Filters. The range for T is (0-5).

TABLE 2. DECIMATING HALFBAND MAXIMUM OUTPUT RATES vs CONFIGURATION

	HALFBAND FILTER SECTION NUMBER					MAXIMUM INPUT SAMPLE RATE (MHz)	MODE	MAXIMUM OUTPUT RATE (MHz)
5	4	3	2	1	(F <sub>PR</sub> /F <sub>S</sub> )	F <sub>PR</sub> = 35MHz	Activated Halfband Filter	F <sub>PR</sub> = 35MHz
0	0	0	0	0	1.00	35.00	Bypass - None	35.00
1	0	0	0	0	7.00	5.000	HB5	2.500
0	1	0	0	0	6.00	5.853	HB4	2.917
1	1	0	0	0	9.50	3.684	HB5 & HB4	0.921
0	0	1	0	0	5.00	7.000	НВ3	3.500
1	0	1	0	0	8.50	4.4118	HB5 & HB3	1.029
0	1	1	0	0	8.00	4.375	HB4 & HB3	1.084
1	1	1	0	0	9.75	3.590	HB5 & HB4 & HB3	0.449
0	0	0	1	0	4.00	8.750	HB2	4.375
1	0	0	1	0	7.50	4.667	HB5 & HB2	1.167

TABLE 2. DECIMATING HALFBAND MAXIMUM OUTPUT RATES vs CONFIGURATION (Continued)

0	1	0	1	0	7.00	5.000	HB4 & HB2	1.250
1	1	0	1	0	8.75	4.000	HB5 & HB4 & HB2	0.500
0	0	1	1	0	6.50	5.385	HB3 & HB2	1.346
1	0	1	1	0	8.25	4.242	HB5 & HB3 & HB2	0.530
0	1	1	1	0	8.00	4.375	HB2 & HB3 & HB4	0.547
1	1	1	1	0	8.88	3.944	HB5 & HB4 & HB3 & HB2	0.247
0	0	0	0	1	3.00	11.667	HB1	5.833
1	0	0	0	1	6.50	5.385	HB5 & HB1	1.346
0	1	0	0	1	6.00	5.833	HB4 & HB1	1.458
1	1	0	0	1	7.75	4.516	HB5 & HB4 & HB1	0.565
0	0	1	0	1	5.50	6.364	HB3 & HB1	1.591
1	0	1	0	1	7.25	4.828	HB5 & HB3 & HB1	0.603
0	1	1	0	1	7.00	5.000	HB4 & HB3 & HB1	0.625
1	1	1	0	1	7.88	4.444	HB5 & HB4 & HB3 & HB1	0.278
0	0	0	1	1	5.00	7.000	HB2 & HB1	1.750
1	0	0	1	1	6.75	5.185	HB5 & HB2 & HB1	0.648
0	1	0	1	1	6.50	5.385	HB4 & HB2 & HB1	0.673
1	1	0	1	1	7.38	4.746	HB5 & HB4 & HB2 & HB1	0.297
0	0	1	1	1	6.25	5.600	HB3 & HB2 & HB1	0.700
1	0	1	1	1	7.13	4.912	HB4 & HB3 & HB2 & HB1	0.307
0	1	1	1	1	7.00	5.000	HB4 & HB3 & HB2 & HB1	0.313
1	1	1	1	1	7.44	4.706	HB5 & HB4 & HB3 & HB2 & HB1	0.147

#### 255 TAP FIR Filter

The 255 TAP FIR filter has a minimum realizable decimation rate of R = 1. The maximum decimation rate realizable in this filter is R = 16. The filter can be "effectively" bypassed by setting  $C_0$  = 1 and  $C_N$  = 0. This requires two clock cycles. The filter is clocked by PROCCLK, so the maximum input rate is 35MHz. One clock is used to write data into the ROM.

#### 1. Determining the Number of FIR Filter Taps

For the generic filter configuration, use Equation 4 to calculate the number of taps available at a given input sample rate. We can use Equation 5 to calculate the maximum input rate, and Equation 6 to calculate the maximum output rate.

Taps = floor[PROCCLK/(
$$F_{SAMP}/R$$
) - R] • (1 + SYM) - (SYM • ODD) for real filters) (EQ. 4A)

Taps = floor[PROCCLK/( $F_{SAMP}/R$ )-R]/2 for complex filters

(EQ. 4B)

where floor is defined as the integer portion of a number; PROCCLK is the compute clock; F<sub>SAMP</sub> = the FIR input sample rate; R = Decimation Rate; SYM = 1 for symmetrical filter, 0 for asymmetrical filter; ODD = 1 for an odd number of filter taps, 0 = an even number of taps.

#### **Example FIR Filter "Number of Taps" Calculation**

As an example, for a 35MHz compute clock, a 5MHz input sample rate, decimation by 2, even symmetry, and an odd

number of taps, the number of taps is:

Ta ps = floor[35MHz/(5MHz/2) - 2]  $\bullet$  (1 + 1) - (1  $\bullet$  1) = floor[14 - 2]  $\bullet$  2 - 1 = 12  $\bullet$  2 - 1 = 23 for a real filter and

Taps = floor[35MHz/(5MHz/2) - 2]/2 = floor[14 - 2]/2 = 6 for a complex filter

#### 2. Calculating the Maximum Input Sample Rate

We can rearrange Equation 3 to yield the maximum input sample rate.

$$F_{SAMP} = PROCCLK \bullet (R)/[R + [(Taps) + (SYM \bullet \overline{ODD})]/(1 + SYM)]$$
 for real filters (EQ. 5A)

$$F_{SAMP} = PROCCLK \cdot R/[R + [(Taps) \cdot 2]]$$
  
for complex filters (EQ. 5B)

where PROCCLK is the compute clock;  $F_{SAMP} = the FIR$  input sample rate; R = Decimation Rate; SYM = 1 for symmetrical filter, 0 for asymmetrical filter;  $\overline{ODD} = 1$  for an odd number of filter taps, 0 = an even number of taps.

#### **Example Maximum Input Rate Calculation**

Let's use the example provided above to see if we can predict the 5MHz input rate.

 $F_{SAMP} = 35MHz^*(2)/[2 + [(23)+(1)]/(2)] = 5.00MHz$ , which is correct.

#### 3. Calculating the Maximum Output Rate

#### **Application Note 9720**

Table 3 provides a sampling of the filter output rate calculations. The maximum output rate as a function of a real symmetric 127 tap filter configuration with varying decimation rates is given. Use of Equations 4, 5 and 6 provide the details necessary to calculate an application specific filter configuration. Remember that prior to obtaining a part level operational configuration, the input rate of the 255 tap FIR Filter section must match the output rate of the Halfband filter section.

Figures 7 and 8 provide a plot of Input Rate and Output Rate as a function of Decimation Rate for a set of odd number of

tap, symmetric filters (15, 31, 63, 127, 191 and 255). They will help in estimating input and output rates if the filter is known

Another approach is to determine the number of filter taps that can be implemented at a specific input rate. Figures 9 through 12 are plots of the number of filter taps based on the input rate. Each figure represents a different decimation rate (R = 1, 2, 4, 8, and 16). These plots will help determine the extent of shaping that can be done with the FIR filter for the specific input rate.

TABLE 3. MAXIMUM OUTPUT RATE vs FILTER CONFIGURATION

MODE	DECIMATION (R)	REAL OR COMPLEX	SYMMETRIC OR ASYMMETRIC	NUMBER OF TAPS	MAXIMUM INPUT SAMPLE RATE (MHz)	MAXIMUM OUTPUT RATE (MHz)
Bypass	1	Real	-	1	17.5 (Note 3)	17.5 (Note 3)
Filter	2	Real	Symmetric	127	1.060606	0.530303
Filter	3	Real	Symmetric	127	1.567164	0.522388
Filter	4	Real	Symmetric	127	2.058824	0.514706
Filter	5	Real	Symmetric	127	2.536232	0.507246
Filter	6	Real	Symmetric	127	3.000000	0.500000
Filter	7	Real	Symmetric	127	3.450704	0.492958
Filter	8	Real	Symmetric	127	3.888889	0.486111
Filter	9	Real	Symmetric	127	4.315068	0.479452
Filter	10	Real	Symmetric	127	4.729730	0.472973
Filter	11	Real	Symmetric	127	5.133333	0.466667
Filter	12	Real	Symmetric	127	5.526316	0.460526
Filter	13	Real	Symmetric	127	5.909091	0.454545
Filter	14	Real	Symmetric	127	6.282051	0.448718
Filter	15	Real	Symmetric	127	6.645570	0.443038
Filter	16	Real	Symmetric	127	7.000000	0.4375 (Note 4)

#### NOTES:

- 3. Assumes a 35MHz PROCCLK.
- 4. 0.129630 output rate for a decimation of 16 is not possible due to limitations in later stages.

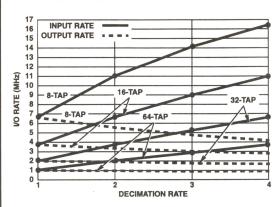


FIGURE 7. DETERMINING MAXIMUM INPUT AND OUTPUT RATES BASED ON FILTER DECIMATION FOR A 8, 16, 32 AND 64 TAP FILTER ( $F_S = 33$ MHz)

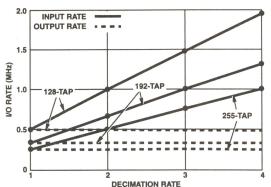


FIGURE 8. DETERMINING MAXIMUM INPUT AND OUTPUT RATES, BASED ON FILTER DECIMATION FOR A 127, 192 AND 255 TAP FILTER ( $F_S = 33 \text{MHz}$ )

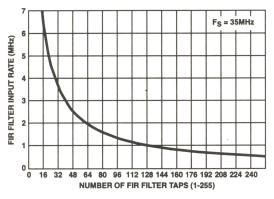


FIGURE 9. THE NUMBER OF FILTER TAPS VS INPUT RATE FOR A DECIMATION OF 2

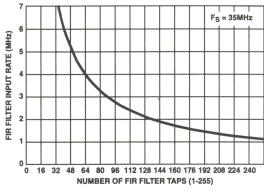


FIGURE 10. THE NUMBER OF FILTER TAPS VS INPUT RATE FOR A DECIMATION OF 4

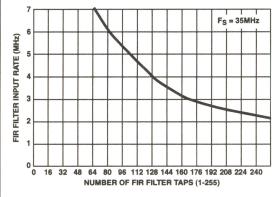


FIGURE 11. THE NUMBER OF FILTER TAPS VS INPUT RATE FOR A DECIMATION OF 8

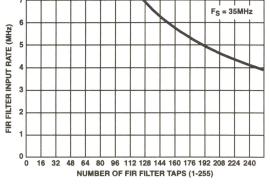


FIGURE 12. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 16

#### AGC Multipliers

The data multiplication by the AGC involves multiplexing and delay circuitry resulting an output to input clock ratio of 6. Since the circuitry is clocked by PROCCLK, the maximum input rate is 35MHz, yielding a maximum output rate of 35/6 = 5.833MHz. Table 4 details this rate transfer.

TABLE 4. MAXIMUM INPUT AND OUTPUT RATES OF THE AGC MULTIPLIERS

MAX INPUT RATE (MHz)	MAX OUTPUT RATE (MHz)
35.00	5.833

# Polyphase Filters and Interpolating Halfband Filters

The polyphase filter and interpolating halfband filters will be considered a block. The polyphase filter is clocked by PROCCLK and enabled by the Re-Sampler NCO, which is set via processor control. Equation 7 details the calculation of the Re-Sampler NCO Carry Output frequency.

The output sample rate is determined by the Re-Sample NCO.

$$F_{CO} = F_S \times (TCF + TOF)/2^{32}$$
 (EQ. 7)

where  $F_{CO}$  = ;  $F_{S}$  = Re-Sampler NCO Clock Frequency (FIR output rate); TCF = Timing Center Frequency; and TOF = Timing Offset Frequency. TCF is processor programmed and TOF is input via the serial interface. Both TCF and TOF are 32-bit word values (0 < x < 4,294,967,295). The maximum output rate is 0.999. . . X input rate.

The halfband filters are clocked by PROCCLK.

Emptying the filters requires a certain number of PROC-CLKs, depending on which filters are enabled. The number of cycles, as well as the maximum I/O rates, are shown in Table 5.

TABLE 5. POLYPHASE FILTER AND INTERPOLATING HALF-BAND FILTER MAX OUTPUT RATES

BAND TIETEN MAX COTT OF TIATES						
MODE	CLOCK CYCLES	INPUT RATE (MHz)	INTERPO- LATION RATE	MAX OUTPUT RATE (MHz)		
Bypass	0	35.000	-	35.000		
Polyphase Filter	6	35/6 = 5.833	-	NCO (5.833)		
Polyphase and 1 Halfband Filter	13	35/13 = 2.692	2	NCO (5.385)		
Polyphase and 2 Halfband Filters	23	35/23 = 1.522	4	NCO (6.087)		
1 Halfband Filter	7	35/7 = 5.00	2	10.000		
2 Halfband Filters	17	35/17 = 2.059	4	8.235		

#### Cartesian to Polar Converter

The maximum output rate of the Cartesian to Polar Converter is a function of the precision desired in the answer. This circuitry is clocked by PROCCLK, so the maximum input rate is 35MHz. To obtain full accuracy of 16 bits, 17 clocks are required. The maximum output rate is 35/17 = 2.059MHz.

Table 6 details the output resolution based on the maximum output clock, assuming the input is sampled at 28MHz. Six bits may be sufficient for many applications. In general the resolution on the phase output will need to be greater than on the magnitude output.

TABLE 6. BIT RESOLUTION AS A FUNCTION OF INPUT/OUT-PUT RATE INTO THE CONVERTER

INPUT RATE (MHz)	OUTPUT RATE (MHz)	MAGNITUDE OUTPUT ERROR (%)	PHASE OUTPUT ACCURACY (DEGREES)
35	35.000	-	-
35	17.500	14.12	45
35	11.667	3.98	26.565
35	8.750	1.03	14.036
35	7.000	0.26	7.125
35	5.833	0.07	3.576
35	5.00	0.02	1.790
35	4.375	0.004	0.895
35	3.889	Less than 0.004	0.447
35	3.500	Less than 0.004	0.224
35	3.182	Less than 0.004	0.112
35	2.916	Less than 0.004	0.056
35	2.688	Less than 0.004	0.028
35	2.500	Less than 0.004	0.014
35	2.333	Less than 0.004	0.007
35	2.188	Less than 0.004	0.003

NOTE: This table assumes full scale input.

#### References

For Harris documents available on the web, see http://www.semi.harris.com/ Harris AnswerFAX (407) 724-7800.

[1] HSP50214 Data Sheet, Harris Semiconductor, Answer-FAX Doc. No. 4266.



No. TB302

December 1991

# Harris Digital Signal Processing

## **Notice To Specification Change HSP48901**

Author: Clay Olmstead

This is notification of a change to the  $T_{LCS}$  specification of the HSP48901. The new specification is:

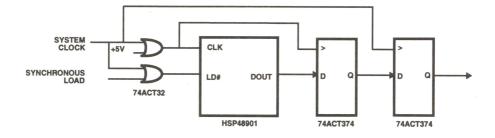
,		-30 (3	BOMHz)	-20 (20MHz)								
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX							
LD# Setup Time	T <sub>LCS</sub>	31	T <sub>CYCLE</sub> +2	40	T <sub>CYCLE</sub> +2							
The Old Specification was:												
		-30 (3	BOMHz)	-20 (20MHz)								
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX							
LD# Setup Time	T <sub>LCS</sub>	28	-	40	-							

This parameter specifies the timing for changing the configuration of the part while processing data. This applies mainly to loading coefficients and changing coefficient banks. It

does not affect customers who change the part's configuration asynchronously or during periods when no valid data is processed.

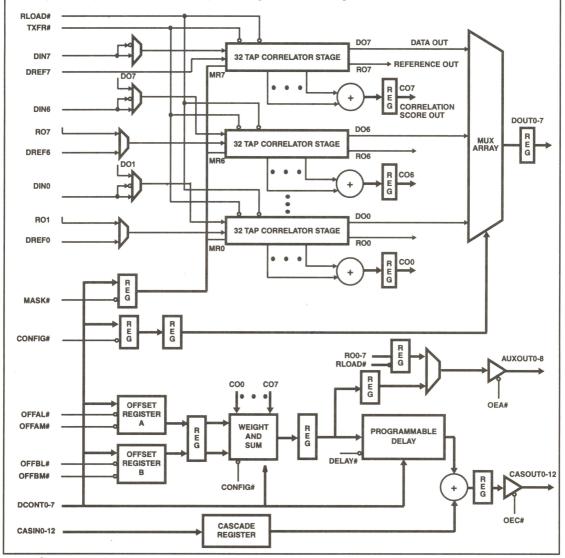
This change is being made to achieve a closer match with the specifications for the parts that would be used to generate these signals.

A circuit for implementing this function with the new timing is shown below. The two 74ACT32 gates shown must be in the same package in order to minimize timing skew between them. Using this circuit, the skew will typically be less than 2 nanoseconds over temperature, so that the rising edge of LD# will be nearly coincident with the rising edge of CLK, causing LD# to take effect during the following clock cycle.By cascading two 74ACT374's, the timing skew with the rest of the system is eliminated; the first synchronizes the output with the local (delayed) clock, while the second synchronizes the output with the rest of the system.



The block diagram in Figure 1 of the data sheet for the HSP45256 Correlator is incorrect; the corrected block diagram is shown below. The difference is in the registers on the data input and output. The function of the chip is unchanged,

but the pipeline delay from DIN to DOUT is different from that which would have been calculated using the previous block diagram. The circuits in the back of the data sheet showing various configurations of cascaded correlators are correct.



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No. TB306 January 1994

# Harris Digital Signal Processing

## **Cascading Multiple HSP45256 Correlators**

When multiple correlators are cascaded for longer reference data sets, the Programmable Delay is used to adjust the timing between chips so that they can be connected with no external hardware. Figure 1 shows the portions of two correlators that would be active when two 45256's are set up to perform a 1 bit, 512 tap correlation. In this case, DOUT7 of one correlator is connected to DIN7 of the next one; CASOUT0- 12 of the first part are connected to CASIN0-12 of the second one. (See the HSP45256 data sheet.) Figure 2 shows the relevant portions of two Correlators which are

cascaded together; in this example, each is configured as 1x256. In the interest of clarity, the only portions shown are the final stage of the first correlator and the first stage of the second one. The data sample number at each stage for a given clock cycle is shown in the boxed in numbers. Note that the Programmable Delay of the first part is set to a delay of one (the minimum possible) and the second part is set to a delay of two. This assures that the proper samples are added in the Cascade Summer.

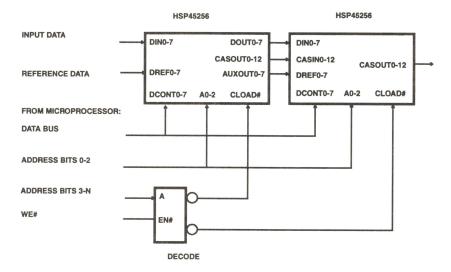


FIGURE 1. CIRCUIT BLOCK DIAGRAM

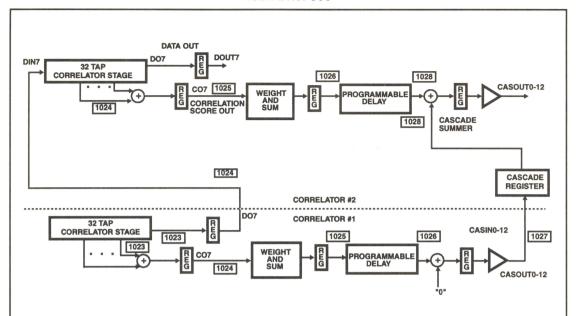


FIGURE 2. CASCADED CORRELATORS SHOWING RELATIVE CLOCK CYCLES.



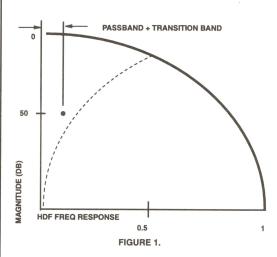
No. TB308 January 1994

# Harris Digital Signal Processing

# HSP43220 DECI•MATE Design Rule Checks

In order to maximize effectiveness of DECI•MATE software there are two design rule checks that need some in depth discussion. Once these crosschecks are understood the usefulness of DECI•MATE and the DDF will improve because filters that were previously thought unrealizable are in fact achievable. Consider the following normalized HDF response (to first null).

In Figure 1 the dotted line represents aliasing. The point defined by stopband attenuation (50dB) and the sum of the passband and transitionband frequencies, must not cross the dotted line. Sometimes in MANUAL design mode you will come upon a filter in which you can vary either the transitionband or passband frequencies or attenuation by just a few Hz or a few dB, and find the filter jumps from unrealizable due to many taps to a viable filter that only needs a few taps. This may be due to crossing the aliasing curve. This in effect, renders the HDF ineffective and DECI•MATE is trying to accomplish everything in the FIR. You may also get the error message "HDF unrealizable".



Violation of the second rule exhibits similar symptoms.

Figure 2 illustrates the design rule check that the HDF rolloff should not violate the passband attenuation spec. This condition can occur in a variety of ways, if the passband is a large percentage of the output rate, if the passband attenuation is very small, if most of the decimation is being done in the HDF (which brings the first null of the HDF response in close to the passband region). The number of stages in the HDF also determines the rolloff of the HDF response. This design rule check is done with no knowledge of the type of FIR being used, STANDARD, IMPORTED, or PRECOMP. Therefore switching to a PRECOMP, or IMPORTED FIR will not alleviate a violation of this rule. The PRECOMP FIR can in fact reduce the HDF rolloff effect when the rolloff is within the limits stated above.

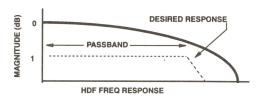


FIGURE 2.

It is important the user understand which rule is being violated because the first one is hard and fast, must not be violated. The second is correctable with additional work (manual design of FIR on other software). It is of course possible that both rules are being broken. There are two simple tests that can be done to identify what the problem is. If the difficulty is with HDF rolloff in the passband (rule 2), then relaxing the passband attenuation will allow the software to generate a filter.

If the problem is intrusion of stopband attenuation past the dotted line (rule 1), then changing the passband attenuation will not solve anything. Try reducing the stopband attenuation, a little, then a lot, if this results in a filter design then the problem is rule 1.

#### Solutions

If DECI+MATE was in design mode MANUAL when the problem occurred then the user can adjust the design parameters (input rate, output rate, passband, transition band, passband attenuation, stopband), or the HDF filter parameters to achieve a filter. For problems with rule 1 try any of the following: higher input rate, narrower passband, less stopband attenuation, less HDF decimation, more HDF stages. For problems with rule 2 try any of the following: higher input rate, higher output rate, narrower passband, looser passband attenuation, less HDF decimation, fewer HDF stages.

In general, if DECI•MATE was in design mode AUTO when the problem occurred, then going to manual design mode and playing with HDF stages, or HDF decimation will not produce any better results (with the one exception noted below as "Special Case"). The user then must decide if the system can tolerate the relaxed design parameters (input rate, output rate, passband, transition band, passband attenuation, stopband attenuation) needed to achieve a realizable filter. If not, the user will need to perform a manual design of the HDF and FIR filter parameters.

#### Special Case

For those users who have the option of low system decimation rates there are some alternatives. For those with system decimation rates of less than 10, trying varying combinations of HDF decimation and HDF stages may prove worth while. Also, for those that can have system decimation of 16 or less, bypassing the HDF (setting HDF decimation to 1 and HDF stages to 0) and using only the FIR may be beneficial.



No. TB309 January 1994

# Harris Digital Signal Processing

## Notes on Using the HSP43220

#### **Operation And Programming**

Typical operation of the part using DECI•MATE software is as follows. RESET# is held low long enough to satisfy the specification of 4 clocks for the slowest clock. Coming out of reset both start inputs must be high. After waiting the specified reset recovery time the registers are then loaded. H\_Register1: H\_DRATE register will accept values from 0 to 1023. H\_BYP is set as desired. F\_CLA is typically set to a zero, F\_DIS is set to a zero. H\_Register2: H\_STAGES is set as desired, a six or seven may be entered and will be interpreted as a five. H GROWTH is entered as specified in the data sheet or DECI•MATE with acceptable values from 0 to 63, with values above 50, the most significant bits of the input data will be dropped. F\_Register: F\_TAPS will accept values from 2 to 511. DECI•MATE always generates odd tap filters, therefore the value N to be entered will typically be even. F DRATE, enter value between 0 and 15 as desired. F ESYM, as with most filter design software, DECI.MATE always generates even symmetric filters, enter a one. F\_BYP, enter as desired. F\_0AD, typically set to a zero, used only for non-symmetric filters and for verifying filter coefficients. FC\_Register, for a the value N loaded in the F TAPS register there will be (N/2)+1 coefficients to be entered for odd length filters and N/2 coefficients for even length filters. It takes two writes to load each coefficient. Internally the number of coefficients loaded is recorded and used to determine the length of the filter, NOT F TAPS. F TAPS is used to offset a read pointer in the data RAM and to determine if an odd or even number of taps is being done to properly handle the center tap.

With programming of the HSP43220, the part must be started as described in the data sheet. If STARTIN# is used, it will be the third rising edge of CK\_IN (from STARTIN# active) that the DATA\_IN pins will start accepting data. If ASTARTIN# is used it will be the fifth rising edge of CK\_IN.

If at any time RESET# goes active, or glitches low, the above procedure must be repeated (except for reloading coefficients). Also see reprogramming.

#### Implementing Non-symmetric Filters

The HSP43220 can implement up to a 256 tap non-symmetric filter. Correct programming procedures are as follows. By definition the number of coefficients loaded is equal to the

number of taps (N). The F\_TAPS is set equal to 2N-1, and F\_0AD and F\_SYM are set to a one. The remaining registers are loaded normally.

#### Data\_in Bus

In many cases the source of information to be fed into the DATA\_IN pins will be less than 16 bits wide. The recommended configuration is to connect the input bus to the most significant bits of DATA\_IN and to tie unused DATA\_IN pins to GND. In some systems there will be available a 16 bit bus to connect to the DATA\_IN pins but the full range of the bus is not being used. For example the upper 4 bits are always sign bits. This can be adjusted for in software by setting the growth for three more than normal. Even if the HDF is to be bypassed this can be accomplished by manually putting the HDF in bypass. This is done by setting H\_STAGES and H\_DRATE to 0. For the case described above, H\_GROWTH would be set to 50+3, or 53. This pushes the 3 extra sign bits off the top of the data shifter.

#### Output Format

As stated on page 4-5 of the DECI.MATE manual, the FIR coefficients are computed using the Parks-McClellan (Remez) method and then scaled by the inverse of the HDF scale factor as well as an additional factor which accounts for the maximal ripple gain of the derived FIR. As a result, the output format is as follows. DATA\_OUT bits 0-15 are the most significant bits. If OUT SELH is held high, then DATA OUT bits 16-23 are simply sign extension, if held low they are the LSB extension, for a total of 24 bits of resolution. For those that wish more bits of resolution the sign extension bits can be used. This may be accomplished through the users own software or the coefficients from DECI+MATE may be scaled. This is accomplished by determining the magnitude of the largest coefficient, and then multiplying all coefficients by the factor 0.999999/mag. The coefficients must then be quantized to 20 bits. This results in the magnitude of the largest coefficient being about 0.999999, the largest representable value. This procedure also allows the realization of filters of greater than 96dB attenuation since it reduces quantization effects. The new position of the decimal point in the output will be moved into the sign extension bits with its exact position being dependent on the coefficients.

#### Bypass Modes Of The HDF And FIR

When the H\_BYP bit is set, H\_Register2 bits are affected as follows. H\_GROWTH is set to 50, H\_STAGES is set to zero. The clock divider is disabled so CK\_DEC=CK\_IN. The H\_Register1 value H\_DRATE is not altered by setting the H\_BYP bit. H\_Register2 must be reloaded after H\_BYP has been returned to a zero.

With H\_BYP set to a one, the feedback paths in the integrators and the holding registers in the comb are zeroed. The 16 bits of chip input data pass through the HDF section unaltered. As always, the first data sample out of the HDF (after reset/startup) is a zero due to resetting of the data paths. Because the FIR section has several operations to complete between rising edges of CK\_DEC it is necessary for FIR\_CK to be faster than CK\_IN as described in the data sheet. The duty cycle of CK\_IN must meet the conditions described Tech Brief TB312. DECIMATE can be used to determine the necessary frequency of FIR\_CK or equation 1.0 in the data sheet can be solved for the case of HDF in bypass by setting Hdec=1.

When the F\_BYP bit is set the FIR filter is configured as a 3 tap, even symmetric filter, no decimation with one input to the pre-adder set to zero (same side as if F\_0AD was set). The output of the coefficient ram is forced to 00004H to aid in positioning the result in the accumulator. The output multiplexes are set by the F BYP bit to output data from the bottom of the accumulator. For a 3 tap filter there are two multiply/accumulate (MAC) cycles. The data flow is as follows. A new piece of data becomes available at the HDF output as signaled by a rising edge of CK\_DEC. The FIR is signaled and the data is written into the data ram. The first MAC cycle begins. From the data ram the new data and some old data are read. The new data is added to zero in the pre-adder, then multiplied by the coefficient, and then accumulated with a zero (because start of new FIR cycle). The second MAC cycle starts one FIR\_CK cycle after the first. Two old pieces of data are read from ram. But two zeros are input to the pre-adder because of zeroing the other side of the pre-adder at the center of odd length tap filters. The resulting zero is multiplied by the coefficient and accumulated. The accumulator results are sent to the output pins along with a DATA\_RDY.

#### Reprogramming

After initial startup of the HSP43220 the FIR section can be reprogrammed using the F\_DIS bit of H\_Register1. When writing H\_Register1 be sure to maintain the same values in bits 0-10, H\_DRATE and H\_BYP. When the F\_DIS bit is written the FIR section will terminate a FIR cycle if one is in progress, no DATA\_RDY is issued. The FIR section is disabled from performing multiply/accumulate cycles. The FIR\_CK must continue to run. The HDF section continues to operate and its output continues to be written into the data ram. By letting the HDF section continue to run the synchro-

nous operation of multiple DDFs is maintained. By continuing to load the data ram a transient response is avoided when the FIR section is restarted. Writing the F\_DIS bit also resets the coefficient ram address pointer to zero (to allow for reloading coefficients) and enables writing of the coefficient ram (writing is disabled when FIR section is enabled). Once the bit is set and at least two rising edges of FIR\_CK have occurred, the user may then reconfigure the FIR section as desired. The FIR section can be re-enabled either by writing F\_DIS to a zero or by generating a high to low transition on either of the start inputs, which automatically clears F\_DIS.

For those users that wish to clear the HDF data paths before bringing in a new signal, or for those that wish to change HDF programming and have multiple DDFs running synchronously, activating the RESET# input is recommended. Reprogramming the DDF and restarting will be necessary. The coefficient ram is not corrupted by reset and will not need to be reloaded unless new coefficients are needed. It is also possible to reconfigure the HDF without losing synchronization between DDFs if CK\_IN is stopped (high or low) during writing of the registers. For single chip applications or where synchronization is not a concern, the HDF registers can be written on the fly. This will result in a transient response and changing HDF registers at regular intervals in an attempt to achieve fractional decimation rates with the chip is not recommended.

#### Internal Decimation

The total decimation in the DDF, also called the system decimation, is equal to the product of Hdec and Fdec. The output rate of the DDF will be equal to CK\_IN divided by system decimation, regardless of FIR\_CK speed. The time from the start of the DDF to the first DATA\_RDY may not be the same as time between DATA\_RDYs. To the user the FIR decimation appears at the FIR output. That means the output of the DDF is equivalent to using a standard FIR filter and only looking at every Nth output for FIR decimation of N.

In the HDF the counter used for decimation is initialized to Hdec. The first CK\_DEC (internal to chip) will occur about Hdec CK\_INs after the part is started. The FIR decimation counter is initialized to zero and the first CK\_DEC will always cause an FIR cycle which generates a DATA\_RDY about taps/2 FIR\_CKs later. Thus the time delay from start of the DDF to the first DATA\_RDY is about CK\_IN period times Hdec plus FIR CK period times taps/2.

#### Transient Response

After reset, after changing the source of input data, or after re-programming the HDF, the output of the DDF will have a transient response until the data ram is sufficiently full of "valid" data. There is no transient response when only the FIR is reprogrammed using the FIR disable bit in the control register. It is impossible to predict exactly when the transient is complete as the answer depends on the FIR filter coefficients as well as new data values relative to old data values in both the FIR and HDF.

First the integrator stage(s) must be flushed of old data (except when reset is used). The number of stages and growth will influence this. But in general the flushing of the integrator stages is small compared to the remainder of the chip. For N stages it will take N CK\_DEC cycles to flush all the holding registers in the comb. The number of taps deternines how many locations of the data ram needs to be written with new data. The equation for the number of input samples needed to complete the transient response is:

number of input samples = Hdec(taps + N)

The number of output samples that are part of the transient response is:

number of output samples = taps/Fdec + N/Fdec

Because the center coefficients are usually much larger than outer coefficients the transient response is done before all the ram locations are filled. In some cases in half the time described above.

The simulator in DECI+MATE assumes all unwritten ram locations are zero and may not necessarily reflect the startup transient of the DDF. This can be overcome by making sure leading zeros are input ahead of the signal for both the simulator and the chip. For the case of the data input changing (one signal followed by another) the simulator will match the DDFs transient response. You cannot simulate reprogramming the DDF.

#### Clock Inputs

The requirement that the two input clocks be synchronous is driven by the handshake circuitry between the HDF and FIR section. In this circuitry there is a flip/flop which has CK\_DEC as the data input and FIR\_CK as the clock input. Based on the theory that it is impossible to design a synchronizer that

is 100% immune to metastable conditions it was needed to specify the FIR CK and CK IN inputs as synchronous inputs. Metastable condition refers to when the flop output oscillates due to the data and clock changing simultaneously. For the user that finds it very inconvenient to use synchronous clocks, or for one that does not wish to use clocks that are integer multiples (which is by definition not synchronous), the use of a local synchronizer can be of benefit. This option puts the risks and control of metastability at the board level under user control. One example of this might be a user that has designed the needed filter in DECI+MATE and the required FIR CK is 35Mhz with a CK IN rate of 5Mhz. Through the use of equation 1.0 in the data sheet the minimum FIR CK is 32Mhz. The software chose 35Mhz because it is smallest integer multiple (30Mhz would have been to slow). Assume the fastest available speed grade of HSP43220 is 33Mhz. The user may then use a local synchronizer to make the filter realizable. The following is just one example of a local synchronizer that re-aligns the system clock edges to create a synchronous CK IN.

The following restrictions are needed to insure maximum performance.

- System clock must have high and low times greater than oscillator period.
- Have to still meet DATA\_IN setup and hold times at DDF pins. Use of Q bar output makes this easier.
- Realistically the maximum system clock rate is one sixth of oscillator.

Node A can still become metastable but it has one oscillator period to become stable. The user has access to node A and can make his own evaluation as to if the circuit performance is acceptable. In general the higher the speed capabilities of the flip/flops used makes for faster resolution of the metastable condition if it should occur.

# M TeaBrief

No. TB311 January 1994

# Harris Digital Signal Processing

# HSP43220 - Design of Filters With Output Rates <2(Passband + Transition)

One of the design rule checks in DECI•MATE is that the output rate must be greater than 2 times the sum of passband + transition band. For the informed user, violation of this rule is a valid design choice. Suppression of this rule check in DECI•MATE is not possible, but design of such a filter using DECI•MATE is possible.

The general solution is to use DECI•MATE to design a filter with an output rate that is twice the desired rate, or a integer multiple of the desired rate that is >2(pass + trans). Outside of the Design Module the FIR decimation rate is increase by the factor needed to achieve the desired output rate. The new filter response is obtained graphically.

Consider a filter with a passband of 70KHz and a transition band of 60KHz. The desired output rate is 200KHz. DECI•MATE requires an output rate of >260KHz, an output rate of 400KHz is chosen (see Figure 1 below and FILTER 1 page 2).

By increasing the FIR decimation by a factor of 2 the folding point  $(F_S/2)$  is moved and the desired output rate is obtained. The filter response can be generated graphically. The aliasing component is represented by the dotted line (see Figure 2 below).

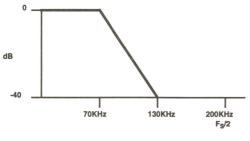
Notice in FILTER 1 the stopband attenuation was limited to 40dB (FIR\_CK=CK\_IN). Because the FIR decimation was increased from 5 to 10, there are more taps available with FIR\_CK=20MHz. Using equation 2.0 from the 43220 data sheet, we see how many taps are available.

$$\#Taps = \left(\frac{2 \times 20(10)10}{20} - 10 - 4\right) = 172$$

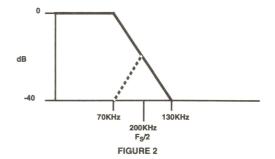
We can therefore use FILTER 2 which uses 151 taps and has 96dB stopband. The part will of course be programmed for FIR decimation rate of 10 and an FIR\_CK of 20MHz is used.

To correctly simulate or generate PROM files for the "new filter" the \*.DAR file must be edited. The corrected value for FDRATE on line 1 column 4 is entered. The correct output rate and FIR\_CK rate are entered on the next to the last and the last line of the \*.DAR file.

The above procedure works for standard or Precomp FIR. Remember the maximum FIR decimation rate is 16.







#### Tech Brief 311

DESIGN	MODULE	-	SIMULATOR	MODULE	A Superior Control of	PROM	MODULE
		HS	SP43220 DDF	FILTER	SPECIFICATION		
D	Filter File	:	filter1.DDI	P			
1	Input Sample Rate		20	MHZ	Design Mode	:	AUTO
В	Output Rate		400	kHz	Generate Report	:	YES
	Passband	:	70	kHz	Display Response	9 :	LOG
C	Transition Band	:	60	kHz	Save Freq Respon	nses:	NO
	Passband Atten	:	0.1	dB	Save FIR Respons	se :	NO
I	Stopband Atten	:	40	dB			
.							
	FIR Type	:	STANDARD				
м							
A							
	HDF Order	:	2	FIR	Input Rate :		2 MHz
т	HDF Decimation	:	10	FIR	Clock (min) :		
1	HDF Scale Factor	:	0.78125	FIR	Order :		81
Е				FIR	Decimation :		5

FIGURE 3. FILTER DESIGN USING STANDARD TECHNIQUE.

DESIG	N MODULE	SIMULATOR	MODULE	PROM	MODULE
	l HS	P43220 DDF	FILTER SPECIFICATION		
D	Filter File :				
1	Input Sample Rate:	20		:	AUTO
E	Output Rate :	400	kHz Generate Report	:	YES
1 1	Passband :	70	kHz Display Response	в :	LOG
c	Transition Band :	60	kHz Save Freq Respon	nses:	NO
	Passband Atten :	0.1			
1	Stopband Atten :	96		-	
	FIR Type :	STANDARD			
м		O I I I I I I I I I I I I I I I I I I I			
A					
	HDF Order :	4	FIR Input Rate :		2 MHz
т	HDF Decimation :		FIR Clock (min) :		40 MHz
1 - 1	HDF Scale Factor :				151
Е	indi boule ractor .	0.31035	FIR Decimation :		5
	1				

FIGURE 4. FILTER DESIGN DISREGARDING FIR CLOCK (MIN).

# M TearBrief

No. TB312 Janua

January 1994

# Harris Digital Signal Processing

## HDF Bypass in the HSP43220

When HDF bypass is selected special timing restrictions exist for signal CK\_IN.

When no decimation is selected for the HDF section either by setting the H\_BYP bit to 1 or by setting H\_DRATE = 0, the timing requirements for CK\_IN require special consideration. The FIR section of the chip is signaled that there is new data from the HDF when a transition is detected on the signal CK\_DEC (see Figure 1). Failure to meet the timing requirements on CK\_IN when  $H_{\rm d}=1$  results in no or erratic DATA\_RDY pulses being issued.

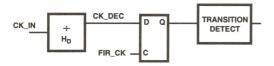


FIGURE 1. CK\_DEC GENERATION AND DETECTION

When  $H_d > 1$ , the internal divider sets the high or low time of CK\_DEC equal to the period of CK\_IN, guaranteeing that CK\_DEC will be detected by FIR\_CK (Figure 2). When  $H_d = 1$ , the duty cycle of CK\_DEC is the same as CK\_IN as shown in Figure 3.

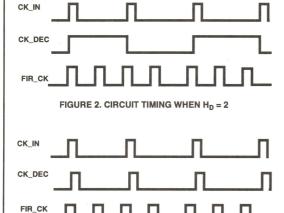


FIGURE 3. CIRCUIT TIMING WHEN  $H_D = 1$ 

By definition of valid part operation, any time  $H_d=1$  the FIR\_CK will be at least 2 times the frequency of CK\_IN.

In the example shown in Figure 3, the state of CK\_DEC is always a zero when sampled by the rising edge of FIR\_CK. To insure that signal CK\_DEC is sampled in both its high and low state by the flipflop requires careful control of CK\_IN. The most obvious solution is for the high or low time of CK\_IN to be a minimum of one period of FIR\_CK. This guarantees sampling both a 1 and a 0 no matter what the phase relation of FIR\_CK and CK\_IN is.

There is a specified range of allowed phase offset between FIR\_CK and CK\_IN as given in the AC specifications by spec TSK. Using this spec with 2ns of margin yields the following minimum CK\_IN high or low time with setup and hold as specified.

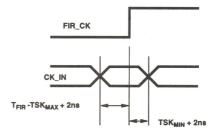


FIGURE 4.

For a 25Mhz part the minimum high or low time requirement for CK\_IN is 19ns (when  $H_d=1$ ) given the above timing (independent of clock frequencies).

For the typical user, guaranteeing the CK\_IN high and low times greater than or equal to the period of FIR\_CK will be the most desirable solution in terms of hardware. For the user with additional system constraints, such as those that vary the frequency of CK\_IN but hold a high or low time constant, the above timing yields the most flexible solution.



No. TB313 January 1994

# Harris Digital Signal Processing

## **Reading Out FIR Coefficients From the HSP43220**

There are two methods of reading out the FIR coefficients. With method 1, a single coefficient is output with every DATA\_RDY. With method 2, a coefficient is output every rising edge of FIR\_CK.

#### Method 1

The premise is to configure the 43220 to look like a FIR filter, input an impulse, and observe the coefficients at the output.

First, the FIR section of the chip is programmed for no decimation ( $F_{\text{dec} = 1}$ ). This may require changing H\_DRATE from the original setup (see BYPASSING THE HDF). The F\_REG is written for the original value of F\_TAPS, F\_BYP = 0, F\_0AD = 0, F\_ESYM = 1, F\_DRATE = 0, and F\_CLA = 0 (H\_REG1). The FC\_REG is loaded normally. The FIR data ram must be sufficiently filled with zeros before the impulse. The minimum number of zeros to clock into the 43220 is Hdee\*taps. The pin OUTSELH should be set to a zero. An impulse, value 0800H, is input and the coefficients will be output in the order, outer coeff through center coeff and back to outer coeff. The 20 bit coefficients are output on the 24 DATA OUT pins with the format shown below.

#### Method 2

This method allows for reading out the FIR coefficients in less time than method 1 but requires the system to have the ability to capture the value on the DATA\_OUT pins every FIR\_CK. DATA\_RDY has no meaning in this mode. The HDF section must be configured as described in the BYPASSING THE HDF portion of this memo. For an NTAP filter, the value for F\_TAPS is either NTAPS or NTAPS-1, which ever is odd. For example, for either a 67 or 68 tap filter, F\_TAPS = 67. Set other FIR parameters as follows: F\_BYP = 0, F\_0AD = 1, F\_ESYM = 1, F\_DRATE = 0, and F\_CLA = 1

Instead of an impulse, the DATA\_IN pins are held at the value 0800H. After (taps/2)(Hdec+10) CK\_IN cycles, all the coefficients will be output on consecutive FIR\_CKs in the order in which they were written.

#### Bypassing The HDF

Use the following equation to determine the  $H_{dec}$  required with  $F_{dec} = 1$  (if  $F_{dec}$  was equal to 1 in the original filter then the correct  $H_{dec}$  is already known).

$$H_{DEC} = \frac{CK_{IN}[(taps/2) + 5]}{FIR CK}$$

Round the resultant value for  $H_{\mbox{\scriptsize dec}}$  up to the next integer value.

For  $H_{dec}=1$ , set  $H_{\_BYP}=1$ , in this case an impulse is defined as the DATA\_IN pins having the value 0800H for one rising edge of CK\_IN.

For  $H_{dec}=N$ , N>1, set HBYP = 0,  $H_{DRATE}=N$ -1,  $H_{GROWTH}=50$ ,  $H_{STAGES}=0$ . In this case an impulse is defined as the DATA\_IN pins having the value 0800H for N rising edges of CK\_IN (see Figure 1).

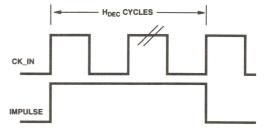


FIGURE 1

**OUTPUT FORMAT** 

DATA\_OUT

23																							
c7	c6	c5	c4	с3	c2	c1	c0	SE	SE	SE	SE	c19	c18	c17	c16	c15	c14	c13	c12	c11	c10	c9	c8

SE - SIGN EXTENSION

# a leastief

No. TB314 January 1994

# Harris Digital Signal Processing

# Quadrature Down Conversion with the HSP45116, HSP43168 and HSP43220

The Harris HSP45116 Numerically Controlled Oscillator/Modulator (NCOM) can be combined with a low pass filter to perform down conversion on a digital signal. The NCOM rotates the spectrum of a real or complex signal and outputs a complex data stream. The signal of interest is now at base band, so that the output can be low pass filtered to eliminate unwanted signals (Figure 1).

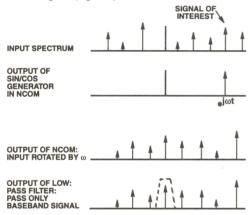


FIGURE 1. DOWN CONVERSION SPECTRAL PLOTS

If the spectrum of the signal of interest is sufficiently narrow, the output sample rate of the filter can be reduced to ease the throughput requirements of the downstream processing. Reducing the sample rate of a signal is commonly known as decimation. The input sample rate divided by the output sample rate is known as the decimation factor, or simply decimation. Note that decimation by one is equivalent to no decimation, and decimation by less than one is undefined. For the purposes of this discussion, base band signals will be divided into two categories: wide band signals, where the decimation factor is 16 or less, and narrow band signals, where the decimation is greater than 16.

#### Narrow Band Down Conversion

For narrow band output signals, Harris has a three chip set with a filter that is capable of decimation by up to 16,384. Figure 2 shows how the NCOM and HSP43220 Decimating Digital Filter (DDF) are connected to perform down conver-

sion and real to quadrature conversion of an input signal. This is a generalized block diagram which can be used as the basis for a specific design.

Several assumptions were made in defining this block diagram. Among these assumptions are:

- Input and output data are sixteen bits. Users requiring less than that should keep bit 15 as the most significant bit, grounding the unused bits on the input of the NCOM. In all cases, bits 0 through 15 on the output of the NCOM should be connected to the sixteen input bits of the DDF. To select the output bits of the DDF, note that if the input is a cosine at frequency A and the NCOM is tuned to frequency B and the phase offset is 0, then the real and imaginary outputs of the NCOM at sample n are:
- Real Output: cos(An)cos(Bn) = [cos(An-Bn) + cos(An+Bn)]
- Imaginary Output: cos(An)sin(Bn) = [sin(An+Bn) sin(An-Bn)]
- Note that the factor of <sup>1</sup>/<sub>2</sub> has been omitted. The output of the Complex Multiplier is shifted left by one bit internally.
   For this reason, both the real and imaginary outputs have the same magnitude as the input.
- The Phase Register is selected to control the phase of the NCOM (as opposed to MOD0-1) and is initialized along with the center frequency. In this example, the LOAD# signal is not exercised, so the initial phase of the NCOM is unknown.
- To shift the positive component of a real input signal to base band, the Center Frequency Register of the NCOM is set to a negative number.
- The Offset Frequency Register, Timer Accumulator and Complex Accumulator of the NCOM are not used.
- The filter clocks of the two DDFs are driven at a higher rate than the input data clocks. For many applications the FIR\_CK, CK\_IN and CLK signals can all be connected together. In this case the divide by N block is not needed.
- The DDFs are reset and started asynchronously with a pulse generator that receives asynchronous commands from an outside source and drives the two DDFs simultaneously. The DDF receiving the asynchronous start pulse performs the synchronization and starts the other part at the proper time.

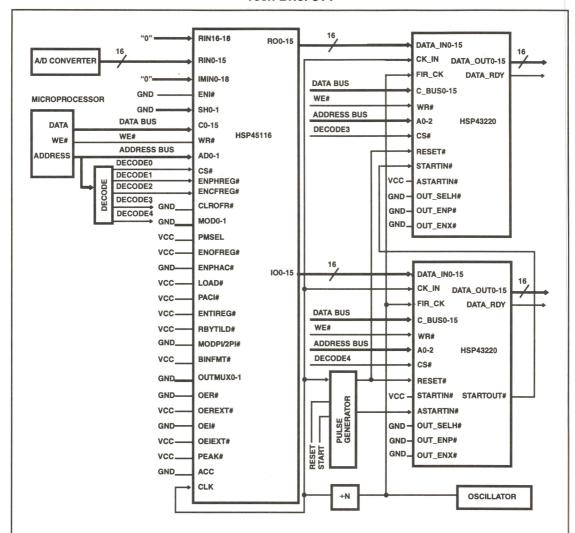


FIGURE 2. BLOCK DIAGRAM FOR QUADRATURE DOWN CONVERSION WITH HSP45116 AND HSP43220.

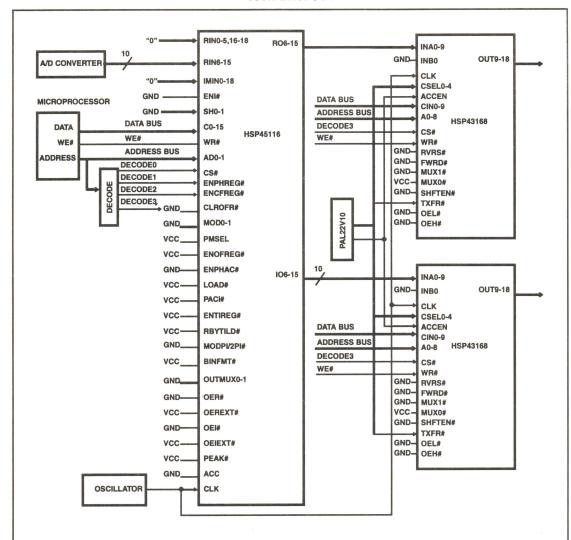


FIGURE 3. BLOCK DIAGRAM FOR WIDE BAND QUADRATURE DOWN CONVERSION WITH HSP45116 AND HSP43168.

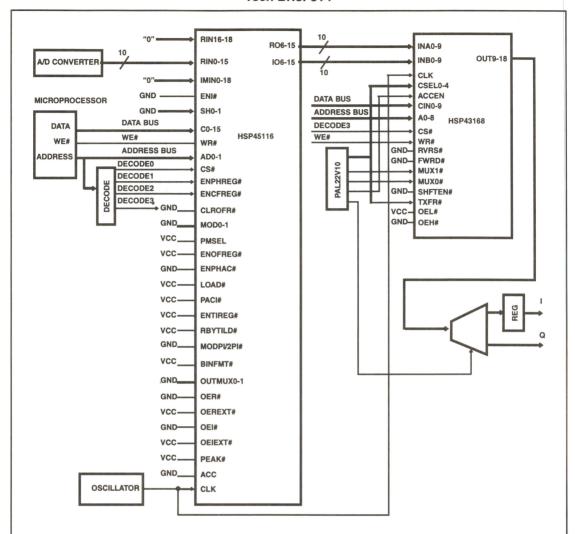


FIGURE 4. BLOCK DIAGRAM FOR WIDE BAND DOWN CONVERSION WITH HSP45116 AND HSP43168.

#### Wide Band Down Conversion

Figures 3 and 4 show how the NCOM and HSP43168 Dual FIR Filter (Dual FIR) are connected to perform down conversion and real to quadrature conversion of an input signal. Because the Dual FIR can implement either one or two filters, two block diagrams are shown. Figure 3 shows the case where each 43168 is implementing a single filter. The maximum number of coefficients in this case is 16 times the decimation factor for each filter. Figure 4 shows the same configuration with the exception that the Dual FIR is now configured as two independent filters, each with a maximum length of 8 times the decimation factor.

These are generalized block diagrams which can be used as the basis for a specific design. Note that they do not represent detailed schematics with all gates represented. For instance, the control signals are driven with a single PAL22V10 operating as a self contained state machine; it reality, the 22V10 may not have enough gates to generate all the necessary output sequences; in that case, it would be necessary to have a counter generate the states and use the PAL to decode the counter output, generate the control signals to the 43168, and reset the counter when the sequence is completed.

The design parameters of these circuits are:

- Input data is 10 bits. Users requiring less than that should keep bit 15 as the most significant bit of the NCOM, grounding the unused bits on the input. In all cases, bits 6 through 15 on the output of the NCOM should be connected to the input bits of the Dual. To select the output bits of the Dual, note that if the input is a cosine at frequency A and the NCOM is tuned to frequency B and the phase offset is 0, then the real and imaginary outputs of the NCOM at sample n are:
- Real Output: cos(An)cos(Bn) = [cos(An-Bn) + cos(An+Bn)]
- Imaginary Output: cos(An)sin(Bn) = [sin(An+Bn) sin(An-Bn)]
- Note that the factor of <sup>1</sup>/<sub>2</sub> has been omitted. The output of the Complex Multiplier is shifted left by one bit internally.
   For this reason, both the real and imaginary outputs have the same magnitude as the input.

- The Phase Register is selected to control the phase of the NCOM (as opposed to MOD0-1) and is initialized along with the center frequency. In this example, the LOAD# signal is not exercised, so the initial phase of the NCOM is unknown.
- To shift the positive component of a real input signal to base band, the Center Frequency Register of the NCOM is set to a negative number.
- The Offset Frequency Register, Timer Accumulator and Complex Accumulator of the NCOM are not used.
- The decimation rate in the Dual FIRs is greater than one.
   For no decimation, TXFR# should be grounded. Note that
  the maximum number of coefficients in the 43168 is eight
  or sixteen times the decimation rate, depending on the
  mode (see above).

#### Combined Narrow And Wide Band

In some applications, it is necessary to pass both wide and narrow band signals. In this case, both the HSP43220 and HSP43168 can be used in parallel, with the user selecting the output of either set of chips, depending on the characteristics of the signal of interest. Figure 5 shows this application, with most of the control signals eliminated for clarity. (These signals can be derived from the previous block diagrams.) In addition, note that the input data clock (CK\_IN) and the FIR clock (FIR\_CK) of the DDF have been connected together. This configuration is applicable when the input data rate is sufficiently high to allow the filter to operate at this rate also. If this is not the case, the divide by N circuit used in Figure 2 could be used, with the high speed clock driving the FIR\_CK pins and the divided down clock used for all other clocks in the circuit.

#### **New Products**

Now available from Harris are the HSP50016 Digital Down Converter, which is a single chip quadrature down converter and low pass filter (Figure 6). In addition, the HSP43216 Half Band Filter allows the user to double the input sample rate of the NCOM for real signals (Figure 7). Contact your local Harris sales office or representative for more details on these and other new products from Harris.

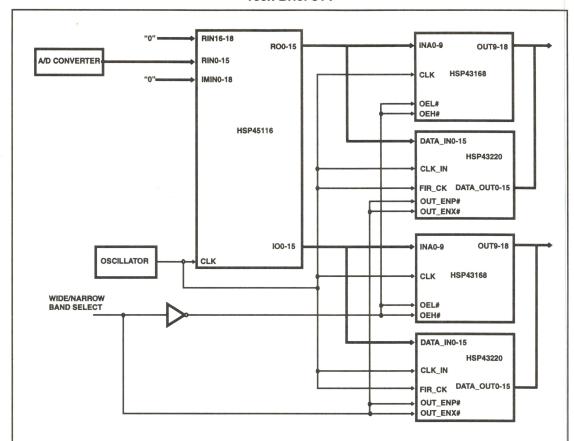


FIGURE 5. BLOCK DIAGRAM FOR QUADRATURE DOWN CONVERSION WITH HSP45116, HSP43220 AND HSP43168

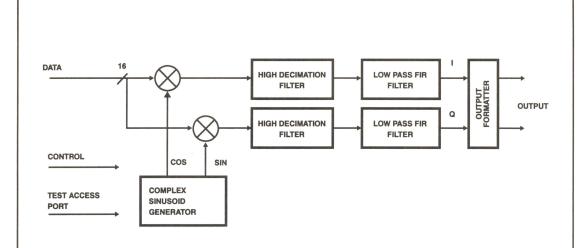


FIGURE 6. BLOCK DIAGRAM OF HSP50016 DIGITAL DOWN CONVERTER

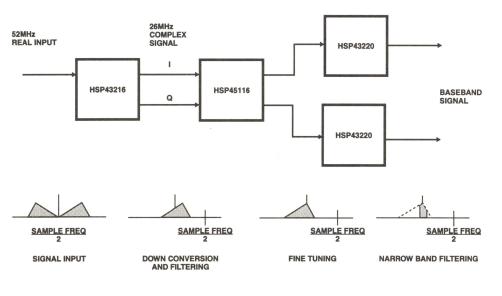


FIGURE 7. HALF BAND FILTER IN QUADRATURE DOWN CONVERSION



No. TB315 May 1993

# Harris Digital Signal Processing

# Processing Signals At Increased Sample Rates With Multiple HSP45116's

It is possible to generate signals with sample rates higher than the rated speed of the HSP45116 Numerically Controlled Oscillator/Modulator by using two parts. Each NCOM is clocked at half the sample rate of the signal to be generated, and the frequency of each is set to half the desired frequency. The phase register of one NCOM is then set to offset the phase of its output by one half of a sample period. The vector inputs and outputs of the two parts are then multiplexed together to form a signal at twice the frequency that would normally be possible; see Figure 1.

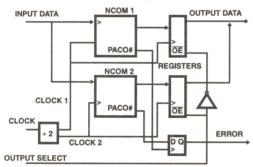
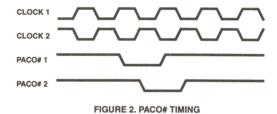


FIGURE 1. CIRCUIT BLOCK DIAGRAM

The value to be put into the phase register is one half of the sum of the center and offset frequency registers. This means that the phase offset between the two NCOMs is limited to the 16 bit resolution of the phase register, which limits the frequency resolution of the complete circuit to 15 bits.

The proper operation of this circuit can be verified by observing the PACO# outputs of the two NCOMs. Since PACO# is the inverted output of the phase accumulator and the phase offset is added to the output of the phase accumulator register, the alignment of the PACO# pulses out of the two parts will not be affected by phase offsets (see HSP45116 data sheet, Figure 1). The timing of the PACO# pulses is shown in Figure 2. The flip flop connected to the PACO# outputs of NCOM 1 and NCOM 2 as shown in figure1 will detect an error in this alignment. Note that the only causes for PACO# misalignment are improper configuration of the NCOMs or circuit noise which is severe enough to cause the parts to false trigger. Should the error signal go active, there will most likely be a problem with the entire circuit.



# M TeenBrief

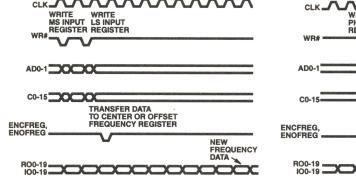
No. TB316 January 1994

# Harris Digital Signal Processing

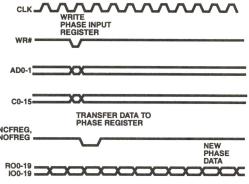
## Pipeline Delay Through the HSP45116

The following timing diagrams show the pipeline delays through the HSP45116 NCOM from the time that data is applied to the inputs until the outputs are affected by the

change. The delay is shown as a number of clock cycles, with no attempt made to accurately represent the setup and hold times or the clock to output delays.







**FIGURE 2. PHASE TO OUTPUT DELAY** 

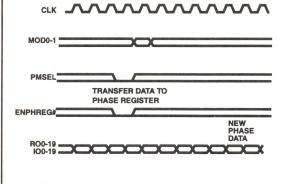


FIGURE 3. PHASE MODULATION TO OUTPUT DELAY

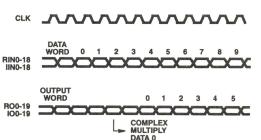


FIGURE 4. VECTOR INPUT TO OUTPUT DELAY



**No. TB317** January 1994

# Harris Digital Signal Processing

### Pipeline Delay Through the HSP45106

The following timing diagrams show the pipeline delays through the HSP45106 NCO16 from the time that data is applied to the inputs until the outputs are affected by the

change. The delay is shown as a number of clock cycles, with no attempt made to accurately represent the setup and hold times or the clock to output delays.

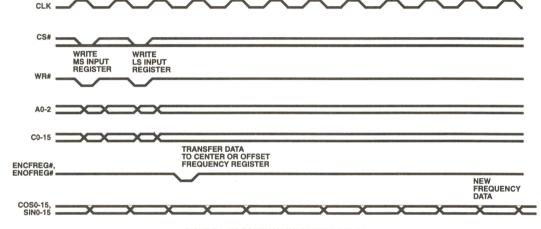


FIGURE 1. FREQUENCY TO OUTPUT DELAY

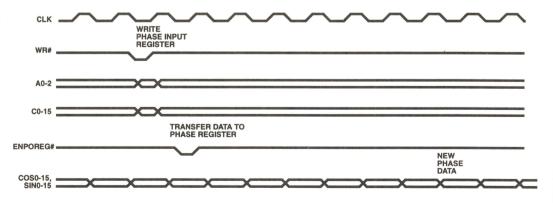


FIGURE 2. PHASE TO OUTPUT DELAY

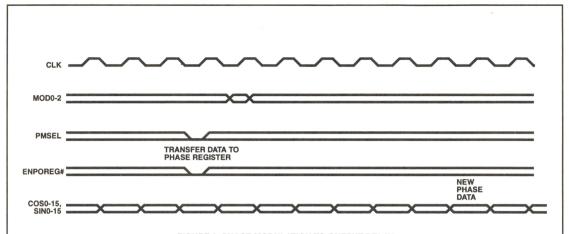


FIGURE 3. PHASE MODULATION TO OUTPUT DELAY



No. TB318 January 1994

# Harris Digital Signal Processing

### The NCO as a Stable, Accurate Synthesizer

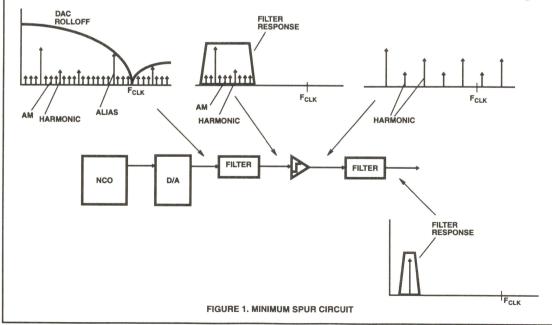
### Low Jitter Frequency Reference

In communication and other circuits, it is often necessary to produce an accurate reference signal whose frequency and phase can be precisely controlled in real time. The Numerically Controlled Oscillator (NCO) is ideally suited for this purpose. For some applications, the output reference signal is a square wave, so the temptation is to use only the MSB of the NCO output. This is useful in low frequency applications such as motor controllers, but is inadequate for most communications tasks. This is because the zero crossings of this signal can vary by one period of the input clock from one pulse to the next, which creates an unacceptable amount of jitter in the output. For example, if the NCO is clocked at 30MHz, the jitter is 33nsec. For a 1MHz square wave, this results in 12° of phase litter. The straightforward solution is to use an NCO with a much higher clock rate. This is not cost effective for applications requiring phase litter of less than 5nsec, however, since it requires a sample rate of 200 Mega Samples Per Second, (MSPS), which drives the user to an ECL NCO.

A much less costly circuit which solves this problem is shown in Figure 1. The output of the comparator is a square wave with much less jitter than the NCO alone. The basic idea is that the sampled sine wave output of the NCO is converted to a smooth sine wave, which is converted back to a square wave with a comparator. In the circuit shown, the comparator drives a filter, which attenuates the odd order harmonics so that the final output of the circuit is a sine wave. The upper limit on the purity of the sine wave is also much better than that of the NCO, as will be seen below.

### The primary sources of error in this circuit are:

In the NCO, spurs are classified as either AM or PM. PM spurs are due to truncation of the phase in calculating the sine and cosine. If M = number of bits into the input of the Sine/Cosine Generator, the PM spur level is -6M + 5.17dB[1]. The AM spurs are due to amplitude quantization on the output of the NCO. If the number of NCO output bits is N, the AM spur level is approximately equal to -6.02N - 1.76dB. [1] There will also be jitter due to the clock oscillator driving the



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NCO, but since it is only the short term jitter, not the long term stability of the oscillator that contributes to phase noise, this will be negligible if a reasonably good oscillator is used.

The DAC introduces additional spurs, which come from three sources: intermodulation spurs due to non-linearities in the DAC; a spur at the clock oscillator frequency due to clock feed-through; and power supply noise. The DAC also faithfully reproduces the aliases and harmonics that are unavoidable products of the NCO due to the digital nature of the output.

The filter on the output of the DAC eliminates the clock feed through, aliases due to the sampled nature of the NCO output and most of the AM spurs are eliminated with the bandpass. Spurs within the pass band are unchanged. The spectrum of the DAC output is a tone surrounded by spurs and noise in the frequency band corresponding to the pass band of the filter with negligible noise elsewhere. The area comprised of the tone, spurs and noise is known as the pedestal.

The input of the comparator is a relatively clean sine wave which the comparator converts into a square wave. This limiting action eliminates the AM spurs but has no effect on the PM spurs. For this reason, the number of bits used on the output of the NCO and the input of the DAC has little measurable effect on the output. The primary contributions to errors on the output of the comparator are the PM spurs on its input, which are passed through relatively unaffected, and power supply noise, which is attenuated by the power supply rejection of the comparator. If the filter on the input of the comparator did not remove the aliases and clock feed through, then the comparator will generate intermodulation components. This makes a good filter and a careful frequency plan essential.

If the desired output of the circuit is a sine wave rather than a square wave, the output of the comparator is filtered to extract the fundamental - that is, to suppress the odd order harmonics of the square wave signal. Note that this signal is much cleaner than the output of the first filter, since the comparator has removed the AM spurs.

The circuit shown here is often used to generate the reference tone for an indirect loop PLL synthesizer. In this case, the output of this circuit is fed into one input of a mixer, with the other input of the mixer driven by a high frequency VCO. The output of the mixer is a high frequency tone. The phase noise at the output of the mixer due to the noise in the reference circuit will be equal to the spur level of the reference circuit plus 20\*log10(output frequency/NCO frequency). For example, using the 45106 as a 5MHz reference for a 1GHz synthesizer, the spurs on the output of the reference would increase by 20log10(200), so the output spur level would be -114 + 46 = -68dBc at 1GHz. The NCO frequency resolution is 0.008Hz at 33 MSPS, so the tuning resolution of the synthesizer is 200(0.008) = 1.6Hz. Finer resolution can be obtained by cascading the Time Accumulator with the Phase Accumulator. (See below.)

### **Extended Frequency Resolution**

The phase accumulator of the HSP45106 (NCO16) is 32bits wide. This corresponds to a frequency resolution of (Sample Frequency)/2<sup>32</sup>. For a 25 MSPS sample rate, this results in an output frequency resolution of 0.006Hz. In certain applications, there is a requirement for much greater resolution. The NCO16 can address these applications using the Time Accumulator as an extension of the Phase Accumulator, Frequency resolutions of up to 64bits can be obtained in this configuration. Using the previous example of a 25MHz clock, the frequency resolution is 25MHz/2<sup>64</sup> = 1.35picoHertz. Using the parts in this configuration requires a small change to the external control logic: the Timer Accumulator register must be loaded over the control bus interface. This mode of operation has no effect on any of the other performance parameters, such as spurious free dynamic range, phase resolution, etc.

To configure the HSP45106 for this application, the setup shown in Figure 2. Note that the Timer Accumulator output, TICO#, is connected to the Phase Accumulator input, PACI#. To set the output frequency of the part, the Center Frequency Register and the Timer Accumulator must be loaded. Assuming that the Offset Register is not used, the equation for calculating the output frequency is now:

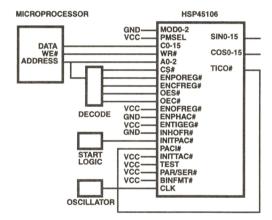


FIGURE 2. EXTENDED FREQUENCY RESOLUTION CIRCUIT

Center Frequency =

CLK Frequency x ((Center Frequency Register / 2<sup>32</sup>)

+ (Timer Accumulator Register / 264)

In this equation, the contents of the value in the Center Frequency Register is a two's complement number, i.e., the part tunes from -(CLK Frequency) / 2 to +(CLK Frequency) / 2. The value in the Timer Accumulator is an unsigned number.

It is unsigned because it provides the carry in to the Phase Accumulator, which is always added to the LSB of the current phase value.

The user should note that there is a flip flop between the Time Accumulator carry out and the TICO# pin, and another flip flop between the PACI# pin and the Phase Accumulator carry input. This will cause a two clock cycle delay between the carry out of the timer into the carry in of the accumulator. This will only have an effect on the output when the frequency register is updated; in effect, the Time Accumulator lags the Phase Accumulator by two clock cycles. If this is a concern, this can be compensated for by loading the input registers for both accumulators, then toggling ENTIREG# two clock cycles before ENCFREG#.

While the internal architecture of the HSP45116 NCOM and the HSP45106 NCO16 are very similar, this application works better with the NCO16 for two reasons. The first is that on the NCO16, the timer is loaded using a unique pin, rather than sharing this function with the ROM bypass line. This means that the output of the NCO16 is always valid, instead of having erroneous results on the output whenever the timer is updated. The second is that with the NCO16, the data for the various registers is downloaded into separate input registers, which can be downloaded into the operating registers with the ENXXREG# pulses. With the NCOM, there is only one 32bit input register, which must be downloaded into the

appropriate operating register before the next value can be input into the part. In this application, it means that the user can adjust the phase between the register updates with the NCO16 but not with the NCOM.

### Example

The circuit used to verify this equation is shown in Figure 2. The clock oscillator frequency was measured at 25.24102MHz. In order to achieve an output frequency of 1.000000Hz, the center frequency was set to hexadecimal AA, the offset frequency set to 0, and the Timer Accumulator set to hexadecimal 28880000. A frequency counter was attached to bit 15 of the cosine output. The actual frequency out varied from 0.9999999 to 1.0000003 as the oscillator drifted with time. A more stable oscillator would yield more predictable results. Note that going through the calculations results in an output frequency of 1.000006Hz. The difference is due to the fact that the oscillator frequency measurement was only carried out to 7 digits, but the counter used in this example had 8 digits.

### References

[1] Cercas, Francisco A. B., Tomlinson, M and Albuquerque, A. A. Designing with Digital Frequency Synthesizers, Proceedings of RF Expo East, 1990

# m Teersrief

No. TB319 January 1994

# Harris Digital Signal Processing

### Reading the Phase Accumulator of the HSP45106

The block diagram shown below illustrates the method of reading the phase accumulator of the NCO16 from a microprocessor. The setup shown is very similar to that used when the part is used for generating a complex sinusoid, except that the internal SIN/COS lookup is bypassed by putting a logic 1 on the TEST pin. While the TEST pin is high, the phase accumulator continues to drive the inputs of the SIN/COS Generator while the most significant 28 bits of the phase accumulator are multiplexed out onto the output pins. Because of this, the part can be operated in two modes, one where the SIN/COS Generator is permanently bypassed, and one where the phase accumulator output is brought out to the outputs as a check.

Figure 1 shows the circuit for reading out the phase accumulator all the time. In this case, a microprocessor loads the frequency and phase registers of the NCO16. This is fairly straightforward, except the Start Logic block, which needs to be synchronous to the oscillator clock and the microprocessor interface. This has been left as an undefined function, since it is dependent on the implementation. Also note that COSO-15 are connected up, although only COS4-15 are valid in this application. The microprocessor reads the sine and cosine data busses as if they were RAMs, using the decoded address bus to select one or the other.

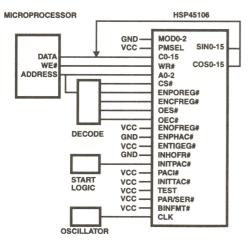
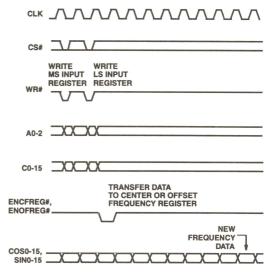


FIGURE 1. CIRCUIT FOR READING PHASE ACCUMULATOR OF NCO16

The timing for loading the center frequency register and seeing the output on COS0-15 and SIN0-15 is shown in Figure 2. This timing is independent of whether the output data represents the phase accumulator data or the SIN/COS Generator output.



**FIGURE 2. NCO16 PIPELINE DELAY** 

When the output of the NCO16 is to be switched back and forth between sine/cosine and the phase accumulator, a circuit such as the one shown in Figure 3 could be used. In this case, the sinusoidal output cannot be interrupted, so the phase accumulator must be read out between samples. This is possible due to the fact that the TEST signal is simply the control line for a multiplexer on the output of the SIN/COS Generator, but carries with it a limitation on the maximum possible clock rate. Since TEST is a synchronous input, the output of the NCO16 must be either driven by the SIN/COS Generator or the phase accumulator for an entire clock cycle. Therefore, the part must be driven at twice the desired speed at all times so there is a clock cycle available for TEST when necessary. Note that the processor must be driven from the same clock that generates the NCO clock in order to maintain synchronous operation. The timing is identical to that shown in Figure 2 with CLK replaced with CLK/2.

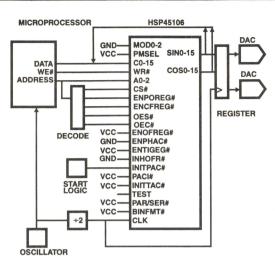


FIGURE 3. CIRCUIT FOR READING PHASE ACCUMULATOR OF NCO16 WHILE GENERATING SINUSOID

# narris Semiconductor



No. TB327 November 1994

# Harris Digital Signal Processing

## Using the HSP45116 as a Complex Multiplier Accumulator

Author: John Fakatselis

### Introduction

The Harris HSP45116 Numerically Controlled Oscillator/ Modulator can be also used as a high speed 16-Bit Multiplier/Accumulator (CMAC). This technical briefing details the part configuration to perform such function; it provides a functional block diagram of the interface circuit that is required, and it shows the timing diagrams of the data and control signals involved.

The features of the HSP45116 configured as a CMAC include:

- · 25MHz Output Rate of the Complex Vector
- · 16-Bit Complex Inputs
- · 20-Bit Complex Output
- 32-Bit Internal Accumulator
- Two's Complement or Offset Binary (Unsigned) Outputs Available
- Peak Bit Growth in the Accumulator Available Through Status Pins

The HSP45116 combines a high performance quadrature numerically controlled oscillator and a high speed 16-bit complex multiplier/accumulator.

To utilize the HSP45116 as a CMAC only, a number of input pins have to be set at the logic levels as specified on the attached pin description table. These pin assignments are necessary, in order to bypass the operations of the Numerically Controlled Oscillator (NCO) and advance the data directly to the CMAC portion of the device. In order to accomplish proper data alignment within the part some external interface circuitry is required as illustrated on the functional block diagram of Figure 1.

Each complex input includes a real and an imaginary component. Notice that while the first complex input vector is being clocked in the HSP45116 through the parallel input ports RIN0-18 and IMIN0-18, the second complex input vector is being clocked from a single 16-bit input port (C0-15), by clocking one complex component at the time. This implies that the clock of the second complex vector (WR#) must be twice the frequency of the clock for the first complex vector (CLK).

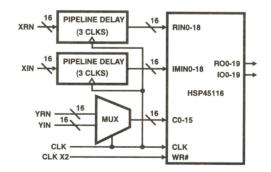
The exact timing relationships between inputs, outputs, control signals, and clocks are shown on Figure 2. Given the timing diagram of figure 2 and the external interface circuit as shown on Figure 1 then full data alignment can be accomplished.

Figure 3, shows an internal block diagram of the device. The block diagram illustrates the additional data path of the sec-

ond complex vector being input through the C0-15 port follows before it lines up with the first complex vector internal to the device. In addition this second input vector (C0-15) must be transferred to the CMAC without being altered by any of the NCO HSP45116 functions.

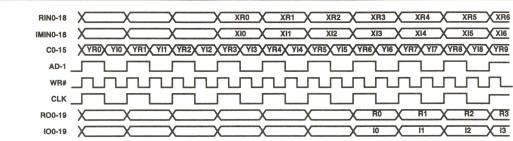
The highlighted signal path of the second complex vector (C0-15), shows the three additional registers that the data is being clocked through compared with the direct path (to the CMAC) of the first complex vector of the RIN0-18 and IMIN0-18 inputs. This three register delay derives the requirement for the external pipeline delays as shown on figure 1 for the data alignment of the two complex vectors. In addition the suggested pin configuration, on the attached pin configuration table, allows the C0-15 data to flow unaltered by any NCO operation to the inputs of the CMAC. By following this internal data path, one can verify that the suggested logic levels assure the transparent transfer of data to the CMAC portion of the HSP45116.

Note that the maximum data size of the second complex input vector is 16 bits, for each of the real and imaginary componets, while the data size of the first complex input through RIN0-18 and IMIN0-18 can accommodate a longer length.



NOTE: Refer to Figure 2 for timing relationship between input signals, control signals and clocks.

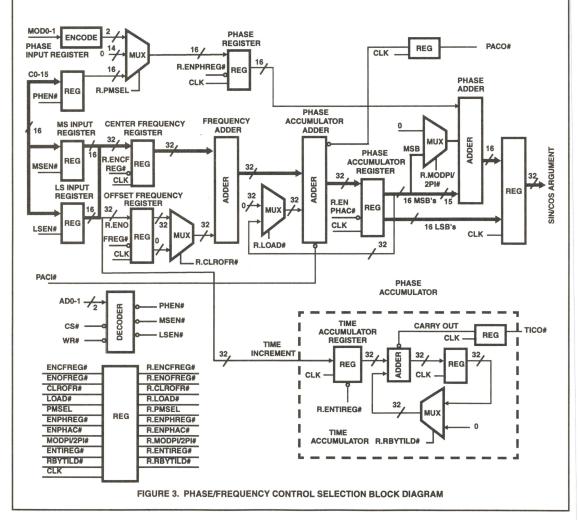
FIGURE 1. INTERFACE BLOCK DIAGRAM UTILIZING THE HSP45116 AS A CMAC



#### NOTES:

- Timing assumes no accumulations of the complex product. Accumulations can be accomplished by controlling the ACC input (refer to data book 302B).
- 2. XR(n) = This represents the real data of the first input vector.
- 3. XI(n) = This represents the imaginary data of the first input vector.
- 4. YR(n) = This represents the real data of the second input vector.
- 5. YI(n) = This represents the imaginary data of the second input vector.

FIGURE 2. TIMING DIAGRAM OF THE HSP45116 USED AS A CMAC



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### Tech Brief 327

### Pin Description Table

NAME	NUMBER	TYPE	DESCRIPTION
V <sub>CC</sub>	A1, A9, A15, G1, J15, Q1, Q7, Q15	ı	
GND	A8, A14, B1, H1, H15, P15, Q2, Q8	ı	
C0-15	N8-11, P8-13, Q9-14	1	Input for real and imaginary for one of the complex vectors.
AD0-1	N7, P7	1	Selects to write alternatively (R) or (I) data from C0-15
CS#	P6	1	
WR#	Q6	ı	Writes C0-15 data, must be twice the clock frequency.
CLK	Q5	1	
ENPHREG#	. M1	T	Logic "0"
ENOFREG#	N1	ı	Logic "1"
ENCRFEG#	N5	T	Logic "0"
ENPHAC#	Q3	ı	Logic "0"
ENTIREG#	P5	ı	Logic "0"
ENI#	Q4	1	Logic "0"
MODPI/2PI#	N6	ı	Logic "0"
CLROFR#	P4	1	Logic "0"
LOAD#	N4	1	Logic "0"
MOD0-1	M3, N3	T	Both pins at Logic "0"
PMSEL	P3 .	1	Logic "0"
RBYTILD#	L3	1	Logic "0"
PACI#	P2	1	Logic "1"
PACO3	L13	0	
TICO3	P1	0	
RIN0-18	C1, C2, D1, D2, E1-3, F1-3, G2, G3, H2, H3, J1-3, K1, K2	ı	Input for real data for one of the input vectors with the imaginary data at IMIN0-8.
IMIN0-18	A2-7, B2-7, C3-8, D3	1	Input for imaginary data for one of the input vectors with the real data at RIN0-18.
SH0-1	K3, L1	1	Shift control inputs. These lines control the input shifters of the RIN and IIN inputs of the complex multiplier. The shift controls are common to the shifters on both of the busses.
ACC	L2	I	Accumulate/dump control. This input controls the complex accumulators and their holding registers. When high, the accumulators accumulate and the holding registers are disabled. When low, the feedback in the accumulators is zeroed to cause the accumulators to load. The holding registers are enabled to clock in the results of the accumulation. This input is registered by CLK.
BINFMT#	N2	ı	This input is used to convert the two's complement output to offset binary (unsigned) for applications using D/A converters. When low, bits RO19 and IO19 are inverted from the internal two's complement representation. This input is registered by CLK.
PEAK#	M2	ı	This input enables the peak detect feature of the block floating point detector. When high, the maximum bit growth in the output holding registers is encoded and output on the DET0-1 pins. When the PEAK# input is asserted, the block floating point detector output will track the maximum growth in the holding registers, including the data in the holding registers at the time that PEAK# is activated.
OUTMUX0-1	N12, N13	1	Logic "0"

### Tech Brief 327

## Pin Description Table (Continued)

NAME	NUMBER	TYPE	DESCRIPTION
RO0-19	C15, D14, D15, E14, E15, F13-15, G13-15, H13, H14, J13, J14, K13-15, L15, M15		These three state outputs are controlled by OER# and OEREXT#. OUTMUX0-1 select the data output on the bus.
IO0-19	A10-13, B8-15, C9-14, D13, E13	0	Imaginary output data bus. These three state outputs are controlled by OEI# and OEIEXT#. OUTMUX0-1 select the data output on the bus.
DET0-1	N15, L14	0	These output pins indicate the number of bits of growth in the accumulators. While PEAK# is low, these pins indicate the peak growth. The detector examines bits 15-18, real and imaginary accumulator holding registers and bits 30-33 of the real and imaginary CMAC holding registers. The bits indicate the largest growth of the four registers.
OER#	P14	ı	Three-state control for bits RO0-15. Outputs are enabled when the line is low.
OEREXT#	M13	ı	Three-state control for bits RO16-19. Outputs are enabled when the line is low.
OEI#	M14	ı	Three-state control for bits IO0-15. Outputs are enabled when the line is low.
OEIEXT#	N14	ı	Three-state control for bits IO16-19. Outputs are enabled when the line is low.
RND#	N/A	I	Round Enable (Available on HSP45116A only). This input enables rounding of the output data precision from 9 to 20 bits (see HSP45116A Description and Operation). This input is active "low". This input must be tied either high or low.

# Marief References

No. TB336 February 1996

# Harris Digital Signal Processing

## 3x3 10-Bit Convolver Using the HSP43168

Authors: Guenter Kremser, Harris Munich; Rick Roberts, Harris Melbourne

### Introduction

The Harris HSP48908 2-D convolver has gained acceptance among customers as an excellent choice for implementing 8-bit 3x3 convolutional kernels. However, new applications in image processing, such as digital video broadcasting and medical imaging, demand higher bit resolutions. This technical brief shows how to implement a 3x3 10-bit kernel using the Harris HSP43168 (Dual FIR Filter) and HSP9501 (Delay Buffer). This technique is also applicable, with appropriate modifications, to convolutions requiring greater than 10-bit resolution.

### 3x3 10-Bit Kernel

Figure 1 shows the block diagram of the 3x3 10-bit convolutional kernel. Use is made of two HSP43168s and two HSP9501s. This configuration will operate up to clock speeds of 32MHz.

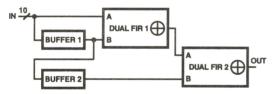


FIGURE 1. BLOCK DIAGRAM OF 3x3 10-BIT CONVOLUTIONAL KERNEL

### Theory of Operation

A 3x3 convolution is implemented as the sum of three row vector dot products. Dual FIR 1 implements the top two row vector dot products and Dual FIR 2 implements the bottom row vector dot product. The convolution sum is facilitated via the A input of Dual FIR 2 and is available at the output of Dual FIR 2.

The row vector coefficients are programmed as the first 3 coefficients of Dual FIR 1 A and B and Dual FIR 2 B. The first coefficient of Dual FIR 2 A has a value of 1.0 with all other coefficients set to zero. Both dual FIRs have the output programmed to A + B (i.e. MUX1-0 is equal to 01).

Row buffer 1 is programmed for a length commensurate with the image row pixel length (e.g. 1024 pixels) while buffer 2 is programmed for the image row pixel length plus five additional delays. These five additional delays are needed to compensate for the pipeline delay associated with Dual FIR 1 (e.g. 1024 + 5 = 1029).

Because of the rounding feature in both dual FIRs, there is no need for shifting the MSB position at the output. The appropriate rounding value is programmed into control address 001H, bits 8-5, and is easily derived.

### Summary

A solution is presented for implementing a 3x3 10-bit convolutional kernel which makes use of two HSP43168 dual FIRs, programmed for A + B output, and two HSP9501 row buffers. Dual FIR 1 A and B, in conjunction with Dual FIR 2 B, implement the row vector dot products, while Dual FIR 2 A provides a path for summing the three dot products to obtain the convolution sum.



### **No. TB325.1** January 1995

# Harris Data Acquisition

## Understanding Glitch in a High Speed D/A Converter

Authors: Juan Garcia and Stephen G. LaJeunesse

### Introduction

Today's high speed D/A converters are used in communications applications such as:

Frequency Hopping Radios Cellular Base Stations Direct Digital Synthesis

These converters need to provide good Spurious Free operation to ensure signal integrity and low inter-channel interference.

The glitch of a given DAC can limit the overall spectral performance of the converter and make it unusable. There are many definitions of this phenomena known as glitch and this article will try to explain them.

### Glitch Area

When a given converter is updated with a new data value the output of the DAC tries to generate a new output voltage. As shown in Figure 1 the output slews to a new final voltage. This step response contains glitch, and settling effects, that must die down in order to reach the new steady state output.

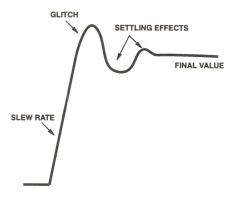
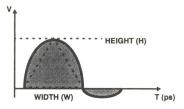


FIGURE 1. DAC OUTPUT RESPONSE

Glitch Area is the measure of the area under the first transient of the output of the D/A converter. The glitch is assumed to be triangular in shape and is calculated as shown in Figure 2.



GLITCH AREA = 1/2 (H X W)

### FIGURE 2. GLITCH AREA

The glitch is the first peak transient. Some manufacturers use the glitch 'doublet' theory where the specification given is a net glitch area

The glitch doublet sums the area of the initial glitch transient and the area of the settling effects. These areas are then added together to yield some very small unrealizable number by most board level designers.

The 'singlet' or peak glitch area is a more realistic specification for board and system level designers as they can more adequately evaluate the severity of the glitch.

### **Glitch Cause**

One cause of glitch is the time skew between bits of the incoming digital data. In a DAC that has no internal register, the time delta between logic inputs causes internal current sources to switch asynchronously resulting in a momentary surge in current. The HI5721 employs an internal register to synchronize the incoming data.

Typically the switching time of digital inputs are asymmetrical, meaning that the turn off time is faster than the turn on time. Unequal delay paths through the device can cause one current source to change before another.

To reduce this, an internal register is used to latch all the digital input data on one clock edge so as to synchronize them in time. Careful layout and sizing of the internal current sources also helps to maintain concurrent switching times.

#### **Reducing Glitch**

In traditional DACs the worst case glitch usually happens at the major transition i.e. 01 1111 1111 to 10 0000 0000. But in the HI5721, the worst case glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R/2R-segmented current source architecture, which decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range.

### **Deglitching Techniques**

Deglitching the output of a high speed converter is no trivial task. Figure 3 shows an ideal deglitching circuit. A deglitcher is a sample and hold that holds the previous conversion while the converter is settling to the new output. A deglitching sample and hold potentially could have a hold to track glitch, that can be larger than the DAC's glitch. The amplifiers in this circuit must be unity gain stable to 500MHz and have a settling time of 2ns for a 1V<sub>P-P</sub> swing to an error band of 0.1%.

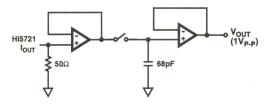


FIGURE 3. A CLASSIC D/A DEGLITCHING CIRCUIT

The on resistance of the switch must be less than  $2\Omega$  and have a leakage of less than 1pA to minimize droop. This is practically impossible with the switches available on the market today. The best way to reduce glitch is to optimize the high speed DAC design as done in the Harris HI5721.

### **Filtering Glitch**

Since the glitch is a transient event this leads designers to believe that a simple low pass filter can be used to eliminate or reduce the size of the glitch. In effect low pass filtering a glitch tends to "smear" the event and does little to remove the energy of the transient. Glitch contains many spectra from near DC up to and beyond the Nyquist sampling rate of the converter. By low pass filtering, the high frequency components of the glitch are removed but the main or majority of low frequency components are not.

This leaves a designer with a usable spectral window however, this technique usually results in a higher noise floor at low frequencies. Noise also increases closest to the cutoff frequency of the filter.

### Picking a Low Glitch D/A

The best methods for choosing a low glitch converter are to choose those that specify the first transient area and those converters that incorporate architectures to minimize glitch. Trying to remove the glitch from a 'glitchey' DAC is not trivial and can simply move the problem to other places as well as complicate the design.

### The HI5721's Peak Glitch

Although the HI5721 specifies a glitch doublet area of 1.5pV-sec (to meet specs quoted by other D/A manufacturers) the peak glitch is ~3.0pV-sec. Figures 4 and 5 show the typical glitch height and width.

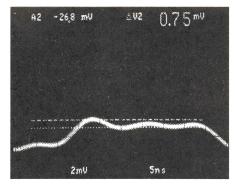


FIGURE 4. GLITCH HEIGHT Code  $64_D$  -  $60_D$ , Scope  $50\Omega$  GND

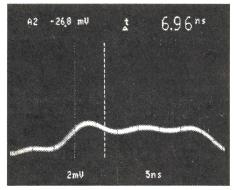


FIGURE 5. GLITCH WIDTH Code  $64_D$  -  $60_D$ , Scope  $50\Omega$  GND

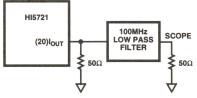


FIGURE 6. GLITCH TEST SETUP

### Summary

Testing standards are evolving and as technology improves the real specifications become evident. For state of the art D/A converters, the HI5721 provides designers with the lowest glitch performance, tested under the most stringent conditions.



**No. TB326** January 1995

# Harris Data Acquisition

# Measuring Spurious Free Dynamic Range in a D/A Converter

Authors: Juan Garcia, Stephen G. LaJeunesse, Douglas Bartow

### Introduction

As high speed DACs migrate into digital receivers and transmitters, spectral specifications become more important to the system designer. Specifications like Signal to Noise Ratio (SNR), Total Harmonic Distortion (THD), and Spurious Free Dynamic Range (SFDR) describe the frequency content of the non-ideal converter and how it will operate in a given system. SFDR has become one of the more important specifications that systems designers use to qualify a device for a given design.

### SFDR Definition

Spurious Free Dynamic Range is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of the difference in amplitude between the fundamental and the largest harmonically or non-harmonically related spur from DC to the full Nyquist bandwidth (half the DAC sampling rate, or f<sub>S</sub>/2). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog output of the DAC. Figure 1 shows how SFDR is measured correctly (SFDR is usually specified in dBc).

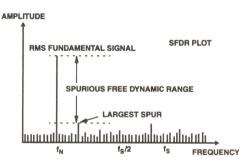


FIGURE 1. MEASURE OF SPURIOUS FREE DYNAMIC RANGE

### The IDEAL Converter

For a given D/A converter, what should a designer expect for a reasonable SFDR specification? In an ideal system, the worst case Signal to Noise Ratio is calculated by Equation 1:

$$SNR_{IDEAL} = 6.02 (N) + 1.76$$
 (EQ. 1)

where N is the number of bits of the converter.

The worst case Signal to Noise Ratio for a 10-bit ideal digital system is -62dB. This is the worst case spurious noise of the system with the assumption that the quantization noise is uniformly distributed. A digital system does not have spurious noise or distortion influencing spectral performance so SFDR equals the worst case Signal to Noise Ratio.

Unlike digital systems, D/A converters have many factors that detract from optimum spectral performance such as total harmonic distortion, non linearity, glitch, power supply noise, board layout, etc. For a D/A converter, the SFDR will always be less that the ideal SNR figure. For example, an SFDR of -58dBc is considered average performance for a real-world 10-bit DAC.

### SFDR Within a Window

Many manufacturers of high speed converters specify SFDR over a frequency spectrum that is less than the Nyquist bandwidth. By picking an arbitrary window size, the 2nd or 3rd harmonic are often not included in the measurement. Because many systems designers intend to use a narrow band pass filter around the fundamental signal, they are more interested in the spectral performance within a band that the filter will pass. However, having full knowledge of a DAC's spectral performance is essential to the selection of an appropriate band pass filter to remove the harmonics.

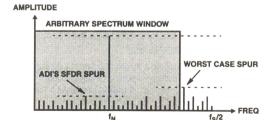


FIGURE 2. COMPETITORS SFDR

Figure 2 shows the method used by some DAC suppliers to measure SFDR. Utilizing this method, the fundamental frequency of  $f_{\rm N}$  and the span used to measure SFDR does not include the 2nd harmonic.

So what is valid for a true SFDR specification? The answer is both methods have merit and should be considered. A systems designer needs to know the full spectral performance of a given DAC up to the Nyquist bandwidth. The best way to show a DAC's actual performance is with a typical performance curve, showing spurs and spectral performance up to Nyquist. Curves, showing the arbitrary windows used by some DAC suppliers, are also of interest to many designers.

Figure 3 shows a typical performance plot of the Harris HI5721 10-bit DAC from DC to the full Nyquist bandwidth. Testing was performed with a 100MHz sample clock yielding a Nyquist bandwidth of 50MHz. The fundamental signal is sited at 5.0MHz and is attenuated by 20dB. The SFDR under these conditions was measured at -64dBc. The second harmonic is the only in-Nyquist band harmonic.

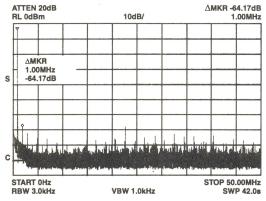


FIGURE 3. SFDR TO NYQUIST

Figure 4 shows a typical performance plot of the HI5721's SFDR within a window span of 5MHz. You will notice that all of the harmonically related spurs are outside this window. In this span the noise floor is down -81dBc.

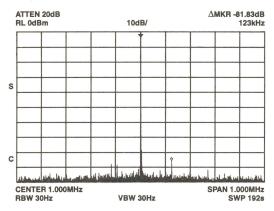


FIGURE 4. SFDR WITHIN A 1MHz SPAN

### **How to Improve SFDR**

SFDR is directly related to linearity and glitch performance of a DAC. The quantization noise of the converter (i.e., the number of bits) the converter can accurately represent will limit the overall dynamic range.

Glitch is a broad spectral event that has spurs throughout the Nyquist band starting at DC and continues up through the sampling frequency. Eliminating glitch is a difficult task at best. Designers can simplify their system design, by choosing a low-glitch DAC like the HI5721.

Other ways to improve SFDR are to slow down data and clock edge rates. A  $50\Omega$  shunt termination resistor on the clock line reduces the clock step size and provides proper termination. Since any noise on the clock line will degrade the DAC's performance dramatically, make clock lines as short as possible, and use proper termination.

Bypassing the converter is another method to improve overall SFDR performance in a DAC. A  $0.01\mu F$  capacitor paralleled with a  $0.1\mu F$  capacitor on all power supply pins provides the best decoupling and noise reduction solution. Surface mount components give the best results since they have less lead inductance and stray capacitance.

### Summary

The Spurious Free Dynamic Range of a D/A converter needs to be specified over the full Nyquist bandwidth as well as over the band of interest for a given application. Only this way can a system designer obtain a complete picture of the converter's spectral performance and determine it's impact to their system's performance. Selecting a low glitch, linear converter helps to significantly reduce spurs. Proper board layout and termination rules must be followed so as not to introduce undue system noise into the DAC. The HI5721 was designed to provide superior SFDR performance over the full Nyquist bandwidth and is one of the highest performance 10-bit DACs available today.



No. TB330 April 1995

# Harris Data Acquisition

# Higher Speed Clock Rates Help Ease Filtering Requirements in Communication D/As

Authors: Stephen G. LaJeunesse, Juan C. Garcia

### Introduction

As high speed D/A converters find their way into more digital communications systems it becomes apparent that adequate filtering solutions must be available. One way to ease the burden of filtering is to choose a D/A with as high a sampling frequency as possible. This helps to simplify any filtering choice by moving harmonics and clock aliases away from the frequency band of interest.

### Sampling and Aliases

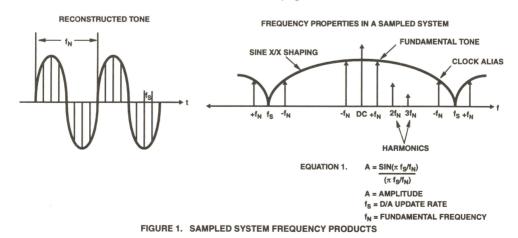
In a digital communications system, a high speed D/A converter is used to reconstruct the digital data into an analog signal. This signal can represent either an Intermediate Frequency (IF) or a baseband signal. When reconstructing the signal in a D/A converter, harmonics and sampling artifacts are produced, that generate unwanted spurs in a system, and must be removed by filtering. Harmonics are created by the nonidealities in the D/A such as linearity, and glitch. However, alias products are a consequence of using a sampled system. In a sampled system where a tone is generated at  $f_N$  using a clock at  $f_{\rm S}$ , harmonics will appear at every multiple of  $f_N$  while a clock alias term is generated at  $f_{\rm S}$ - $f_{\rm N}$ . The spurs in a sampled system are attenuated by a (SIN X)/X function that is an artifact of sampling. Figure 1 shows the results of a sampled system. The fundamental at  $f_N$  has

harmonics related to it. The harmonics replicate up through the frequency band and are attenuated by the linearity of the converter. The amplitude of a given harmonic increases along with the Integral linearity of the converter worsen. The clock alias always exists at  $f_{\rm S}\text{-}f_{\rm N}$ . The amplitude of the alias is attenuated by the (SIN X)/X function, a by-product of a sampled system. Clock alias products are almost as large as the fundamental frequency and, as a result, the largest unwanted spur in a system.

### Higher Sampling Frequencies Ease Filtering

The example in Figure 1 shows a typical frequency plan for a generic sampled system. The HI5721 has a maximum clock sampling rate of 125MHz. This clock frequency represents a 25% increase over the closest competitive device. In a system where the fundamental frequency is 40MHz, using a 125MHz  $f_{\rm S}$  generates harmonics that reside at 80MHz (2nd) and 120MHz (3rd). The clock alias will reside at  $f_{\rm S}\text{-}f_{\rm N}$  (125MHz -40MHz) or 85MHz.

If the system actually had a sampling frequency at 100MHz, then for the same fundamental frequency (40MHz) the clock alias would reside at 60MHz. The alias amplitude would be only -30dBc below the fundamental due to the (SIN X)/X shaping.



The filter required for the 100MHz clocked converter would have to reduce the clock alias by -30dB to maintain a 10-bit dynamic range of -60dBc. With the alias at 60MHz and the fundamental at 40MHz, the low pass filter used would need to rolloff at -15dB/decade. With a system clocked at 125MHz the clock alias appears at 85MHz. Assuming that harmonics are well below the -60dBc needed for a 10 bit system, then to reduce the clock alias at 85MHz by -30dB, the rolloff of a low pass filter could be relaxed to -7dB/decade. Therefore the higher conversion rate of the HI5721 enables designers to use simpler and less expensive low pass filtering solutions.

# Higher Sample Rate can Eliminate Up Convert Stages

In a digital communications system the baseband and IF processing can be done digitally with standard off the shelf DSP products. Modulators, Baseband Encoders and the like

have become readily available from a variety of manufacturers, bringing the ideal world of digital closer to the RF power amplifier. To convert an IF signal with baseband and modulation information to the transmission frequency a mix up convert stage is needed. Higher speed converters can eliminate multiple up-convert stages by taking advantage of their higher clock sampling rates and the processing of data digitally.

### Summary

As converter technology continues to progress, designers will benefit from ever increasing sampling rates. The HI5721, with its 125MHz maximum conversion rate helps simplify filtering requirements in high speed designs. Higher conversion rates also help to eliminate multiple IF stages and move the baseband processing closer to the transfer medium of a communication system.

# MAPPA OTE

No. AN9501.1 June 1995

# Harris Data Acquisition

## Understanding the HI5721 D/A Converter Spectral Specifications

Author: Juan C. Garcia

### Introduction

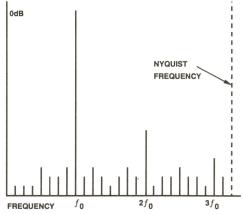
Data converters have, and continue to be one of the basic building blocks in data acquisition systems. However, with the growing dependance on D/A converter spectral purity in today's applications, it is becoming increasingly important for system level designers and IC manufacturers alike to understand the effect of spectral non-uniformity in these complex applications. The performance of a given D/A converter under a specific set of conditions provides the system designer with the data he or she needs to determine whether the converter will meet the requirements of the system.

### Discussion

Although there are a variety of definitions for Spurious Free Dynamic Range (SFDR), one which is commonly accepted is that SFDR is the difference in power between the fundamental and the highest spur over the full Nyquist bandwidth. SFDR is specified in dBc (decibels below carrier). Some variations of this specification include: a) the definition of a frequency window of interest around the fundamental and b) the exclusion of harmonics in the calculation of SFDR. Though sound arguments can be made to justify any of these definitions for SFDR, particular attention must be paid to what is actually being defined in each case.

Depending on the glitch impulse characteristics of the D/A converter, noise within a band limited range of frequencies (or window) can be dominated by its effects. Glitch impulse, which is a measure of the glitch area created by switching transients during converter updates, will generate high frequency spurs that fold back in band and cannot be filtered. This noise, which resides close to the fundamental, can define "windowed" SFDR.

Therefore, while the definition of a window around the fundamental provides useful information regarding the nature of the noise floor, it provides too limited a scope. Unless the user filters the output signal in a similar fashion to that being used to test the converter, the effect of the remainder of the noise floor on the application is unknown. The same can be said of defining SFDR using harmonics. Since harmonic distortion typically exceeds noise in the D/A converter's spectrum (as seen in Figure 1), little information about the characteristics of the noise floor are obtained. Figure 2 graphically illustrates this point. As one can see, dramatically different SFDR specifications can arise depending on the

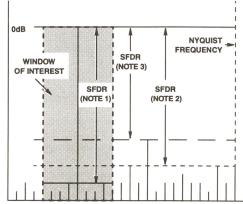


 $f_0$  = FUNDAMENTAL FREQUENCY

 $2f_0$  = SECOND HARMONIC

 $3f_0$  = THIRD HARMONIC

FIGURE 1. TYPICAL D/A CONVERTER SPECTRUM



### NOTES:

- 1. SFDR as Defined In 'Window'
- 2. SFDR to Nyquist Without Harmonics
- 3. SFDR to Nyquist Including Harmonics

FIGURE 2. DEFINING SFDR

method used for its definition. Specific system requirements will dictate which of the outlined methods will best suit your needs. However, by using method 2 (as shown in Figure 2) and determining the peak non-harmonically related noise generated by the converter in combination with total harmonic distortion (which defines noise generated by harmonics only), a better determination of the D/A converter's overall spectral purity can be obtained.

Total Harmonic Distortion (THD) is defined as the difference in power between the fundamental and the RMS contribution of all harmonics in band (to Nyquist), and is specified in dBc. While harmonics in general are dominated by any repetitive sources of error in a given converter, the shape of the transfer curve, or more specifically, the combination of integral non-linearity (INL), which is specified as the worst case deviation from the straight line approximation of a given converter's transfer function, and differential non-linearity (DNL), which is the worst case deviation from an ideal step size between adjacent codes along the transfer curve, will dominate the harmonic content of the spectrum.

Analysis of the Fourier series expansion of a given function reveals that:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) + \sum_{n=1}^{\infty} b_n \sin(n\omega_0 t)$$

where

$$a_n = \frac{2}{T} \int_{T} f(t) \cos(n\omega_0 t)$$

$$b_n = \frac{2}{T} \int_T f(t) \sin(n\omega_0 t)$$

and  $\frac{a_0}{2}$  is the DC value of the waveform  $f(t)^{[1]}$ .

When a function is even (or f(t) = f(-t)),

$$b_n \equiv 0$$
  $a_n = \frac{4}{T} \int_0^T f(t) \cos(n\omega_0 t) dt$ 

only even harmonics are generated.

Similarly, when a function is odd (or f(t) = -f(-t)),

$$a_n = 0$$
  $b_n = \frac{4}{T} \int_0^T f(t) \sin(n\omega_0 t) dt$ 

and only odd harmonics are generated.

In order to apply these equations, we must first establish the evenness or oddness of a given function. If we analyze the typical converter transfer functions shown in Figure 3, and prove the periodicity of these functions by superimposing them on to a sine wave, we now become free to apply the visual test for evenness or oddness<sup>[2]</sup>. Figure 4 graphically illustrates this procedure. The results of this test determine that the characteristic 'bow' function is even, while the 'S' function is odd.

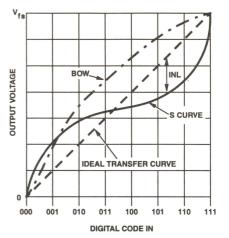
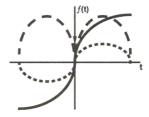


FIGURE 3. TYPICAL D/A CONVERTER TRANSFER FUNCTIONS



- 1/2 PERIOD OF SINE WAVE
- RESULTANT ERROR FUNCTION WHEN BOW IS SUPERIMPOSED ON SINE WAVE
- RESULTANT ERROR FUNCTION WHEN 'S' IS SUPERIMPOSED ON SINE WAVE

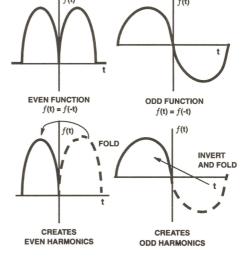


FIGURE 4. VISUAL TEST FOR EVENNESS OR ODDNESS

Applying this knowledge, we can determine that a 'bow' characteristic will generate dominant second harmonic, and an 'S' characteristic will generate a dominant third.

While this analysis assumes that functions are perfectly even or perfectly odd (which rarely occurs), it does provide an intuitive feel for the nature of harmonic distortion in data converters.

Signal to Noise + Distortion (SINAD) is the ratio of the power of the fundamental to RMS noise including harmonics (depending on the manufacturer, this specification may also be called Signal to Noise Ratio), and is specified in dB. Since this specification encompasses all noise in band (both harmonically and non-harmonically related over the full Nyquist bandwidth), it defines the overall effective resolution of the converter being tested. Once SINAD has been computed, the effective number of bits (ENOB) of a given converter is defined by the following equation:

$$\mathsf{ENOB} = \frac{(\mathsf{SINAD} - 1.76)}{6.02}$$

Signal to Noise Ratio (or SNR) is defined as the ratio of the power of the fundamental to RMS noise (the RMS value of the entire noise floor, minus harmonics, over the full Nyquist bandwidth), and is specified in dB. While this specification does not include any harmonic contributions, it does provide insight to the overall characteristic of its noise floor. Therefore, the combination of this specification with THD provides the user with more information about the nature of both harmonically and non-harmonically generated distortion than SINAD alone can provide.

### Conclusion

Since these specifications define the level of resolution for a given converter, it is important to understand the test conditions used when defining these parameters, and their applicability to the system being designed. Also, since not all manufacturers guarantee a minimum level of dynamic accuracy on their converters (usually given as typical values, if at all), it has been shown that careful analysis of the DC specifications can yield relevant spectral information. The nature of the converter's transfer function (which outlines the linearity performance of the converter) as well as specifications such as settling time and glitch impulse can assist the designer in anticipating the nature of both harmonic and noise floor degradation, which will limit the overall resolution of the converter.

### References

- [1] R.J. Mayhan, "Discrete-Time and Continuous Time Linear Systems", 1984, pp. 398-402.
- [2] R.W. Ramirez, "The FFT Fundamentals and Concepts", 1985, pp. 41-46.

# M APPOTE

No. AN9509.1 April 1995

# Harris DSP and Data Acquisition

# Digital IF Sub Sampling Using the HI5702, HSP45116 and HSP43220

Author: Carl Andren and John Fakatselis

### Introduction

This note is about the conversion of previously analog receiver designs into a digital form. It includes a technique for IF sub sampling that can simplify the digital circuits compared to a one to one correspondence with analog methods. An example of a Digital Receiver design based on off-the shelf Harris Components, is included.

### Discussion

It is often desired to downconvert a bandpass signal to its baseband representation. Bandpass signals can be expressed as a sum of two quadrature components which are 90 degrees out of phase. In general:

$$x(t) = x1(t) \cos \omega_c t + x2(t) \sin \omega_c t$$

where x1(t) is the in phase component, x2(t) is the quadrature component of the signal x(t) and  $\omega_c$  is the center frequency of the band pass signal (carrier frequency).

In the down conversion process the receiver needs to effectively shift the carrier frequency  $\omega_c$  to baseband (DC). To achieve this one must multiply the incoming bandpass signal x(t) with the complex phasor [ $cos\omega_c\,t$ -  $jsin\omega_c\,t$ ] and then low pass filter the result. This operation will accomplish the desired frequency shift.

$$x(t) [\cos\omega_c t - j\sin\omega_c t] = 1/2[x1(t) + x1(t) \cos2\omega_c t - jx1(t) \sin2\omega_c t + x2(t) \sin2\omega_c t - jx2(t) + jx2(t)\cos2\omega_c t]$$

After low pass filtering the second harmonic components are filtered out and the result is the desired baseband signal representation of x(t):

LPF (output) = 
$$1/2[x1(t) - j x2(t)]$$

Figure 1 illustrates the functional block diagrams that represent this mathematical process.

$$x(t) = x1(t) \cos \omega_{c} t + x2(t) \sin \omega_{c} t$$

$$x(t) = x1(t) \cos \omega_{c} t + x2(t) \sin \omega_{c} t$$

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FIGURE 1. BASEBAND DOWNCONVERSION BLOCK DIAGRAM

An all digital implementation of this function implies that the an A/D converter needs to digitize the incoming waveform x(t).

The carrier frequency  $\omega_c$  is typically much higher than the frequency of the actual baseband signal. The Nyquist criterion specifies the minimum sampling rate of the A/D required for signal reconstruction. This minimum sampling rate is defined as twice the frequency of the baseband signal. Based on this definition alone it appears that the carrier frequency  $\omega_c$  does not influence the sampling rate of the A/D converter. For example, if a baseband signal of 9600 bits/sec is transmitted using a  $\omega_c$  of 45MHz at the A/D input, then the sampling rate to reconstruct the 9600 bits/sec signal needs to be a minimum of 9600 x 2 = 19.2kHz. The 19.2kHz rate is the signal reconstruction requirement for the sampling rate independent of the value of  $\omega_c$  Based on this discussion, a low speed A/D can potentially be used to sample the signal at very high IF frequencies and still recover the baseband information. This concept is referred as under sampling or sub sampling. Sub sampling makes an all digital implementation of down conversion at high IF frequencies (i.e. 40MHz-200MHz) feasible. This is because A/Ds would no longer present a limiting factor. A/Ds at low sampling rates are relatively inexpensive and available. From a pure, Nyquist rate, theoretical standpoint this appears as a viable approach. In practice though there are a number of additional factors that need to be evaluated for such a design. The A/D requirements are still a key factor and they impact the design outcome and overall feasibility to a great extent. The designer must carefully analyze the following requirements before deciding on an A/D for a particular under sampling application.

A/D dynamic range requirement: This is derived by examining the operational environment and desired system signal to noise ratio. The noise environment, signal interference conditions, multipath, and adjacent channel rejection requirements are some of the primary variables that influence the dynamic range specifications of the A/D in a classical receiver architecture. In addition, the existence of a system AGC and the parameters of the filters that proceed the A/D need to be taken into account for these calculations.

A/D sampling rate requirement: This is derived primarily from the baseband signal bandwidth. The minimum rate is defined by the Nyquist criterion. The overall system frequency plan and the baseband digital rates required by the system can also influence the decision on the rate selection. Implementation issues such as availability of only certain clock rates can also play a role in selecting the sampling rate. A minimum rate may be set by the A/D Track and Hold droop specification.

A/D Track and Hold aperture jitter requirement: This requirement is a function of the IF frequency. The track and hold circuit must have enough bandwidth to adequately cover the IF frequency that is being sampled. In addition, the effects on the system performance due to the sampling aperture error have to be evaluated. The aperture jitter of the track and hold directly influences this aperture error result. The degradation due to aperture jitter is a function of the sampled IF frequency. The higher the IF frequency the tighter the track and hold aperture jitter requirements become in order to maintain a desired aperture error system specification.

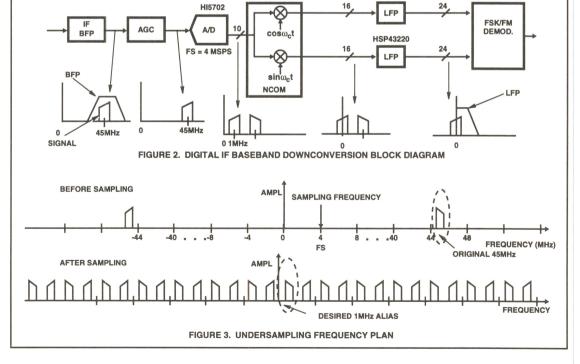
An example of a digital receiver application will be used to further elaborate on under sampling and to demonstrate the points made thus far.

This design is based on the Harris HI5702 A/D for the IF sampling, the Harris HSP45116 numerically controlled oscillator /modulator (NCOM) to perform the multiplication of the A/D samples with the complex phasor  $[\cos\omega_c\,t\,-\,j\sin\omega_c\,t],$  followed by the Harris decimating digital filters HSP43220 that generate the low rate filtered baseband data. The down conversion and filtering operations are followed with a digital FSK/FM demodulator that processes the baseband in phase (I) and quadrature (Q) data as it is being output from the digital low pass filters (HSP43220). The digital demodulator can be a simple discriminator implementation based on delay and multiply calculations on the I and Q channels. Figure 2 illustrates this general purpose digital IF design. The block diagram includes an optional AGC circuit. The utility of this AGC circuit is explained later in this paper.

The target receiver design is a standard FSK/FM receiver with a 45MHz IF and 25kHz of channel bandwidth. It is also assumed that the FSK data has a deviation of (±6.4kHz. This example can be modified for ETACS. AMPS. Nordic Telephone. MMP and other applications. Existing systems that use traditional analog techniques place the A/D after the analog discriminator which performs the FSK/FM demodulation. These systems experience problems with matching the pre detection filtering to the discriminator. Assuming the S curve characteristics of the analog discriminator, it is apparent that frequency matching of the analog filters becomes essential to maintain acceptable performance. The digital implementation doesn't suffer from possible filter mismatching and digital filters are not subject to phase non linearities. In addition, the digital approach can improve the performance of the adjacent signal rejection over the rejection that is provided by the analog IF filter, in front of the A/D converter.

The diagram on Figure 2 shows this basic approach which uses sub sampling to convert the 45MHz IF to a 1MHz IF. This assumes that the track and hold is integrated with the A/D as is the case with the HI5702. The frequency spectrum diagrams in Figure 2 show the basic signal processing flow in sub sampling. The input signal is first filtered using an analog IF bandpass filter and then amplified by an ACG amplifier to a level sufficient to drive the A/D converter. It is then sampled by the high speed track and hold and quantized by a 4MHz rate clock at the A/D converter. The sampling process creates a spectrum that repeats the original spectrum every multiple of the sampling frequency as shown in Figure 3. The negative part of the spectrum is shown folded back on and interleaved with the positive part.

HSP43220



HSP45116

where:

Two of the repeats (aliases) can be found at frequencies between the sampling frequency and DC. The sub sampling approach can be thought of as generating a signal replica at a much lower IF frequency close to DC. In this example the aliased signal is centered at 1MHz. This signal is later going to be processed by the NCOM, as shown in Figure 2, to shift it and center it at DC where it can be digitally filtered. The sampling rate as well as the bit resolution of the A/D are chosen based on the following considerations:

- 1. The highest usable sampling rate is set by the A/D converter and the subsequent digital processing circuits. For low power operation and ease of processing, the lower the rate, the better. Fundamentally, the lowest rate is twice the signal bandwidth according to the Nyquist criterion. For this example, that works out to 50kHz given that the signal occupies a 25kHz channel. Practically, however, the filtering in the RF and IF circuits is usually not sufficient to insure good performance this close in. The sampling frequency has to be high enough so that any noise and interference passing through the RF and IF filtering does not fold back within the sampling bandwidth. These filters only partially reject interference for a bandwidth that is wider than the channel bandwidth. Additionally, the minimum sampling rate is set by the lowest rate that the A/D converter can use without suffering too much track & hold droop. For the Harris HI5702, the lowest rate is 0.5MHz. For these reasons, the sampling rate was chosen to be 4MHz. This sampling rate aliases the 45MHz IF to create the 1MHz IF. This rate is also easily handled by the Harris Digital Signal Processing devices (HSP45116, HSP43220) which follow with complex down conversion, decimating and filtering, Higher sampling rates can also be employed if more over sampling of the baseband signal is desired.
- 2. The digital filters that follow in the processing chain can provide additional adjacent channel rejection to improve selectivity beyond what the analog IF filter is offering. This additional selectivity can be 30-40dB more than provided by the IF filter prior to the A/D. In this example the combination of the analog IF filter and the digital filter selectivities can provide overall adjacent channel rejections of 60dB to 70dB.

One consideration to be addressed is the placement of gain and the use of AGC. In most analog designs, the majority of the gain is in the final IF after the filtering that establishes the selectivity. Since we are using digital processing to do some of this filtering, large interfering signals might exist at the input to the A/D converter. We cannot allow clipping in the IF prior to the A/D converter because of these adjacent channel signals. For this reason, the A/D will have to be operated with adequate headroom in order to insure that the adjacent channel signals are not above full scale. Another reason to use headroom is Raleigh fading due to multipath. This phenomenon causes rapid variations in the signal level for a number of applications such as a mobile cellular terminal. The receiver of this fading signal needs to handle variations that can potentially range from +10dB to -40dB.

Excluding the requirements for multipath and interference. for +10dB of pre detection SNR alone, the required number of A/D bits is 2 (assuming ~ 6dB/bit). The system,

though, needs to achieve 40dB more adjacent channel rejection which implies that the SNR at the A/D will be at -30dB or so given the +10dB of pre detection SNR that is needed. This, along with 6dB of headroom, sets the required A/D quantization to a minimum of 6 bits or about 36dB of ENOB (equivalent number of bits). To insure good ENOB performance, an 8-bit A/D should be sufficient. Note that the driving specification for the A/D is the spurious free dynamic range that the system requires.

3. In choosing the sub sampling rate one should also be concerned with the phase noise due to the clock edge jitter of the sampling clock. This combined with the inherent aperture jitter in the A/D can limit of how low the sampling rate can be set.

An approximation to the aperture error of the A/D converter can be derived from the formula:

> n = number of bits ta = aperture error

Fmax = IF frequency

For the given IF frequency and sampling rate the aperture error of the A/D converter needs to be less than 27ps for a 1 LSB degradation at 8 bits. The hold time is 250ns for the 4MHz sampling rate. All of these requirements are met or exceeded with the HI 5702 A/D converter.

- 4. The quantization noise is another noise source that needs attention. For this example, given the choice of the sampling frequency, the quantization noise will be spread over the 4MHz bandwidth and will therefore be attenuated when the signal is filtered to 25kHz bandwidth during the pre detection filtering. This reduction in bandwidth gives 22dB of SNR improvement. With a required SNR of 35dB in 3kHz of bandwidth after the final filtering at the FM demodulator, the quantization noise is not of concern. The digital filtering process needs to also be evaluated since this process is essential to achieve the additional filter selectivity for the overall system. By using the HSP43220 the additional filter selectivity desired for this application can be achieved. The HSP43220 is a decimating digital filter. Decimation is the filtering operation employed in digital filtering that accomplishes the rate reduction from filter input to filter output. A summary of the HSP43220 features include:
  - . DC to 33 MHz clock rate
  - 16-bit 2's complement input
  - · 20-bit coefficients
  - · 24-bit extended precision output
  - Programmable Decimation up to a maximum of 16,384

Decimation factors, sampling rates and number of filter taps need to be traded in configuring the filter response. For the application of this example the HSP43220 can be programmed to provide the desired filter response. An example of two possible filter specifications are attached. The filter coefficients for these two cases were generated using Deci-Mate which is a software filter design tool developed for the HSP43220. The user defines the desired filter response and the program determines if the HSP43220 can implement the given response and then it derives the necessary coefficients, and hardware configuration.

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The filter parameters as well as the frequency response for these two filter examples are as follows:

Filter 1.

Passband = 7500

Transition Band = 3000

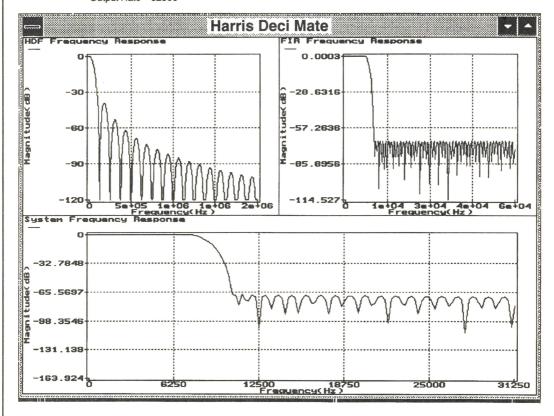
Passband Attenuation = 0.5dB

Stopband Attenuation = 60dB

Input Sample Rate = 4e+06

FIR Input Rate = 125000

Output Rate = 62500

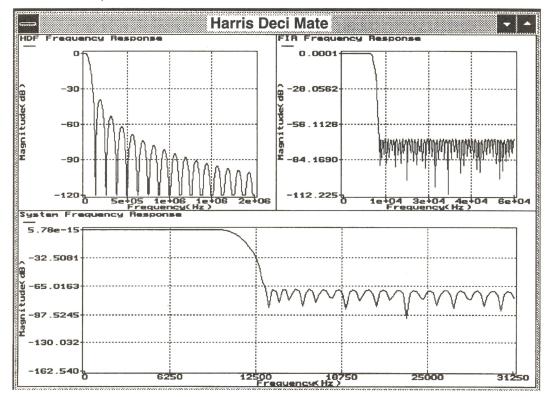


Stopband Attenuation = 60dB

Input Sample Rate = 4e+06

FIR Input Rate = 125000

Output Rate = 62500



The HSP43220 architecture is composed of the cascade of two filtering stages. The High order Decimation Filter (HDF), followed by a Finite Impulse Response (FIR) filter. The individual responses of both filters are shown on the two top frequency spectrum responses. The HDF has a sinx/x type of a response and it does the initial filtering followed by the FIR that provides the desired stopband and transition band output characteristics. The cascaded final system response which is the actual output of the HSP43220 is shown on the bottom frequency response plot.

Besides the HSP43220 Harris has a number of other high speed Digital Filters that can be appropriate for under sampling applications. The reference part numbers for some of these filter products include the HSP43168, the HSP43124, the HSP43216 and the HSP50016. Information and more details of these Digital Filters as well as for other Digital Signal Processing (DSP) products can be found in the Harris DSP data book.



### No. AN9619 May 1996

# Harris Data Acquisition

### Optimizing Setup Conditions for High Accuracy Measurements of the HI5741

Author: Juan C. Garcia

### Introduction

The HI5741 is a 14-bit 100MHz Digital to Analog Converter. This current out DAC is designed for low glitch and high Spurious Free Dynamic Range operation. As a result of its inherently high dynamic range, special care must be taken to assure that any accuracy measurements made on the device are not corrupted by external stimuli introduced by the measurement equipment being used. The purpose of this application note is to outline proven measurement techniques (both static and dynamic) to assure accurate Digital to analog converter performance is observed.

### Measuring Spurious Free Dynamic Range (SFDR)

The Spurious Free Dynamic Range of the HI5741 DAC is the most important specification for communication applications. This specification shows how Integral Linearity, Glitch, and Switching Noise affect the spectral purity of the output signal. Several important things must be noted first.

When a quantized signal is reconstructed, certain artifacts are created. Let's take the example of trying to recreate a 2.03MHz sine wave with a  $1V_{P,P}$  output. In the frequency domain the fundamental should appear at 2.03MHz as shown in Figure 1.

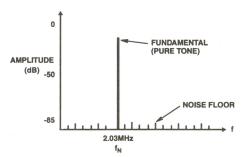


FIGURE 1. SIGNAL CHARACTERISTICS

The fundamental of a pure 2.03MHz tone should appear as an impulse in the frequency domain at 2.03MHz. In a sampled system noise terms are produced near the sampling frequencies called aliases. These aliases are related to the fundamental in that they are located at  $\pm f_N$  around the sampling frequency as shown in Figure 2.

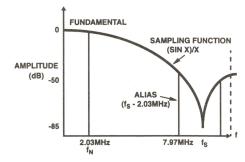


FIGURE 2. ALIASING CHARACTERISTICS OF SAMPLED SYSTEMS

So for a 2.03MHz fundamental and a 10MHz sampling rate an alias term is created at 7.97MHz and 12.03MHz. A (SIN (X))/X function shaping is also induced by sampling a signal. Aliases continue up through the frequency spectrum repeating around the sampling frequency and its harmonics (i.e.,  $2f_S$ ,  $3f_S$ ,  $4f_S$ ).

Since the highest spur (either harmonically or non-harmonically related) with respect to the fundamental will define the dynamic range of the system, it is used to define the Spurious Free Dynamic Range of the converter.

### **Checking Your Setup**

Measuring the spectral performance of high speed DACs with high degrees of dynamic range presents an interesting problem during the course of device or system evaluation. In the case of the HI5741 in particular, the device in many cases exhibits levels of dynamic range that either equal or exceed those of the measurement device used.

The problem arises in that the noise floor performance observed when using a spectrum analyzer to measure the DAC varies depending on the settings for resolution bandwidth (RBW) and mixer attenuation which are used. By adjusting these two settings, one can artificially make the spectral performance of the DAC look worse than it really is. This phenomena can be attributed to a variety of factors, the most dominant of which is the sensitivity of the analyzer itself. As a general rule, adjusting the mixer (or internal) attenuation on a spectrum analyzer should not result in any change in measured harmonic performance. A change in the harmonic

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power of the signal is a good indicator of a possible saturation condition on the mixer, which needs to be corrected prior to making final measurements. Increasing the mixer attenuation does have some drawbacks, however, namely an increase in noise floor power, which needs to be compensated for by decreasing the resolution bandwidth. This issue can be seen by observing the spectral sweeps shown in Figures 3 and 4. In both cases, a 2.03MHz fundamental was created at a clock rate of 10MHz. In addition, 16dB of external attenuation was used in all cases.

Figure 3 illustrates the output of the spectrum analyzer (in this case an HP8560E) as seen with no mixer attenuation using a resolution bandwidth of 100Hz. The first thing that one notices by observing this figure is that the second harmonic distortion is much higher than one would expect for a 14-bit converter (59.5dB below the fundamental).

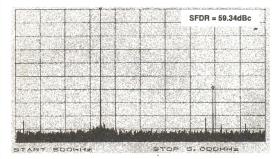


FIGURE 3. SPECTRAL PERFORMANCE WITH NO INTERNAL ATTENUATION

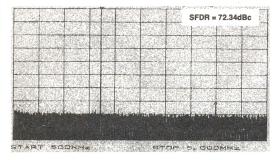


FIGURE 4. SPECTRAL PERFORMANCE WITH 20dB INTERNAL ATTENUATION

In Figure 4, one can see the vast improvement in spectral purity obtained by simply adding 20dB of internal attenuation to the mixer. Note dynamic range over the entire band of interest. Also of note is the increased noise floor characteristic of the spectrum (approximately 15dB average increase) over then entire band. As stated earlier, this is expected when introducing internal attenuation.

The use of external attenuation can also play a significant role in dynamic range measurements. As a rule of thumb, adjusting the external attenuation of the signal (not to be

confused with the mixer or internal attenuation) should result in a dB-for-dB drop in both carrier and harmonic power. If an increase in external attenuation results in an increase in measured dynamic range, the previous measurement was once again limited by the analyzer.

All this being said, the fundamental problem still exists in that one must still make dynamic range measurements in excess of 80dBc over a relatively large frequency span, a condition which most modern spectrum analyzers cannot readily accommodate. As a result, the use of signal filtering needs to play an important role in the course of evaluating performance.

The use of filtering can dramatically ease the problems described above with respect to measuring dynamic range. By using a good quality notch filter, one can eliminate the need to adjust mixer attenuation and in turn bring to bear the full dynamic range of the spectrum analyzer. Figure 5 illustrates the characteristics of such a notch filter.

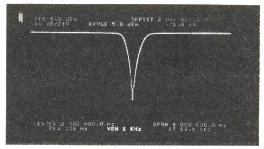


FIGURE 5. NOTCH FILTER CHARACTERISTICS

The three fundamental characteristics which make the use of a notch filter desirable for this type of testing are:

- a) Attenuation of the Fundamental. By attenuating the fundamental, which is the spur with by far the most power in the spectrum, one dramatically decreases the burden on the spectrum analyzer to accurately measure the performance of the device under test.
- b) **Quick Recovery.** By making the attenuation band as narrow as possible, the filter again allows the evaluator to get an accurate depiction of the device's performance without having to worry about attenuation of any harmonic distortion generated by the converter.
- c) Low Insertion Loss. While insertion loss in and of itself can be dealt with when making measurements, lower insertion loss makes the job of characterizing the HI5741 less cumbersome.

As one can see from Figure 5, the filter used to make the described measurements possesses a >60dB notch with a 100kHz attenuation band and negligible insertion loss.

As stated earlier, the introduction of a notch filter to the system allows the evaluator to bring the full dynamic range of the spectrum analyzer to bear when making measurements. As seen in Figure 6, this can result in a significant improvement in the measured dynamic range of the HI5741.

While these high quality filters can be quite expensive and cumbersome to use at times, the goal of filter use is to ascertain the actual device or system level performance, not enhance it.

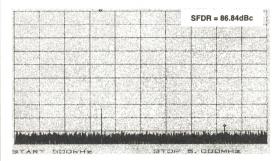


FIGURE 6. SPECTRAL PERFORMANCE OF THE HI5741

#### Linearity

Linearity measurements on Digital-to-Analog converters are typically performed in a static state. An input code is generated and presented to the digital inputs of the converter. The converter is then strobed (or clocked) to pass the data through the converter. After a predetermined amount of wait time has passed (to assure the output of the DAC has settled), the output of the converter is then measured several times (to eliminate the presence of noise) and an average output voltage is recorded. Once all of the data has been collected, an LSB (or Least Significant Bit) size is computed based on the following equation:

$$LSB = \frac{(FSR)}{2^{n} - 1}$$
 (EQ. 1)

Where FSR is defined as the full scale range of the converter and n is the resolution (number of bits).

Once the LSB size has been computed for the converter being tested, the linearity performance (both Integral and Differential) can be computed by the following equations:

$$INL = \frac{(V_{CODE} - ((LSB \cdot CODE) + OFFSET))}{LSB}$$
 (EQ. 2)

$$DNL = \left(\frac{(V_{CODE} - V_{CODE} - 1)}{LSB}\right) - 1$$
 (EQ. 3)

Where  $V_{CODE}$  is the voltage measured on the load resistor at a given code,  $V_{CODE-1}$  is the voltage measured on the load resistor at the previous code and OFFSET is the offset voltage of the converter (or voltage output at CODE = 0).

While the same fundamental concepts of measuring linearity apply to high resolution converters as for lower (10 bits and below) resolution DACs, special care must be taken to avoid thermal effects from degrading performance. Unlike dynamic testing, where the voltage created on a load resistor is changing very rapidly, the nature of linearity testing allows the thermal characteristics of these resistors to come into play.

Typical temperature coefficient ratings for such resistors are quoted to be in the 100ppm to 200ppm per degree Celsius range. In the case of the HI5741, which has an LSB size of approximately 60µV, this TC performance can result in as much of 3 LSB of error in linearity. To avoid this, the use of low temperature coefficient resistors (40ppm/°C maximum) will effectively remove the effects of thermal drift from linearity measurements of the HI5741. Refer to Figures 7 and 8 below for the typical linearity performance of the HI5741 using the methods outlined above.

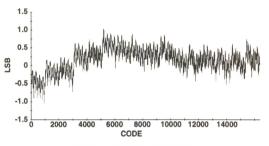


FIGURE 7. TYPICAL HI5741 INL

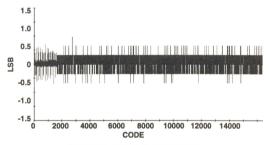


FIGURE 8. TYPICAL HI5741 DNL

#### **Board Layout Considerations**

A task that can be just as challenging, if not more frustrating as making sure the measurement equipment being used reports both repeatable and realistic numbers, is the that of making sure that the evaluation platform (specifically the PCB) does not introduce unwanted noise.

Series Termination Resistors - As with any mixed signal design, it is important to keep noise generated from high speed digital signals from corrupting high accuracy analog data. To assist with this effort, the use of series termination resistors, which interact with the input capacitance of the device, provide an adequate low pass filter. The choice of resistor value depends on the requirements set by the system being designed. The only restriction when choosing a resistor value is that of voltage drop across the resistor, which will be driven by the input current of the device. The worst case specification for input current on the HI5741 is  $700\mu\text{A}$ , which needs to be taken into consideration to make sure enough amplitude remains to trigger the device.

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The frequency response of the low pass filter can be determined by the following equation:

$$f_{\text{CUTOFF}} = \frac{1}{2\pi RC}$$
 (EQ. 4)

Where R is the series resistor being solved for, and C is the input capacitance of the HI5741. Since the input capacitance of the device will vary depending on lot to lot variation through manufacturing, one should use the worst case capacitance value of 5pF (as opposed to the typical 3pF stated in datasheets) in determining the appropriate cutoff frequency.

In addition to series termination resistors, trace lengths on the digital inputs should be kept as short and closely matched as possible. At high frequencies, large mismatches in trace lengths on the data lines can generate excessive noise and in extreme cases can result in a setup time violation on the DAC.

Output Loading - Care should be taken to assure that the loads on the two analog outputs of the DAC (I<sub>OUT</sub> and I<sub>OUTB</sub>) are as closely matched as possible. Trace lengths should be closely matched and high precision resistors should be used to assure any impedance mismatch is minimized as seen inside the device.

**Power Planes** - Careful consideration must be taken when laying out the power planes of high speed devices as well. In the case of the HI5741, this consists of three power planes (V<sub>CC</sub>, V<sub>FF</sub> and GND).

Since the only device connection to  $V_{CC}$  is strictly digital in nature, the  $V_{CC}$  plane can be one solid sheet as long as it is appropriately decoupled to the digital ground plane.

In the case of  $V_{EE}$ , particular care should be taken since this is the substrate potential of the HI5741. In order to avoid a loop which will create additional noise at the device, the  $V_{EE}$  supply should be brought in at one central location, and distributed to the  $V_{EE}$  plane through a ferrite bead connection (to reject high frequency noise) to the device as seen in Figure 9 below.

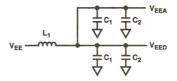


FIGURE 9. RECOMMENDED SUPPLY CONNECTION

In addition, supply decoupling should be placed as close to each pin as possible.

Separate ground planes should be provided and tied together at one central, low impedance ( $<10\Omega$ ) location.

#### Conclusion

As had been outlined in this document, the task of making realistic accuracy measurements on a 14-bit Digital to Analog converter such as the HI5741 can be a demanding task. By using the procedures described, the evaluator will be able to obtain a true picture of the actual performance of the device or system being evaluated. Using filtering, low drift resistors and following the board layout guidelines presented, make it possible to achieve dynamic range measurements in excess of 80dB.

# M APPOTE

No. AN9629 July 1996

# Harris Data Acquisition

### **Multi-Tone Performance of the HI5741**

Author: Juan C. Garcia

### Introduction

The HI5741 is a 14-bit 100MHz Digital to Analog Converter. This current out DAC is designed for low glitch and high Spurious Free Dynamic Range operation. As a result of its inherently high dynamic range, the HI5741 allows base station designers to carry a higher degree of dynamic range through the converter. This in turn lowers system cost by reducing board space, power and filtering requirements.

### Definition

Originally defined as a figure of merit for applications such as ADSL (Asymmetric Digital Subscriber Line), where groups of tones are input to the device with defined "dead zones" (or separations between groups), an MTPR (or Multi-tone Power Ratio) specification provides system designers with an average level of dynamic range from peak power to peak distortion in the zones void of tones.

Though this definition for MTPR is useful and quite appropriate for ADSL applications, base station requirements are quite different and as a result, require an alternate interpretation of the original definition. As a result, the scope of the MTPR Specification was modified to encompass only one "dead zone", and in turn provide a true dynamic range specification to base station manufacturers.

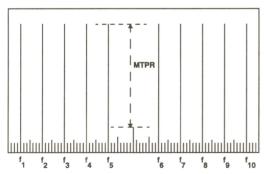


FIGURE 1. DEFINING MTPR

As seen in Figure 1, a series of equally spaced tones is input to the DAC with one tone removed in the center of the range. The worst case converter generated distortion, which is generally a third order harmonic product of the fundamental fre-

quencies (2f1-f2 or 2f2-f1), will appear as the worst case spur at the frequency of the missing tone in the sequence. The resultant dynamic range from peak power to peak distortion in the region of the removed tone is defined as MTPR.

### Advantages

Traditionally, Digital to Analog Converter (DAC) spectral specifications have centered around single tone outputs and the corresponding degrees of distortion generated by the DAC itself. Specifications such as Signal to Noise Ratio (SNR), Signal to Noise + Distortion (SINAD), Total Harmonic Distortion (THD) and Spurious Free Dynamic Range (SFDR), all provide system level designers valuable information with respect to the spectral properties of the DAC being evaluated, however the task of determining how the converter responded to multitone conditions was still left to the designer. The specification of DAC performance under multi-tone output conditions therefore provides system designers with a key piece of data necessary to determine the applicability of a given converter in their design.

From a system standpoint, the ability to maintain high degrees of dynamic range under multi-tone conditions simplifies the overall design. Traditionally, base-station designs utilized one converter per transmit channel which meant having multiple DACs per board. The ability of the HI5741 to maintain high degrees of dynamic range under a 10 tone condition therefore equates to reduced board space, design complexity and most importantly, cost.

### Measuring MTPR

MTPR testing of the HI5741 was performed using the evaluation circuits shown in Figures 2 and 3. In measuring the MTPR performance of the HI5741, a series of 10 tone patterns were created and input to the converter. To truly determine the performance of the converter across frequency, tone spacing was maintained at 200kHz for all frequencies tested, with clock frequencies ranging from 10MHz to 75MHz. These conditions were also repeated for clock to output frequency ratios ( $f_{\rm OUT} = f_{\rm CLK}/n$ ) of 10, 5 and 4. Once the desired frequencies were obtained and observed on the spectrum analyzer, the Multitone power ratio of the device was measured as the dynamic range from peak power to peak distortion in the gap between tones 5 and 6. Figures 4 through 6 graphically illustrate the level of performance that can be expected from the HI5741

under the conditions described above. Also included are spectral plots under the three clock to output frequency ratios described above at a clock rate of 22.4MHz.

As can be seen in Figures 4 through 6, the HI5741 exhibits high degrees of dynamic range (>70dBc) under all three clock to output frequency conditions at clock frequencies up to 30MHz. Once past a clock frequency of 30MHz, the full scale settling time of the device begins to dominate the performance of the HI5741, resulting in steadily declining levels of MTPR.

### Conclusion

**Application Note 9629** 

The inclusion of dynamic range specifications for Digital to Analog converters under multi-tone conditions can provide base station designers with key information with respect to the anticipated performance of a given converter in their system. For cellular applications, high degrees of dynamic range under multi-tone conditions can reduce system cost by allowing greater throughput (by passing more information through each converter) from each individual DAC, thus reducing board space, power consumption, filtering requirements, and overall system cost.

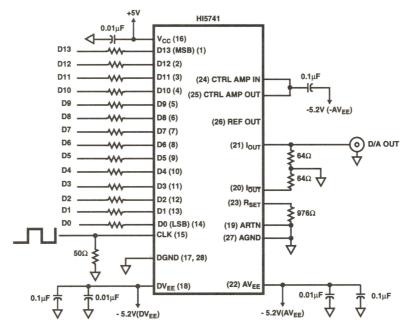


FIGURE 2. HI5741 MTPR EVALUATION CIRCUIT

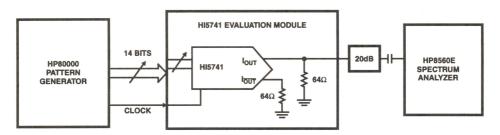
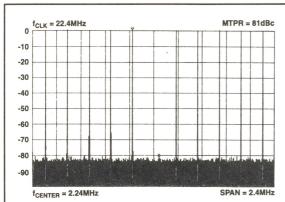


FIGURE 3. LAB SETUP FOR HI5741 EVALUATION

### **Application Note 9629**



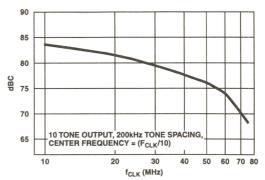
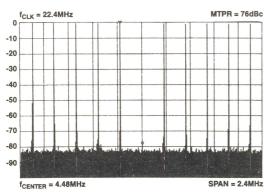


FIGURE 4A.

FIGURE 4B. HI5741 MTPR PERFORMANCE vs CLOCK FREQUENCY

FIGURE 4. HI5741 MTPR PERFORMANCE WITH  $f_{OUT} = (f_{CLK}/10)$ 



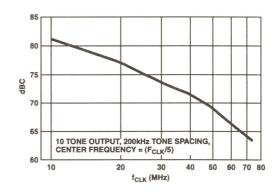
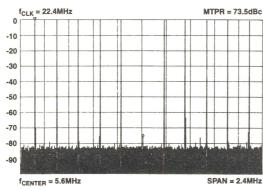


FIGURE 5A.

FIGURE 5B. HI5741 MTPR PERFORMANCE vs CLOCK FREQUENCY

FIGURE 5. HI5741 MTPR PERFORMANCE WITH f<sub>OUT</sub> = (f<sub>CLKT</sub>/5)



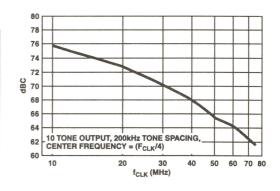


FIGURE 6A.

FIGURE 6B. HI5741 MTPR PERFORMANCE vs CLOCK FREQUENCY

FIGURE 6. HI5741 MTPR PERFORMANCE WITH f<sub>OUT</sub> = (f<sub>CLK</sub>/4)

### Introduction

The primary application of coherent sampling is sinewave testing of A/D converters. If the proper ratios between  $f_{\rm IN}$  and  $f_{\rm S}$  are observed, the need for windowing is eliminated. This greatly increases the spectral resolution of a FFT and creates an ideal environment for critically evaluating the spectral response of the A/D converter. Care must be taken, however, to insure the spectral purity and stability of  $f_{\rm IN}$  and  $f_{\rm S}$  in the testing environment. Figure 1 illustrates this procedure.

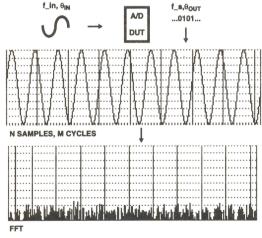


FIGURE 1. TESTING SYSTEM FOR SINEWAVE ANALYSIS

### **Definition of Coherence**

Coherent Sampling of a periodic waveform occurs when an integer number of cycles exist in the sample window. In other words, coherent sampling occurs when the relationship of Equation 1 is rational.

$$\frac{f_{1N}}{f_{S}} = \frac{M}{N}$$
 (EQ. 1)

### Where:

f<sub>S</sub> is the sampling frequency

f<sub>IN</sub> is the input frequency

M is the integer number of cycles in the data record

N is the integer, factor of 2, number of samples in the record

### Ideal Parameters for Coherence

The coherence relationship will work for any arbitrary M and N, but practical values provide better results. A prudent choice for N is a power of 2. The FFT requires the number of samples to be a power of 2 because of its inherent periodicity. The DFT can be performed on an arbitrary sample size, but requires more computation time. M should be odd or prime. By making M odd, we eliminate many common factors with N. A prime M eliminates all common factors with N. Common factors between M and N lead to different harmonics of f<sub>IN</sub> having the same frequency bin in the FFT after aliasing. The uniqueness of M is absolutely imperative to Harmonic Distortion calculations.

What follows is a mathematical analysis defining a simple rule that evaluates true when two harmonics have equivalent bins in the FFT. Equation 2 represents the location,  $M_h$ , in a FFT, of a harmonic h.

$$M_{h} = \begin{pmatrix} h - NxINT \left(\frac{h + \frac{N}{2}}{N}\right), h \neq \frac{N}{2} \\ 0, h = \frac{N}{2} \end{pmatrix}$$
 (EQ. 2)

Suppose harmonic 1 and harmonic 2 have the same FFT bin locations,  $M_{h1} = M_{h2} = M_h$ , then, from Equation 2,

$$\mathbf{M_{h}} = \left( \left( \left| \mathbf{h_{1}} - \mathbf{NxINT} \left( \frac{\mathbf{h_{1}} + \frac{\mathbf{N}}{2}}{\mathbf{N}} \right) \right| = \left| \mathbf{h_{2}} - \mathbf{NxINT} \left( \frac{\mathbf{h_{2}} + \frac{\mathbf{N}}{2}}{\mathbf{N}} \right) \right| \right) \mathbf{h_{1}} = \mathbf{h_{2}} \neq \frac{\mathbf{N}}{2}$$

$$0, \mathbf{h_{1}} = \mathbf{h_{2}} = \frac{\mathbf{N}}{2}$$
(EQ. 3)

Consider that h1, h2, and N will always be positive values. Simplifying Equation 3 results in Equation 4.

$$\frac{(h_1 \pm h_2)}{N} = INT \left( \frac{h_1 + \frac{N}{2}}{N} \right) \pm INT \left( \frac{h_2 + \frac{N}{2}}{N} \right)$$
 (EQ. 4)

Since the right side of Equation 4 must necessarily be an integer, the left side must also be an integer when the two harmonic locations  $M_{h1}$  and  $M_{h2}$  are equal.

$$M_{h1} = M_{h2} \Leftrightarrow \frac{(h_1 \pm h_2)}{N} = INT$$
 (EQ. 5)

Therefore, when Equation 5 is true, the frequency bin of harmonic 1 is equal to the frequency bin of harmonic 2. The FFT provides N/2 frequency bins. To insure the uniqueness of each harmonic of the fundamental frequency bin, Equation 5 must be false for all combinations of h1 and h2 for all multiples of M extending to N.

Sampling at the Nyquist rate of  $f_S = 2^* f_{IN}$  is a classic problem. As an example, consider N = 4096,  $f_{IN} = f_S/2$ , M = N/2. Equation 5 evaluates as  $((h_1 \pm h_2)/4096) = INT$ . If we substitute h =  $x^*M$  for h1 and h2 where x represents the harmonic number, the equation simplifies to  $((x_1 \pm x_2)/2) = INT$ . Whenever this equation holds true, the two harmonics have the same frequency bin. In this case, every odd harmonic will have the same bin as the fundamental and every even harmonic will have the same bin as DC. Therefore, no information about harmonic distortion or signal to noise ratio can be calculated.

### Non-Ideal Parameters for Coherence

Thus far, we have talked about the complexities involved in coherent sampling that usually involve tedious iterative calculations to get the correct sampling ratio. That process ultimately resolves a very accurate solution. When the integer relationship of Equation 1 is not observed, artifacts result in the FFT spectrum.

Figure 2 is a 4096 point sample record from an ideal 10-bit A/D converter. To illustrate how the FFT interprets the 4096 points of data, the same 4096 point data record has been shifted in time by 4096 points and copied onto the graph. The FFT assumes that the 4096 data points represent a periodic waveform that extends to infinity in both directions. Because of this assumed periodicity, the calculation time of the FFT is reduced significantly and a smaller number of samples is required. Observe Figure 3. The waveform has been mirrored in the same way as Figure 1, except the record now contains 1.1 cycles instead of the original 1.0 cycles of Figure 1. It is obvious that if this is to be the signal that we perform the FFT on, the results will be degraded.

The characteristics of non-coherent sampling are obvious for gross errors, but are illusive with smaller error. Figure 4 is the FFT spectrum of a coherently sampled ideal 10-bit A/D converter. Notice there is no significant activity below -80db and the harmonic components are virtually nonexistent. Conversely, adjusting the coherence relationship to reflect a

change in M of as little as 0.005, the harmonic components are significantly increased, and a unique condition called spreading occurs. Spreading, sometimes referred to as smearing or leakage, causes a spike centered around the frequency bin of the fundamental. The width of the spike is an indication of the magnitude of non-coherence. A concept crucial to understanding the nature of the problem is interpreting what a 0.005 change in M really means with respect to  $f_{\parallel N}$  and  $f_{\rm S}$ . If N and  $f_{\rm S}$  stay constant, and M is increased by  $f_{\rm S}/N^*0.005$  causing leakage in the time domain window that leads to non-coherence.

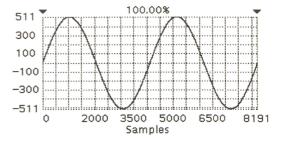


FIGURE 2. TRANSIENT RESPONSE OF A COHERENTLY SAMPLED DATASET AS SEEN BY FFT

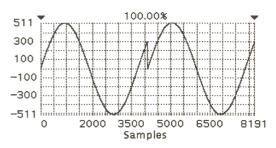


FIGURE 3. TRANSIENT RESPONSE OF A NON-COHERENTLY SAMPLED DATASET AS SEEN BY FFT

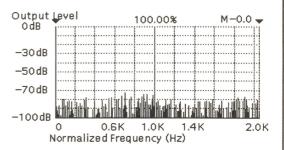


FIGURE 4. FFT SPECTRUM OF A COHERENTLY SAMPLED WAVEFORM

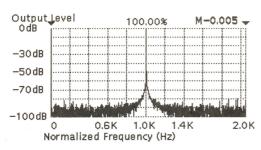


FIGURE 5. FFT SPECTRUM OF A NON-COHERENTLY SAM-PLED WAVEFORM

An important specification for A/D testing is ENOB or Effective Number of Bits. Figure 6 shows the effect on ENOB performance of a shift in M from M-0.5 to M+0.5. Since the data is based on an Ideal converter, we expect to be able to achieve 10-bit accuracy. Indeed, there is a region where 10 bits is achievable, but it is very slim. The acuity of this region highlights why coherence must be accurately observed. Although, Figure 6 is somewhat misleading. Assuming the input frequency was 10MHz, the range of Figure 6 would represent an input frequency range from 9995117Hz to 10004883Hz. In most instances, high frequency equipment will perform within 1Hz of the programmed value resulting in a range of ±0.5Hz or a variability in M of ±0.00005 for our high-frequency example. Further narrowing in on the ideal range of variability for M, Figure 7 shows the change in ENOB for a change in M of ±0.0005. The assumed accuracy of our high-frequency source puts it within the 9.95 - 10.0 bit range for an Ideal signal.

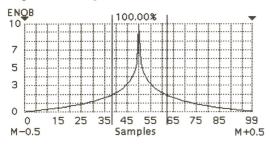


FIGURE 6. ENOB vs M FOR M-0.5 TO M+0.5

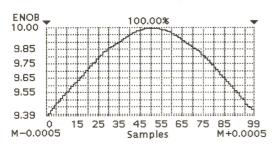


FIGURE 7. ENOB vs M FOR M-0.0005 TO M+0.0005

#### Unwrapping

A coherently sampled sine wave can be reassembled using a concept called unwrapping. Figure 8 shows a sinewave with M=11 sampled N=4096 times. Figure 9 is the same waveform after unwrapping is applied. If a waveform has been coherently sampled, the unwrapped waveform should look like one cycle sampled N times.

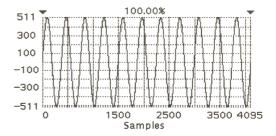


FIGURE 8. COHERENTLY SAMPLED WAVEFORM FOR M = 11

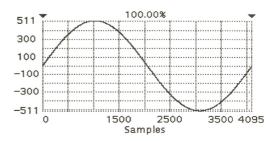


FIGURE 9. COHERENTLY SAMPLED WAVEFORM AFTER UNWRAP FOR M = 11

#### Windowing

Leakage is not a problem in all cases. It does not affect transient data as long as the transient occurrence is fully contained within the sample window. Leakage only occurs when the FFT is used to extrapolate frequency information from the sampled waveform. The actual source of leakage is not the signal itself but the window used in acquisition. The amount of leakage depends on the window shape and how the signal fits into the window.

Consider the coherently sampled waveform of Figure 12. The window of acquisition is rectangular and precisely set so that an integer number of cycles are captured. Therefore, leakage does not occur, the noise floor is nearly ideal for a 10 bit device, and harmonic distortion is nonexistent. In many cases the signal or sampling variables can not be precisely controlled. This makes it difficult to obtain exactly an integer number of cycles. But, leakage can be avoided or controlled by modifying the window to fit the data or to modify the data to a better form.

#### **Application Note 9675**

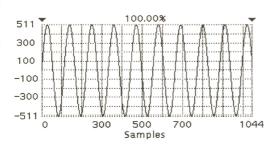


FIGURE 10. 9.5 CYCLE SINE WAVE

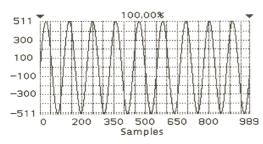


FIGURE 11. 9.0 CYCLE SINE WAVE

### Resampling and Interpolative Resampling

For example, if 9.5 cycles of a waveform are captured, the data window can be shortened to disregard the extra 0.5 cycle. Assuming the original data set is 1045 samples long, as in Figure 10, after discarding the extra 0.5 cycle, the data set is reduced to 990 samples as illustrated by Figure 11. A 990 point DFT can now be performed on the modified data to produce accurate results free of leakage. This presents a problem to FFT algorithms that are limited to power of 2 sample sets. There is, however, a solution. The new sample set can be resampled to fit a given sample size or interpolation techniques can be applied to fit the waveform into the appropriately sized sample set. The 9.0 cycle waveform of Figure 11 was resampled to provide 1024 samples. Figure 15 shows the affects of the linear resampling in the frequency domain. Figure 14 is a similar example except the data has been resampled using linear interpolation. Linear resampling preserves the levels of the original data and avoids leakage, but does produce a more discontinuous waveform leading to harmonic distortion. Linear interpolative resampling circumvents this problem but does not entirely preserve the original data. Figure 12 is provided as a reference.

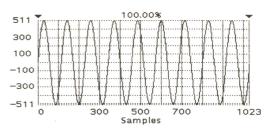


FIGURE 12. COHERENT 9.0 CYCLE SINEWAVE

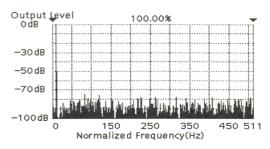


FIGURE 13. FFT OF COHERENT 9.0 CYCLE SINEWAVE

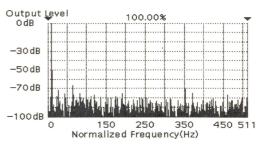


FIGURE 14. FFT OF FIGURE 11 AFTER INTERPOLATION

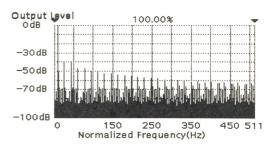


FIGURE 15. FFT OF FIGURE 11 AFTER RESAMPLING

#### **Different Window Shapes**

Since almost periodic data does not have a definable period, the above techniques are not applicable. Windowing the data can however force the data to begin and end at the same or nearly the same level. The technique of mathematical windowing is accomplished by multiplying the sampled waveform by an appropriate function. This prevents discontinuity at the window edge. Eliminating the discontinuity does not always eliminate leakage, but it does help to reduce it.

There are several functions that taper at the window edges. They are shown in Table 1. The first column is the actual window which should be applied to the sampled signal. The second column defines the shape equation for each window. As a basis for comparison, the third column contains the normalized frequency domain magnitude for each window. The fourth column lists the peak magnitude in the frequency domain as compared to that of the rectangular window. The decreased major lobe magnitude is due to the addressed area (energy) of each window as compared to the rectangular window. Adjusting the amplitude of the window will accommodate this difference. The fifth column lists the amplitude of the highest side-lobe in decibels referenced to the major lobe peak.

The 3dB bandwidth of the major lobe is given in the sixth column. These bandwidth values are normalized to Beta, the reciprocal of the window's time duration. The last column of parameters lists the theoretical rate of decay (roll-off) of the side lobes.

In choosing a windowing function, the bandwidth and side lobe levels should be considered. In general, the lower the side lobes, the less leakage in the frequency domain of the windowed data. However, lowering the side lobes also results in more energy being concentrated in widening the major lobe. Figures 17 and 18 illustrate these qualities. The Extended Cosine Bell has a very narrow major lobe and very high side lobes whereas the Parzen window has very low side lobes but a wide major lobe. Figure 16 is provided as a reference. Table 1 lists the windows in order of decreasing side lobe level and as a result they are listed in order of increasing bandwidth. The exception is the Hamming because of its non-zero edges.

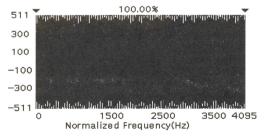
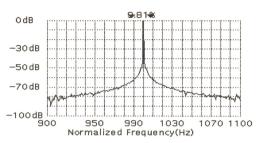


FIGURE 16A. RECTANGULAR WINDOWED SINE WAVE



### FIGURE 16B. FFT SPECTRUM OF RECTANGULAR WINDOWED SINE WAVE

In terms of spectral separation, the greater the window's bandwidth, the less selectivity it provides for equal amplitude and adjacent frequencies. The wide bandwidth causes them to blur together. Alternatively, lower side lobe levels increases selectivity between adjacent components of unequal amplitudes since the lower magnitude components are no longer buried in the leakage skirts. Usually, it takes a lot of trial and error before the correct window function is selected. Figures 19 through 22 provide some insight into the trial and error pitfalls involved in selecting the correct window shape. In Figure 21, the large side lobes of the Extended Cosine Bell window overshadow the original signals apparent in Figure 19. Conversely, the wide major lobes of the Parzen Window absorb one and another as is evident by Figure 22. A compromise can be arrived at by using the Hanning shape. The FFT spectrum of Figure 20 has reduced leakage to a minimum while continuing to preserve spectral separation of the signals.

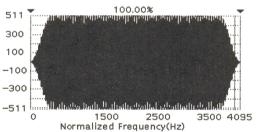


FIGURE 17A. EXTENDED COSINE BELL WINDOWED SINE WAVE

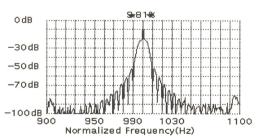


FIGURE 17B. FFT OF EXTENDED COSINE BELL WINDOWED SINE WAVE

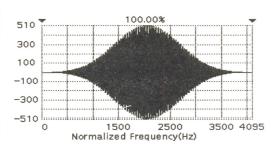


FIGURE 18A. PARZEN WINDOWED SINEWAVE

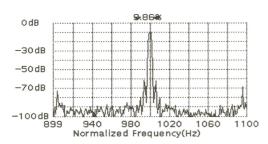


FIGURE 18B. FFT SPECTRUM OF PARZEN WINDOWED SINEWAVE

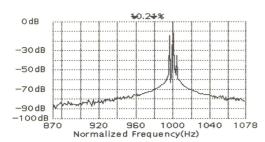


FIGURE 19. FFT OF A 3-SIGNAL NON-COHERENT WAVEFORM

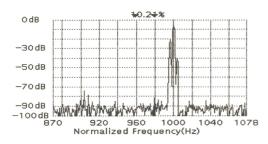


FIGURE 20. FFT OF WAVEFORM OF FIGURE 18 WINDOWED WITH A HANNING SHAPE

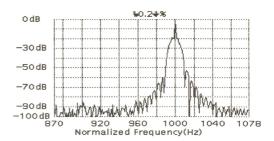


FIGURE 21. FFT OF WAVEFORM OF FIGURE 18 WINDOWED WITH AN EXTENDED COSINE BELL SHAPE

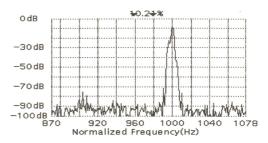


FIGURE 22. FFT OF WAVEFORM OF FIGURE 18 WINDOWED WITH A PARZEN SHAPE

#### Conclusion

Coherent testing of A/D converters provides an ideal environment for evaluating the spectral response. The rules for coherent sampling are simple. M must be prime or odd. N must be a factor of 2. The sampling and input frequency and phase must be stable and predictable. There are two methods for evaluating coherence. Unwrapping the waveform will show non-coherent anomalies in the time domain. The algorithm for unwrapping is provided below. Another indication of noncoherence is leakage skirting, or spreading, in the FFT spectrum. In the case of a single tone, sine wave curve fitting can be used to calculate signal to noise ratio. When the rules of coherent testing are not observed, windowing may be applied to try and resolve spectral components.

When should windowing be used, and when should it not? If windowing is needed, which windowing function should be used? The answer to these questions depend upon what you are looking for. If a waveform has adjacent components of nearly equal magnitude, you may want to leave the data in the rectangular window. The increased major lobe width of another window shape may cause the two adjacent components to leak into each other and appear as one. On the other hand, if there is a small component near a large component, a low side-lobe window will decrease leakage around the large component and make the small component easier to distinguish. Ultimately, selecting the window is a compromise between needed side-lobe reduction and a tolerable increase in major lobe width.

#### TABLE 1. WINDOWING FUNCTIONS

UNITY AMPLITUDE WINDOW	SHAPE EQUATION	FREQUENCY DOMAIN MAGNITUDE	MAJOR LOBE HEIGHT	HIGHEST SIDE LOBE (dB)	BAND- WIDTH (3dB)	THEORETICAL ROLL-OFF
Rectangle  T=1/β  T=1/β	A = 1 for t = 0 to T	Y	Т	-13.2	0.86β	6
Extended Cosine Bell	A = $0.5(1-\cos(2\pi5t/T))$ for t = 0 to T/10 and t = $9T/10$ to T A = 1 for t = T/10 to $9T/10$		0.9T	-13.5	0.95β	18 Beyond 5B
Half Cycle Sine	$A = \sin(2\pi 0.5t/T)$ for t = 0 to T		0.64T	-22.4	1.15β	12
Triangle	A = 2t/T for t = 0 to T/2 A = -2t/T +2 for t = T/2 to T		0.5T	-26.7	1.27β	12
Cosine <sup>2</sup> (Hanning)	A = 0.5(1-cos(2πt/T)) for t = 0 to T		0.5T	-31.6	1.39β	18
Half Cycle Sine <sup>3</sup>	A = $\sin^3(2\pi 0.5t/T)$ for t = 0 to T		0.42T	-39.5	1.61β	24
Hamming	A = $0.08 + 0.46(1-\cos(2\pi t/T))$ for t = 0 to T		0.54T	-41.9	1.26β	6 Beyond 5B
Cosine <sup>4</sup>	A = $(0.5(1-\cos(2\pi t/T)))^2$ for t = 0 to T		0.36T	-46.9	1.79β	30
Parzen	A = $1-6(2t/T-1)^2 + 6 2t/T-1 ^3$ for t = $T/4$ to $3T/4$ A = $2(1- 2t/T-1 )^3$ for t = 0 to $T/4$ and t = $3T/4$ to T		0.37T	-53.2	1.81β	24

#### **Application Note 9675**

#### **Algorithms**

The coherence algorithm accepts known values for each of the coherence parameters and evaluates the closest value to the initial guess so that all values are integer related. N must be a power of 2 greater than 4. The error is not more than  $\pm (N/2)$  for f\_s and  $\pm (f_s/N)$  for f\_in.

The unwrap algorithm accepts two arrays(tsample and unwrap) the number of cycles captured(M), and the array length(N). The tsample array is the sampled waveform. The unwrap array is the unwrapped waveform. It should look like one cycle of the waveform but sampled N times. The variable M is the number of cycles in the record.

The alias algorithm accepts N and fbin as variables and computes the correct FFT bin assignment of fbin.

#### References

- [1] R.W. Ramirez, *The FFT Fundamentals and Concepts*, 1986, pgs. 140-141.
- [2] M.. Mahoney, Tutorial DSP-Based Testing of Analog and Mixed-Signal Circuits, 1987, pgs. 45-58.

```
void coherence(f in,f s,N,M)
      double *f_in,*f_s;
      int N.*M:
      int K;
             K = (*f s + N/2)/N;
            ^*M = (int)(^*f_in)/(int)K/2^*2+1;
           *f s = K*N;
           f_{in} = K^{*}(M);
      /* Sample Call */
      /* coherence(&f_in,f_s,N,M); */
      }/* End of Coherence Algorithm */
void unwrap_algorithm(tsample,unwrap,size_cap.M)
      int tsample[],unwrap[],M,size_cap;
      int i.i:
      for (i=0; i<size cap;i++)
            j = M*i % size_ cap:
            unwrap[j] = tsample[i];
      /* Sample Call */
      /* unwrap_algorithm(tsample,unwrap,size_cap,f_bin);
      }/* End of Unwrap Algorithm */
void alias algorithm(fbin.N)
      int *fbin,N;
      *fbin=fabs((float) ( *fbin - N *((*fbin+N/2)/N) ) );
      if (*fbin == N/2) *fbin = 0;
      /* Sample Call */
      /* alias_algorithm(&fbin,M); */
      }/* End of Alias Algorithm */
```

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HI5710A	HI5710EVAL		
HI5746	HI5746EVAL1		
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HI5805	HI5805EVAL1		
HI5808	HI5808EVAL1		

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# Development Tools (Continued)

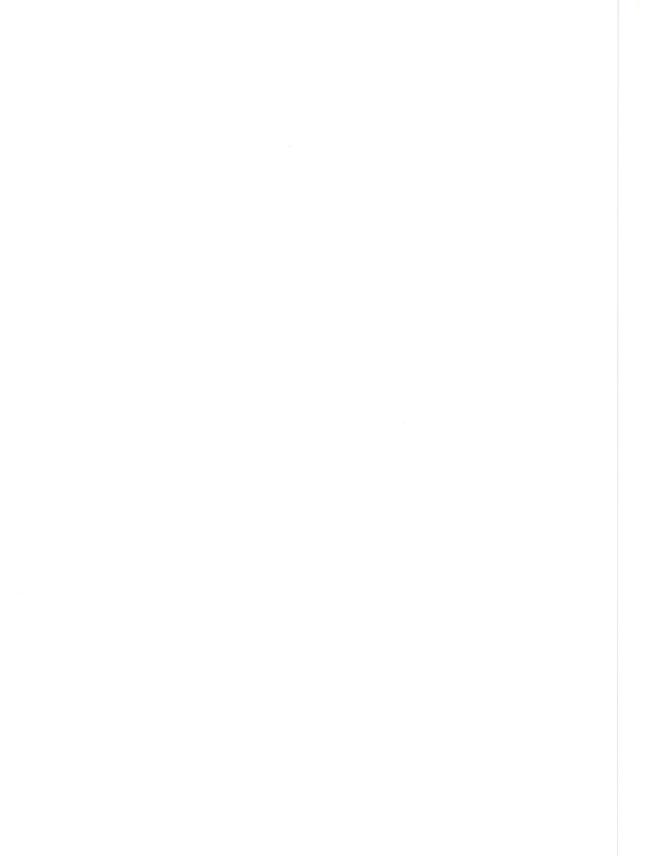
PART NUMBER	DEVELOPMENT TOOL
Linear	
HFA1100, HFA1120	HFA11XXEVAL, SPICE Model Available
HFA1110	HFA1110EVAL
HFA3046, HFA3096, HFA3127, HFA3128	SPICE Model Available
HFA3600	HFA3600EVAL
Digital Signal Processing	
DSP Evaluation Platform	HSP-EVAL
HSP43124	SERINADE™ Development Software
HSP43220	DECI•MATE™ Development Software
HSP45116	HSP45116-DB
HSP50016	HSP50016-EV
HSP50110	HSP50110/210EVAL
HSP50210	HSP50110/210EVAL

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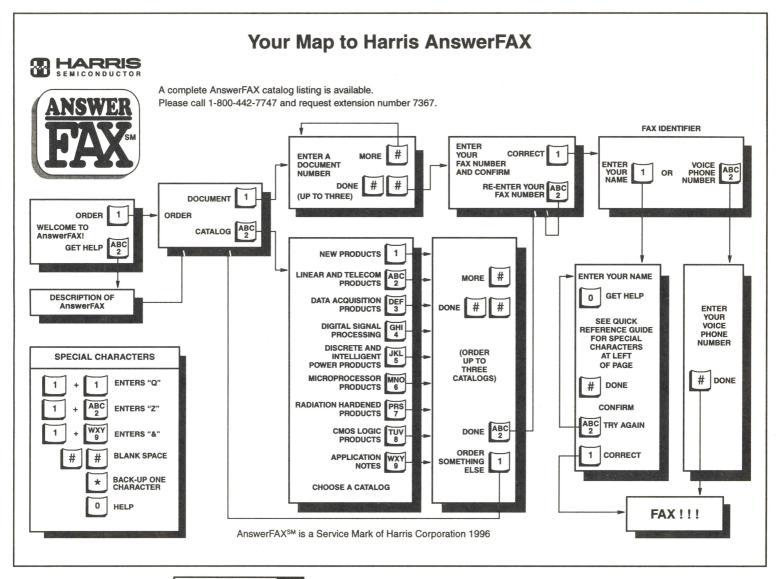
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#### Harris AnswerFAX Data Book Request Form - Document #199 **Data Books Available Now**

PUB. NUMBER	DATA BOOK/DESCRIPTIO	DN .
7004	Complete Set of Commercial Harris Data Books	
7005	Complete Set of Commercial and Military Harris Data Books	
DB223B	POWER MOSFETs (1994: 1,328pp) This data book contains detailed technical information including standard power MOSFETs (th popular RF-series types, the IRF-series of industry replacement types, and JEDEC types), MegaFETs, logic-level power MOSFET (L2FETs), ruggedized power MOSFETs, advanced discrete, high-reliability and radiation-hardened power MOSFETs.	
DB316	POWER MOSFET DATA BOOK SUPPLEMENT (1996: 380pp) This data book co and also updates some of the data sheets in the Power MOSFET Data Boo specification for these products.	k DB223B. These data sheets contain the detaile
DB235B	<b>RADIATION HARDENED</b> (1993: 2,232pp) The Harris radiation-hardened produ logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 standard cells and custom devices.	
DB260.2	CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS (1995: 436pp) Semiconductor CDP6805 products for commercial applications and supersedes Harris, GE, RCA or Intersil names.	
DB301B	DATA ACQUISITION (1994: 1,104pp) Product specifications on A/D converters (D/A converters, switches, multiplexers, and other products.	display, integrating, successive approximation, flash
DB302B	<b>DIGITAL SIGNAL PROCESSING</b> (1994: 528pp) Product specifications on synthesizers, multipliers, special function devices (such as address sequencers,	binary correlators, histogrammer).
DB303.1	MICROPROCESSOR PRODUCTS (1997: 1,260pp) In the ever-changing IC mature commitment to continue servicing mature CMOS products and technical architecture microprocessor families for markets including cellular communical medical and avionics instrumentation.	ologies. As always, we will supply mature, standar
DB304.1	INTELLIGENT POWER ICs (1994: 946pp) This data book includes a complete sonotes with design details for specific applications of Harris products, and a descri	
DB309.1	MCT/IGBT/DIODES (1995: 706pp) This MCT/IGBT/Diodes data book represents the full line of these products made by H Semiconductor Discrete Power Products for commercial applications.	
DB319	HARRIS IGBT UFS SERIES SUPPLEMENT (1997: 164pp) The UFS series IGBT (Insulated Gate Bipolar Transistor) Data B Supplement represents a new generation of IGBT products from Harris Semiconductor Discrete Power Products for commer applications. This data book supplement describes Harris Semiconductor's line of UFS (Ultra Fast Switching) IGBTs.	
DB314	SIGNAL PROCESSING NEW RELEASES (1995: 690pp) This data book represents the newest products made by Harris Semiconduc Data Acquisition Products, Linear Products, Telecom Products and Digital Signal Processing Products for commercial applications.	
DB315.1	CROSS-REFERENCE GUIDE (1996: 554pp) Listing of semiconductor products that are second-sourced by Harris Semiconductor.	
DB317	COMMUNICATIONS DATA BOOK (1997: 708pp) Technical information including data sheets and application notes for a variety of H Integrated Circuits targeted for the communications industry. These products include the PRISM 2.4GHz DSSS Wireless Transc Chip Set, the new HC5517 Ringing SLIC as well as Standard Linear, Data Acquisition, DSP and Power products.	
DB321	APPLICATIONS FOR COMMUNICATION ICs (1997: 392pp) Application Notes range from wireless PRISM™ 2.4GHz WLAN chip set to Telecom HC5517 ringing SI	
DB318	LPT/FCT CMOS LOGIC EXPANSION (1997: 620pp) This data book fully describes Harris Semiconductor's LPT and FCT CMOS Local ICs. It includes a complete set of data sheets for product specifications, application notes and techbriefs with design details for special applications of Harris products, and a description of the Harris Quality and Reliability program.	
DB450.4	TRANSIENT VOLTAGE SUPPRESSION DEVICES (1995: 400pp) Product sp general informational chapters such as: "Voltage Transients - An Overview," "Suppression - Automotive Transients."	
DB500.3	LINEAR ICs (1996/97: 1446pp) Harris offers an extensive line of Linear compor Amps, Comparators, Sample/Hold Amps, Video Crosspoint Switches, Special Ar	
Analog Military	ANALOG MILITARY (1989: 1,264pp) This data book describes Harris' military line circuits.	e of Linear, Data Acquisition, and Telecommunication
DB312	ANALOG MILITARY DATA BOOK SUPPLEMENT (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 19 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear a Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiati Hardened Product Data Book (document #DB235B)	
PSG201.24		
SG103	CMOS LOGIC SELECTION GUIDE (1994: 288pp) This product selection guide contains technical information on Harris Semiconduc High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Spe CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.	
BR-057.3	AnswerFAX CATALOG (Fall 1996: 112pp) A Complete AnswerFAX Catalog listing	
IAME:	COMPANY	
	COMPANY: ADDRESS:	

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# June 10, 1997 AnswerFAX Technical Support Linear & Telecom Communication Products Listing

	Υ	
AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
27007	BR-007	Complete Listing of Harris Sales Offices, Representatives and Authorized Distributors World Wide (10 pages)
27027	BR-027	Ordering Nomenclature Guide (20 pages) BR-027.1
7049	PCS03.1	PRISM™ Development Kits (2 pages)
7071	DB317 Section 08	1997 Communications Databook Quality & Reliability (20 pages)
LINEAR ARTI	CLE REPRINTS	
7030	Wireless Design & Development 6/6/95	System Considerations in Spread-Spectrum Designs (3 pages)
7036	RF Design Cover Story 10/95	Four-Chip Set Supports High- Speed DSSS PCMCIA Applications (5 pages)
LINEAR DATA	SHEETS	
341	CA3045, CA3046	General Purpose NPN Transistor Arrays (6 pages) FN341.3
480	CA3081, CA3082	General Purpose High Current NPN Transistor Arrays (3 pages) FN480.3
481	CA3083	General Purpose High Current NPN Transistor Array (4 pages) FN481.3
483	CA3086	General Purpose NPN Transistor Array (5 pages) FN483.3
595	CA3096, CA3096A, CA3096C	NPN/PNP Transistor Arrays (12 pages) FN595.3
662	CA3127	High Frequency NPN Transistor Array (6 pages) FN662.3
532	CA3146, CA3146A, CA3183, CA3183A	High-Voltage Transistor Arrays (8 pages) FN532.3
1345	CA3227, CA3246	High-Frequency NPN Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz (5 pages) FN1345.3
1076	CD22100	CMOS 4 x 4 Cros0spoint Switch with Control Memory High- Voltage Type (20V Rating) (9 pages) FN1076.3
2871	CD22101, CD22102	CMOS 4 x 4 x 2 Crosspoint Switch with Control Memory (12 pages) FN2871.2

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1310	CD22103A	CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/ 8.448Mb/s Transmission Applications (6 pages) FN1310.3
1695	CD22202, CD22203	5V Low Power DTMF Receiver (6 pages) FN1695.3
1696	CD22204	5V Low Power Subscriber DTMF Receiver (5 pages) FN1696.3
1368	CD22301	Monolithic PCM Repeater (5 pages) FN1368.3
2491	CD22M3493	12 x 8 x 1 BiMOS-E Crosspoint Switch (5 pages) FN2491.4
3587	CD22M3493R2536	12 x 8 x 1 BiMOS-E Crosspoint Switch (7 pages)
2793	CD22M3494	16 x 8 x 1 BiMOS-E Crosspoint Switch (6 pages) FN2793.5
1682	CD22354A, CD22357A	CMOS Single-Chip, Full- Feature PCM CODEC (10 pages) FN1682.3
1257	CD22859	Monolithic Silicon COS/MOS Dual-Tone Multifrequency Tone Generator (5 pages) FN1257.3
1719	CD74HC22106, CD74HCT22106	QMOS 8 x 8 x 1 Crosspoint Switches with Memory Control (9 pages) FN1719.3
3675	HC5509A1R3060	SLIC Subscriber Line Interface Circuit (10 pages) FN3675.2
2799	HC-5509B	SLIC Subscriber Line Interface Circuit (10 pages) FN2799.4
4126	HC-5509B 3999-003	SLIC Subscriber Line Interface Circuit (10 pages) FN4126
3963	HC5513	SLIC Subscriber Line Interface Circuit (18 pages) FN3963.7
4235	HC5515	SLIC Subscriber Line Interface Circuit (18 pages) FN4235.1
4147	HC5517	Ringing SLIC Subscriber Line Interface Circuit (18 pages) FN4147.1
4232	HC5519	SLIC Subscriber Line Interface Circuit (1 page) FN4232
4148	HC5520	CO/PABX Polarity Reversal Subscriber Line Interface Circuit (20 pages) FN4148.2
4265	HC5521	SLIC Subscriber Line Interface Circuit (1 pages) FN4265



# June 10, 1997 AnswerFAX Technical Support Linear & Telecom Communication Products Listing

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DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
4144	HC5523	SLIC Subscriber Line Interface Circuit (18 pages) FN4144.1
2798	HC-5524	SLIC Subscriber Line Interface Circuit (12 pages) FN2798.3
4151	HC5526	SLIC Subscriber Line Interface Circuit (18 pages) FN4151.1
2887	HC-5560	PCM Transcoder (9 pages) FN2887.2
4323	HC55171	5 REN Ringing SLIC Subscriber Line Interface Circuit (3 pages) FN4323
2889	HC-55564	Continuously Variable Slope Delta-Modulator (CVSD) (6 pages) FN2889.2
4260	HC6094	ADSL Analog Front End Chip (2 pages) FN4260
2945	HFA1100, HFA1120	850MHz, Low Distortion Current Feedback Operational Amplifiers (10 pages) FN2945.5
3615	HFA1100/883	850MHz Current Feedback Amplifier (16 pages)
3597	HFA1102	600MHz Current Feedback Amplifier with Compensation Pin (5 pages) FN3597.2
3547	HFA1102Y	Ultra High-Speed Current Feedback Amplifier with Compensation Pin (4 pages)
2944	HFA1110	750MHz, Low Distortion Unity Gain, Closed Loop Buffer (8 pages) FN2944.5
3620	HFA1110/883	750MHz, Low Distortion Unity Gain, Closed Loop Buffer (15 pages)
2992	HFA1112	850MHz, Low Distortion Programmable Gain Buffer Amplifier (12 pages) FN2992.4
3610	HFA1112/883	Ultra High Speed Programmable Gain Buffer Amplifier (18 pages)
1342	HFA1113	850MHz, Low Distortion, Output Limiting, Programmable Gain, Buffer Amplifier (15 pages) FN1342.3
3618	HFA1113/883	Output Limiting, Ultra High Speed Programmable Gain, Buffer Amplifier (22 pages)
3151	HFA1114	850MHz Video Cable Driving Buffer (5 pages) FN3151.3

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
3369	HFA1130	850MHz, Output Limiting, Low Distortion Current Feedback Operational Amplifier (11 pages) FN3369.1
3076		Ultra High Frequency Transistor Arrays (9 pages) FN3076.8
3663	HFA3101	Gilbert Cell UHF Transistor Array (12 pages) FN3663.3
3635	HFA3102	Dual Long-Tailed Pair Transistor Array (6 pages) FN3635.2
4288	HFA3421	1.7GHz - 2.3GHz Low Noise Amplifier (3 pages) FN4288
4131	HFA3424	2.4GHz - 2.5GHz Low Noise Amplifier (4 pages) FN4131.2
4062	HFA3524	2.5GHz/600MHz Dual Frequency Synthesizer (15 pages) FN4062.4
3655	HFA3600	Low-Noise Amplifier/Mixer (16 pages) FN3655.2
4066	HFA3624	2.4GHz Up/Down Converter (18 pages) FN4066.6
4240	HFA3661	2.0GHz to 2.7GHz DownConverter (6 pages) FN4240
4241	HFA3663	2.3GHz UpConverter with Gain Control (6 pages) FN4241
4242	HFA3664	2.7GHz UpConverter with Gain Control (6 pages) FN4242
4067	HFA3724	400MHz Quadrature IF Modulator/Demodulator (22 pages) FN4067.4
4236	HFA3761	400MHz AGC and Quadrature IF Demodulator (10 pages) FN4236
4237	HFA3763	400MHz Quadrature Modulator and AGC (10 pages) FN4237
4308	HFA3824	Direct Sequence Spread Spectrum Baseband Processor (41 pages) FN4308
4132	HFA3925	2.4GHz - 2.5GHz 250mW Power Amplifier (7 pages) FN4132.3
4282	HFA3926	2.0GHz - 2.7GHz 250mW Power Amplifier (8 pages) FN4282
4063	PRISM™ 2.4GHz Chip Set	Direct Sequence Spread Spectrum Wireless Transceiver Chip Set (2 pages) FN4063.5

# June 11, 1997 AnswerFAX Technical Support Linear & Telecom Communication Products Listing

AnswerFAX		
DOCUMENT	PART	
NUMBER	NUMBER	DESCRIPTION
4238	PRISM™ Full Duplex Radio Front End	For Voice and Data (1 page) FN4238.1
LINEAR AND	TELECOM APPLICA	TION NOTES
99640	(General Communications) AN9640	Glossary of Communication Terms (31 pages) AN9640.1
99666	PRISM Chip Set AN9666	Wireless LAN Evaluation Kit SW Installation and Usage (3 pages) AN9666
99627	<b>HFA3424</b> AN9627	Using the HFA3424 Evaluation Board (2 pagers) AN9627
99630	HFA3524EVAL PRISM™ Chip Set AN9630	Using The HFA3524 Evaluation Board (13 pages) AN9630
99618	HFA3624EVAL, PRISM™ Chip Set AN9618	Using the PRISM™ HFA3624 Evaluation Board (12 pages) AN9618.2
99714	HFA3661EVAL, PRISM™ Chip Set AN9714	Using the HFA3661 Evaluation Board Preliminary Release (2 pages) AN9714
99713	HFA3663EVAL, HFA3664EVAL, PRISM™ Chip Set AN9713	Using the HFA3663 and HFA3664 Evaluation Board Preliminary Release (2 pages) AN9713
99711	HFA3761EVAL, PRISM™ Chip Set AN9711	Using the PRISM™ HFA3761 Evaluation Board Preliminary Release (4 pages) AN9711
99712	HFA3763EVAL, PRISM™ Chip Set AN9712	Using the PRISM™ HFA3763 Evaluation Board Preliminary Release (4 pages) AN9712
99638	HFA3925EVAL, PRISM™ Chip Set AN9638	Using The HFA3925 Evaluation Board (5 pages) AN9638
99614	PRISM™ Chip Set AN9614	Low Data Rate Applications (3 pages) AN9614.1
99617	PRISM™ Chip Set AN9617	Hardware/Software Interface Description for PRISM™ Radio Design with an Example Using the AM79C930 Media Access Controller (13 pages) AN9617.1
99622	PRISM™ Chip Set AN9622	Using the PRISM™ HFA3724 Evaluation Board (16 pages) AN9622
99623	PRISM™ Chip Set AN9623	Measurements Using the PRISM™ Chip Set (4 pages) AN9623
99624	PRISM™ Chip Set AN9624	PRISM™ DSSS PC Card Wireless LAN Description (6 pages) AN9624.3

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DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	
99633	PRISM™ Chip Set AN9633	Processing Gain for Direct Sequence Spread Spectrum Communication Systems and PRISM™ (4 pages) AN9633	
99665	PRISM™ Chip Set AN9665	PRISM™ Power Management Modes (7 pages) AN9665	
99673	PRISM™ Chip Set AN9673	PRISM™ DSSS Radio Operation in Continuous Links (2 pages) AN9673	
99639	PRISM™ Chip Set AN9639	Harris PRISM™ Wireless LAN Network Connectivity and Utility SW (non IEEE802.11) For the WLAN Evaluation Kit (3 pages) AN9639	
99700	CDP68HC05, PRISM ChipSet AN9700	Interfacing the CDP68HC05 Microcontroller Family with PRISM™ Wireless Products (5 pages) AN9700	
99537	HC5513, HC5526, HC5513EVAL, HC5526EVAL AN9537	Operation of the HC5513, HC5526 Evaluation Board (HC5513EVAL, HC5526EVAL) (7 pages) AN9537.2	
99606	HC5513EVAL, HC5517, HC5517EVAL, HC5523EVAL AN9606	Operation of the HC5517 Evaluation Board (HC5517EVAL) (10 pages) AN9606.4	
99608	HC-5509B, HC5509A1R3060, HC5517, HC-5524 AN9608	Implementing Pulse Metering for the HC5509 Series of SLICs (4 pages) AN9608	
99628	HC5509B, HC5509A1R3060, HC5517, HC5524 AN9628	AC Voltage Gain for the HC5509 Series of SLICs (2 pages) AN9628.1	
99632	HC5523, HC5515 AN9632	Operation of the HC5523, HC5515 Evaluation Board (9 pages) AN9632	
99636	HC5513EVAL, HC5517, HC5517EVAL, HC5523EVAL AN9636	Implementing an Analog Port for ISDN Using the HC5517 (14 pages) AN9636.1	
99667	HC5509B, HC5524 AN9667	Selecting the Proper Ring Trip Filter Capacitor (C <sub>2</sub> ) for the HC5509B and HC5524 SLICs (4 pages) AN9667	
LINEAR AND TELECOM TECHBRIEFS			
82337	PRISM™ Chip Set TB337	A Brief Tutorial on Spread Spectrum and Packet Radio (3 pages) TB337.1	



# June 10, 1997 AnswerFAX Technical Support Digital Signal Processing Communication Products

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DOCUMENT NUMBER	PART NUMBER	DESCRIPTION			
DSP ARTICL	DSP ARTICLE REPRINTS				
7036	RF Design Cover Story 10/95	Four-Chip Set Supports High- Speed DSSS PCMCIA Applications (5 pages)			
DSP DATA SI	HEETS				
4064	HSP3824	Direct Sequence Spread Spectrum Baseband Processor (39 pages) FN4064.6			
2808	HSP43168	Dual FIR Filter (24 pages) FN2808.6			
3177	HSP43168/883	Dual FIR Filter (8 pages)			
3365	HSP43216	Halfband Filter (21 pages) FN3365.5			
2486	HSP43220	Decimating Digital Filter (19 pages) FN2486.6			
2802	HSP43220/883	Decimating Digital Filter (7 pages)			
2810	HSP45102	12-Bit Numerically Controlled Oscillator (7 pages) FN2810.5			
2809	HSP45106	16-Bit Numerically Controlled Oscillator (10 pages) FN2809.3			
2815	HSP45106/883	16-Bit Numerically Controlled Oscillator (6 pages)			
2485	HSP45116	Numerically Controlled Oscillator/ Modulator (18 pages) FN2485.6			
4156	HSP45116A	Numerically Controlled Oscillator/ Modulator (16 pages) FN4156.1			
2813	HSP45116/883	Numerically Controlled Oscillator/ Modulator (7 pages)			
3288	HSP50016	Digital Down Converter (27 pages) FN3288.4			
3651	HSP50110	Digital Quadrature Tuner (23 pages) FN3651.3			
4149	HSP50110/ 210EVAL	DSP Demodulator Evaluation Board (32 pages) FN4149			
3652	HSP50210	Digital Costas Loop (49 pages) FN3652.3			
4305	ST-114 HSP50214EVAL	ST-114 Harris HSP50214 Evaluation Board (2 pages) FN4305			
4266	HSP50214	Programmable Downconverter (1 page) FN4266			
4346	HSP50215	Digital UpConverter FN4346			
4162	HSP50306	Digital QPSK Demodulator (8 pages) FN4162.1			

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION			
4219	HSP50307	Burst QPSK Modulator (9 pages) FN4219			
4239	HSP50307EVAL1	Burst QPSK Modulator Evaluation Board (21 pages) FN4239			
DSP DEVELO	DSP DEVELOPMENT TOOLS				
4063	PRISM™2.4GHz Chip Set	Direct Sequence Spread Spectrum Wireless Transceiver Chip Set (2 pages) FN4063.4			
DSP APPLICA	ATION NOTES				
99615	<b>HSP3824</b> AN9615	HSP3824 Evaluation Board and Associated Software (18 pages) AN9615			
99616	<b>HSP3824</b> AN9616	Programming the HSP3824 (17 pages) AN9616			
99701	HSP3824, CDP68HC05 AN9701	CRC-16 Algorithm for Packetized WLAN Protocols on the HSP3824 (2 pages) AN9701			
99603	HSP50016, HSP43124, HSP43168 AN9603	An Introduction to Digital Filters (HSP50016, HSP43124, HSP43168) (9 pages) AN9603			
99658	HSP43124, HSP43168, HSP43216, HSP50110, HSP50210 AN9658	Implementation of a High Rate Radio Receiver (HSP43124, HSP43168, HSP43216, HSP50110, HSP50210) (5 pages) AN9658			
99657	HSP50110, HSP50210, HSP50210, HSP50110/ 210EVAL, HSP50016EVAL, HSP50214, HSP43116, HSP43116A, HSP43116DB AN9657	Data Conversion Binary Code Formats (3 pages) AN9657.1			
99659	HSP50110/ 210EVAL AN9659	Using the HSP50110/210EVAL Example Configuration Files (7 pages) AN9659			
99676	HSP50110/ 210EVAL AN9676	Loading Custom Digital Filters Into the HSP50110/210EVAL (6 pages AN9676			
99715	HSP50110/ 210EVAL AN9715	Ten Tips for Successful HSP50110/210EVAL Board Operation (3 pages) AN9715			



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AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
99661	HSP50110, HSP50210, HSP43168 AN9661	Implementing Polyphase Filtering with the HSP50110 (DQT) HSP50210 (DCL) and the HSP43168 (DFF) (6 pages) AN9661
99720	<b>HSP50214</b> AN9720	Calculating Maximum Processing Rates of the PDC (HSP50214) (10 pages) AN9720
99617	PRISM™ Chip Set AN9617	Hardware/Software Interface Description for PRISM™ Radio Design with an Example Using the Am79C930 Media Access Controller. (13 pages) AN9617.1
99623	PRISM™ Chip Set AN9623	Packet Error Rate Measurements Using the PRISM™ Chip Set (4 pages) AN9623
99624	PRISM™ Chip Set AN9624.1	PRISM™ DSSS PC Card Wireless LAN Description (6 pages) AN9624.1
DSP TECH B	RIEFS	
82336	<b>HSP43168</b> TB336	3x3 10-Bit Convolver Using the HSP43168 (1 page) TB336
82314	HSP43168, HSP43220, HSP45116 TB314	Quadrature Down Conversion with the HSP45116, HSP43168 and HSP43220 (7 pages)
82311	HSP43220 TB311	HSP43220 - Design of Filters with Output Rates <2 (Passband + Transition) (2 pages)
82313	<b>HSP43220</b> TB313	Reading Out FIR Coefficients from the HSP43220 (1 page)
82309	<b>HSP43220</b> TB309	Notes on using the HSP43220 (3 pages)
82310	<b>HSP43220</b> TB310	Common Abuses of the HSP43220 (1 page)
82308	HSP43220 TB308	HSP43220 Deci•Mate Design Rule Checks (2 pages)
82312	<b>HSP43220</b> TB312	HDF Bypass in the HSP43220 (1 page)

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
82318	HSP45102, HSP45106 TB318	The NCO as a Stable, Accurate Synthesizer (3 pages)
82317	<b>HSP45106</b> TB317	Pipeline Delay Through the HSP45106 (2 pages)
82319	<b>HSP45106</b> TB319	Reading the Phase Accumulator of the HSP45106 (2 pages)
82327	<b>HSP45116</b> TB327	Using the HSP45116 as a Complex Multiplier Accumulator (4 pages)
82316	<b>HSP45116</b> TB316	Pipeline Delay Through the HSP45116 (1 pages)
82315	<b>HSP45116</b> TB315	Processing Signals at Increased Sample Rates with Mulitple HSP45116's (1 page)
82303	<b>HSP45256</b> TB303	HSP45256 Correction to Data Sheet (1 page)
82306	<b>HSP45256</b> TB306	Cascading Multiple HSP45256 Correlators (2 pages)
82307	<b>HSP45256</b> TB307	Correlation with Multibit Data using the HSP45256 (2 pages)
82305	HSP48410 TB305	Histogramming with a Variable Pixel Increment (2 pages)
82302	HSP48901 TB302	Notice to Specification Change HSP48901 (1 page)
82338	PRISM™ Chip Set TB338	Using the PRISM™ Chip Set for Timing Measurements (Ranging) (2 pages) TB338



# June 10, 1997 AnswerFAX Technical Support Data Acquisition Communication Products Listing

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
DATA ACQUIS	ITION ARTICLE	REPRINTS
7029	Electronics Design 3-20-95	Decipher High-Sample-Rate ADC Specs (8 pages)
7032	Electronic Products 5-95	Deciphering specs for high-speed D/A converters (4 pages)
DATA ACQUIS	ITION DATA SH	EETS
3950	HI5703	10-Bit, 40 MSPS A/D Converter (14 pages) FN3950.5
3921	HI5710A, CXD2310A	10-Bit, 20 MSPS A/D Converter (19 pages) FN3921.4
3949	HI5721	10-Bit, 125 MSPS High Speed D/A Converter (14 pages) FN3949.4
4070	HI5731	12-Bit, 100 MSPS High Speed D/A Converter (15 pages) FN4070.2
4071	HI5741	14-Bit, 100 MSPS High Speed D/A Converter (13 pages) FN4071.2
4129	HI5746	10-Bit, 40 MSPS A/D Converter (16 pages) FN4129.2
4130	HI5766	10-Bit, 60 MSPS A/D Converter (11 pages) FN4130.2
4319	HI5767	10-Bit, 20/40/60 MSPS, A/D Converter with Internal Voltage Reference (12 pages) FN4319
4024	HI5780, CXD2306	10-Bit, 80 MSPS High Speed, Low Power D/A Converter (7 pages) FN4024.3
2938	HI5800	12-Bit, 3 MSPS Sampling A/D Converter (14 pages) FN2938.9
4026	HI5804	12-Bit, 5 MSPS A/D Converter (10 pages) FN4026.2
3984	HI5805	12-Bit, 5 MSPS A/D Converter (11 pages) FN3984.3
4233	HI5808	12-Bit, 10 MSPS A/D Converter (13 pages) FN4233.1
4259	HI5905	14-Bit, 5 MSPS A/D Converter (1 page) FN4259
3581	HI20201, CX20201-1, CX20202-1	10-Bit, 160 MSPS Ultra High- Speed D/A Converter (10 pages) FN3581.4

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION				
DATA ACQUIS	DATA ACQUISITION APPLICATION NOTES					
99413	<b>HI5702</b> AN9413	Driving the Analog Input of the HI5702 (3 pages)				
99509	HI5702, HI5703, HSP43220, HSP45116 AN9509	Digital IF Sub Sampling Using the HI5702, HSP45116 and HSP43220 (5 pages) AN9509.1				
99501	<b>HI5721</b> AN9501	Understanding the HI5721 D/A Converter Spectral Specifications (3 pages) AN9501.1				
99619	<b>HI5741</b> AN9619	Optimizing Setup Conditions for High Accuracy Measurements of the HI5741 (4 pages) AN9619				
99629	<b>HI5741</b> AN9629	Multi-Tone Performance of the HI5741 (3 pages) AN9629				
99675	(General A/D Converters) AN9675	A Tutorial in Coherent and Windowed Sampling with A/D Converters (8 pages) AN9675				
DATA ACQUIS	DATA ACQUISITION TECH BRIEFS					
82325	(General DAQ), HI5721 TB325	Understanding Glitch In A High Speed D/A Converter (2 pages)				
82326	(General DAQ), HI5721 TB326	Measuring Spurious Free Dynamic Range in a D/A Converter (2 pages)				
82330	(General DAQ) TB330	Higher Speed Clock Rates Help Ease Filtering Requirements in Communication D/As (2 pages)				

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**Nova Marketing** 

8421 East 61st Street, Suite P Tulsa, OK 74133-1928 TEL: (800) 826-8557

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Suite 205 Dallas, TX 76248 TEL: (972) 733-0800 FAX: 972 733 0819

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Austin TEL: (512) 338-0287

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Dallas

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Compass Mktg. & Sales, Inc.

5 Triad Center, Suite 320 Salt Lake City, UT 84180 TEL: (801) 322-0391 FAX: 801 322-0392

**Allied Electronics** 

Salt Lake City TEL: (801) 261-5244

Arrow/Schweber Salt Lake City

TEL: (801) 973-6913

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Salt Lake City

TEL: (801) 261-5660

**Wyle Electronics** 

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**Newark Electronics** 

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#### WASHINGTON

Northwest Marketing Assoc.

12835 Bel-Red Road Suite 330N

Bellevue, WA 98005 TEL: (206) 455-5846 FAX: 206 451 1130

**Allied Electronics** 

Renton

TEL: (206) 251-0240

Almac/Arrow

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**Newark Electronics** 

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Spokane TEL: (509) 327-1935 Wyle Electronics

Seattle TEL: (206) 881-1150

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#### **WEST VIRGINIA**

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**Newark Electronics** 

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TEL: (304) 345-3086

#### WISCONSIN

**Oasis Sales** 1305 N. Barker Rd.

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FAX: 414 782 7921

Allied Electronics New Berlin

TEL: (414) 796-1280

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Brookfield TEL: (414) 792-0150

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7590 North Glenoaks Blvd. Burbank, CA 91504-1052 TEL: (818) 768-7400

Minco Technology Labs, Inc. 1805 Rutherford Lane

Austin, TX 78754 TEL: (512) 834-2022

FAX: (818) 767-7038

FAX: (512) 837-6285

Puerto Rican Authorized Distributor

**Hamilton Hallmark** Suite 318

S1 Mariolga Luis Munoz-Marin Caguas, Puerto Rico 00725

TEL: (800) 327-8950

South American Authorized Distributor

Graftec Electronic Sales Inc. One Boca Place, Suite 305 East 2255 Glades Road Boca Raton, Florida 33431

TEL: (561) 994-0933 FAX: 561 994-5518

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Graftec Brasil Ltda.

Rua Baronesa de Itu, 336 ci. 51/52 Sao Paulo - SP CEP: 01231-000

TEL: 55-11-826-1666 FAX: 55-11-826-6526

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7410 Pebble Dr. Ft. Worth, TX 76118 TEL: (800) 433-5700

**Anthem Canada** 300 North Rivermede Rd. Concord. Ontario Canada L4K 3N6 TEL: (416) 798-4884

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25 Hub Dr. Melville, NY 11747

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1941 Ringwood Avenue San Jose, CA 95131 TEL: (408)451-9400

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128 Carnegie Row Norwood, MA 02062 TEL: (617) 769-6000, x156 FAX: 617 762 8931

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FAX: 312 275-9596

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(Commercial Products) 3000 Bowers Avenue Santa Clara, CA 95051

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TEL: (800) 524-4735 Obsolete/Discontinued

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FAX: 508 462 9512

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Waidhausenstrasse 19 A - 1140 Vienna TEL: 43 1 911 28 47 FAX: 43 1 911 38 53

#### **EBV Elektronik**

Diefenbachgasse 35 A - 1150 Vienna TEL: 43 1 89 41 774 FAX: 43 1 89 41 775

#### Spoerle Electronic

Heiligenstädterasse 50-52 A - 1190 Vienna TEL: 43 1 360 46-0 FAX: 43 1 369 22 73

#### BELGIUM ACAL

Lozenberg 4 B - 1932 Zaventem TEL: 32 2 720 59 83 FAX: 32 2 725 10 14

#### **EBV Spoerle Electronic**

Keiberg II Minervastraat, 14/B2 B-1930 Zaventem TEL: 32 2 725 46 60 FAX: 32 2 725 45 11

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Arrow-Exatec A/S Mileparken 20E

DK-2740 Skovlunde TEL: 45 4492 7000 FAX: 45 4492 6020

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DK - 2730 Herlev TEL: 45 4488 0800 FAX: 45 4488 0888 **EBV Elektronik** 

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#### Independent Electronic Components

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#### Spoerle Electronic

Charkovska 24 CZ-10100 Praha 10 Czechoslovakia TEL: 42 2 73 13 54 FAX: 42 2 73 13 55

#### Spoerle Elektronic

ul. Domaniewska 41 PL-02672 Warszawa Poland TEL: 48 22 60 60 447

FAX: 48 22 60 60 348

#### FINLAND

Arrow Field OY

Niittylantie 5 FIN-00620 Helsinki TEL: 358 9 777 571 FAX: 358 9 798 853

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Italahdenkatu, 18 FIN-00210 Helsinki TEL: 358 9 61 31 81 FAX: 358 9 69 22 32 6

#### **EBV Electronics** Pihatorma 1A

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79, Rue Pierre Semard

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#### Sasco Semiconductor GmbH

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#### Spoerle Electronic

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**EBV Electronik** Anaxagora Street 1

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104 Aeolou Street GR - 10564 Athens TEL: 30 1 32 53 626 FAX: 30 1 32 16 063

#### ISRAEL **Aviv Electronics**

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IS - 43651 Ra'anana PO Box 2433 IS - 43100 Ra'anana TEL: 972 9 748 3232 FAX: 972 9 741 6510

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#### Lasi Elettronica

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#### Spoerle Electronic

Coltbaan 17 NL - 3439 NG Nieuwegein (Utrecht)

TEL: 31 30 609 1234

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#### Avnet Nortec A/S

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#### PORTUGAL

#### Amitron-Arrow

Quinta Grande, Lote 20 Alfragide P - 2700 Amadora TEL: 351.1.471 48 06 FAX: 351.1.471 08 02

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#### Arrow TH:s

Box 3027 Arrendevagen 36 S - 16303 Spanga TEL: 46 8 36 29 70 FAX: 46 8 761 30 65

#### Avnet Nortec AB

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#### Basix

Hardturmstrasse 181 CH - 8010 Zürich TEL: 41 1 2 76 11 11 FAX: 41 1 2761234

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CH-8610 Uster TEL: 41 1 9943290 FAX: 41 1 9943291 Spoerle Electronic

Cherstrasse 4 CH-8152 Opfikon-Glattbrugg

TEL: 41 1 874 6262 FAX: 41 1 874 6200

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#### Laser Electronics Ltd.

Ballynamoney Greenore Co. Louth, Ireland TEL: 353 4273165 FAX: 353 4273518

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Comtech House 28 Manchester Road Westhoughton **Bolton** Lancs, BL5 3QJ

TEL: 44 1942 851 800 FAX: 44 1942 851 808

#### Stuart Electronics

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#### Arrow Jermyn

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#### **Electronic Services** Edinburgh Way., Harlow

Essex CM20 2DF TEL: 44 1279 626777 FAX: 44 1279 441687

#### **Farnell Components**

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#### **IEC Micromark Electronics** Boyn Valley Road

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#### Hollybank

13 Burn Bridge Oval Burn Bridge, Harrogate North Yorkshire, HG3 1LR TEL: 44 423 871553

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Corbrook Rd., Chadderton Lancashire OL9 9SD TEL: 44 161 626 3827 FAX: 44 161 627 4321 TWX: 668570

#### **Rood Technology**

Test House Mill Lane, Alton Hampshire GU34 2QG TEL: 44 1420 88022 FAX: 44 1420 87259 TWX: 21137

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TEL: 612-8945244 FAX:612-8945266

#### CHINA/HONG KONG Harris Semiconductor China Ltd

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### Harris Semiconductor China Ltd.

 \* Unit 1801-2, 18th Floor 83 Austin Road
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Edal Electronics Co., Ltd. Room 911-913, Chevalier Commercial Centre, 8, Wang Hoi Road, Kowloon Bay, Kowloon TEL: (852) 2305-3863 FAX: (852) 2759-8225

### Golden Way Electronics (HK) Ltd.

Wharf Cable Towers 9 Hoi Shing Road, N.T. Hong Kong TEL: (852) 2499-3109 FAX: (852) 2417-0961

#### Lucas Trading

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TEL: (852) 2790-8073 FAX: (852) 2763-5477

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#### Intersil Private Limited

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#### **Graftec Elec**

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#### Graftec India

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TEL: (91) 80-661 1095 FAX: (91) 80-222 6490

#### BBS Electronics (India) Pvt Ltd

309 Richmond Tower No 12, Richmond Road Bangalore 560025 TEL: (91) 80-221-7912 FAX: (91) 80-227 8043

#### S M Creative Electronics Ltd 10 Electronic City

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